Physical Circuit-Device Simulation of ESD and Power Devices

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I. Introduction

Physically accurate simulation of electrostatic discharge (ESD) and power semiconductor devices is not possible with conventional SPICE compact models due to complex physical effects relevant at high-field high-current conditions typical for such devices and their applications, as well as complex device geometries not captured by compact models especially for power devices. Mixed-mode circuit-device simulation provides an established however not widely used methodology for incorporating accurate finite-element (FEM) level semiconductor device models in SPICE-type circuits. This mixed-mode approach offers the circuit/device designer a tool to obtain physically accurate predictions of circuit and device behavior including internal characteristics such as heating and damage. Obstacles to wider use are difficulties in setting up FEM models for devices, long simulation times and ease-of-use issues and general unfamiliarity with the approach. We describe a streamlined, proven industrial procedure for accurate mixed-mode SPICE-FEM simulations, which uses device synthesis and calibration to ease FEM model creation, and user interface tools to ease circuit simulation setup and execution [7],[8],[9],[10].

Generally the ESD tolerance of high voltage devices is low in comparison with the logic device. This is because the high voltage device has high breakdown voltage between source and drain, and the breakdown current is not uniform in p-n junctions when an ESD surge current flows. Therefore, the design of the ESD protection device is difficult due to weakness of the device itself. As a result, mixed-mode simulation and physical analysis calibrated to TLP data is indispensable to circuit network optimization of an ESD current path in ESD protection design of high voltage devices. TLP-calibrated SPICE-FEM analysis generates predictions for internal temperatures in devices as a function of time. These temperature predictions are then used for reliability assessments, in particular for the slower ESD events such as HBM (Human Body Model) and in some cases MM (Machine Model).

Our ESD modeling uses 2D FEM models since full three-dimensional simulation for ESD problems would require enormous computing resources as well as engineering resources to set up and calibrate the simulation, while a solution for ESD problems is required within the short period of IO design. In cases where channel width dependence is important, we use fast 2D simulations based on interpolation of devices with different channel width or a circuit-level combination of multiple 2D devices - "2.5D" simulation.

II. High-Current Data (TLP) for Calibration of FEM Models

Experimental characterization of ESD protection devices commonly relies on Transmission Line Pulse (TLP) measurements. Using short current pulses to trace IV allows collection of data at high current levels without damaging the device by overheating. Therefore TLP data is used to capture device electrical behavior Fig. 1, Fig. 2. Device structure information such as doping profiles, oxide layer thicknesses, etc. comes from process simulation or measurements such as SIMS. If some of this information is nor available as may be the case with foundry processes, tuning of doping profiles to match TLP data is used in an "inverse modeling" procedure.

III. Synthesis of Devices and Calibration to TLP

Constructing good quality FEM models is frequently an obstacle to effective use of SPICE-FEM simulations. We use automatic mesh generation and device synthesis (or imported process simulator structures in some cases). As an example Fig. 3 shows the structure and mesh created for the high-voltage NMOSFET in Fig. 2. Parameters are used by the user in a spreadsheet interface to select the specifics of the device. The IV characteristic of the synthesized device is then calculated and compared to TLP for validation and adjustments to the device structure or models (calibration).

IV. Mixed-Mode Circuit Simulation Setup and Execution

SPICE-FEM simulation embeds calibrated FEM device models in realistic circuit environments, which can contain a number of other such FEM device models if necessary, and of course standard compact SPICE models

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for active and passive devices Fig. 5. Our simulation system [7] then carries our a transient simultaneous solution of the circuit equations with automatic time-step control. Circuit behavior (node potentials and currents) is obtained Fig. 6, as well as device internal conditions (electric field, current flow, impact ionization rate, temperature etc.) and can be used by the designer to judge circuit/device performance under target operating conditions Fig. 7, Fig. 8. Simulation times are between 3 minutes (HBM, no heat) to 13 minutes (MM) on a quad-core machine.

V. Results and Conclusions

An industrial methodology for physically accurate and efficient simulation of high-field/high-voltage events such as ESD and power applications has been presented. The methodology has been applied to a number of varied industrial problems with excellent results validated by experimental data. Our approach helps make physical simulation available to designers in cases where simulation has not been widely used previously, in particular for circuit optimization of ESD protection in logic as well as power ICs.

VI. References

7. SEQUOIA Device Designer - ESD, Reference Manual, SEQUOIA Design Systems

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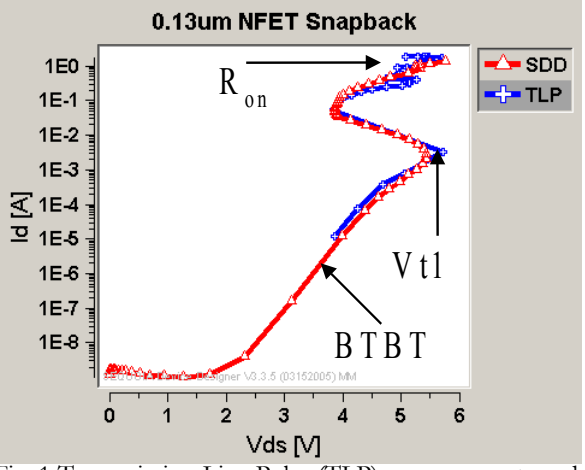

Fig. 1 Transmission Line Pulse (TLP) measurements and calibrated simulation results for a 0.13um ESD protection NMOSFET. Band-to-band tunneling leakage is clearly seen as a straight line in the pre-breakdown part of the curve (log scale plot).

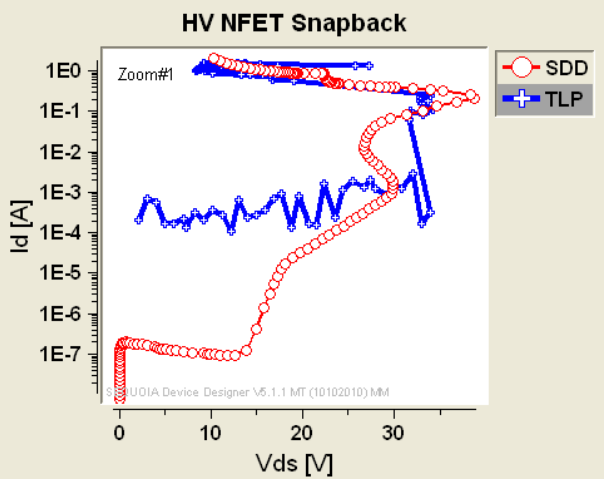

Fig. 2 Transmission Line Pulse (TLP) measurements and calibrated simulation results for a high-voltage NMOSFET. Higher triggering voltage and more complex behavior in comparison to Fig. 1 is evident. TLP resolution limits measured current accuracy at low levels <1e-3A.

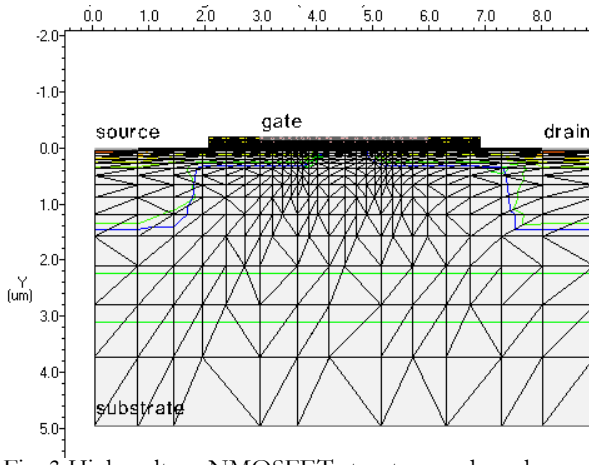

Fig. 3 High-voltage NMOSFET structure and mesh, TLP and breakdown simulation results for this device are shown in Fig. 2

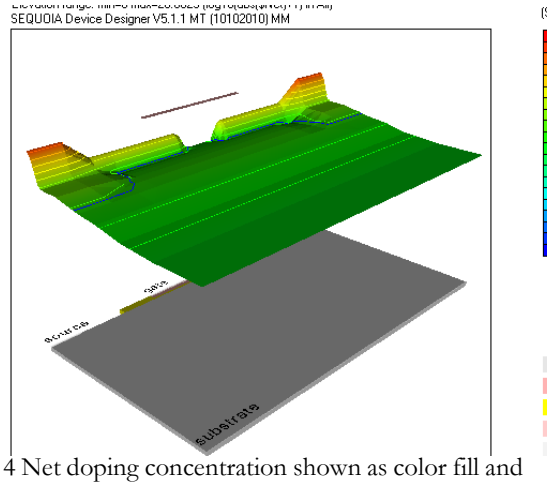

Fig. 4 Net doping concentration shown as color fill and elevation plot (same device as in Fig. 2, Fig. 3)

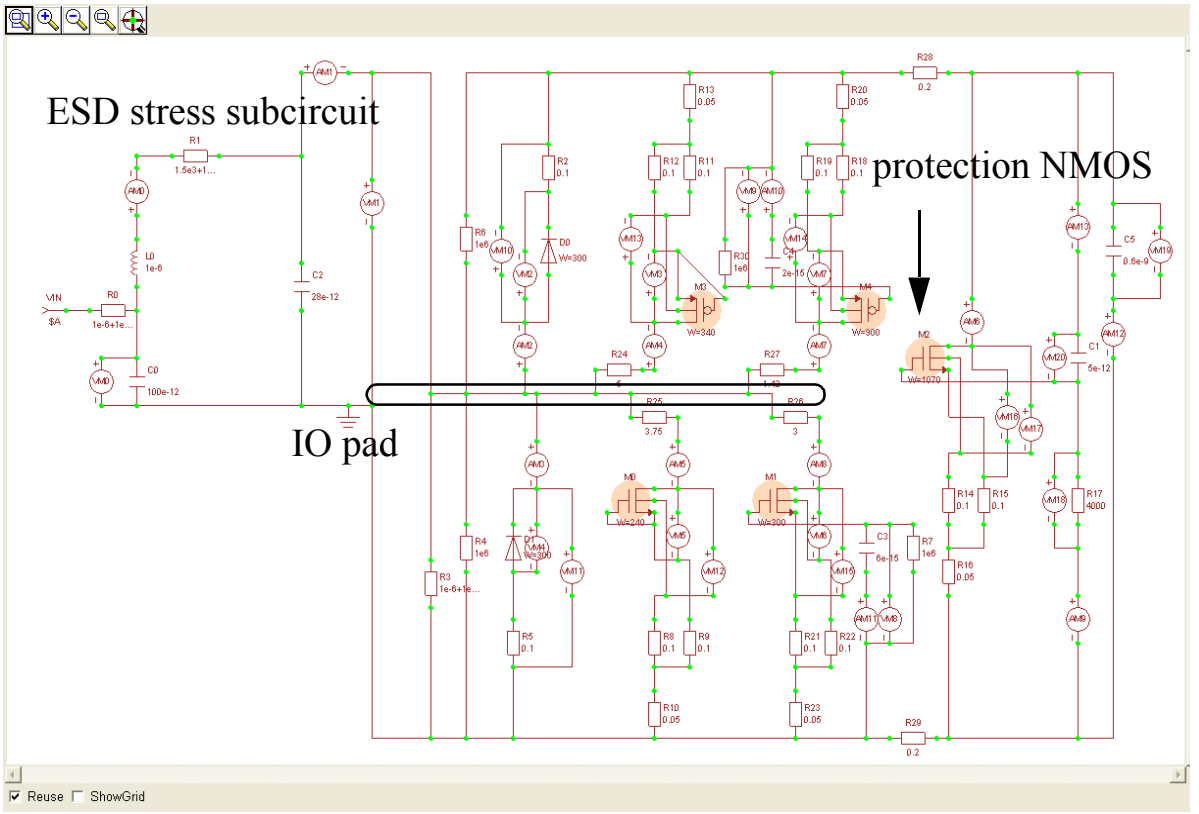

Fig. 5 A typical SPICE-FEM ESD simulation circuit including the protection ggNMOS, I/O buffer and ESD stress subcircuit. A total of 7 FEM devices is included: 3xNMOS, 2xPMOS, 2xDiodes.

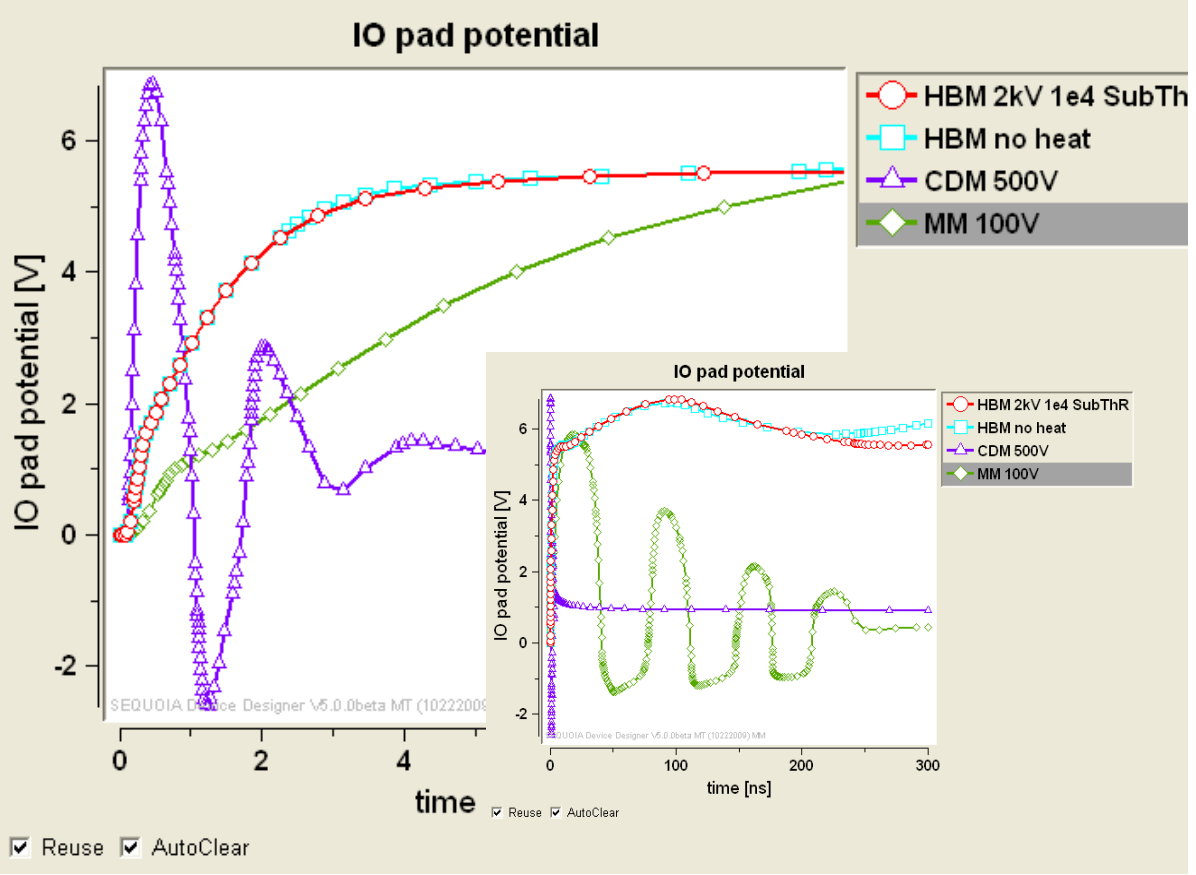

Fig. 6 IO pad potential waveforms for HBM 2kV, CDM 500V and MM 100V stress, the first 10ns of ESD stress response shown in the larger picture, 300ns in the insert at lower right. Typical discharge patterns are seen: very fast oscillations for CDM, slower oscillations for MM, slowest waveforms for HBM. Simulation times are between 3 minutes (HBM, no heat) to 13 minutes (MM) on a quad-core machine.

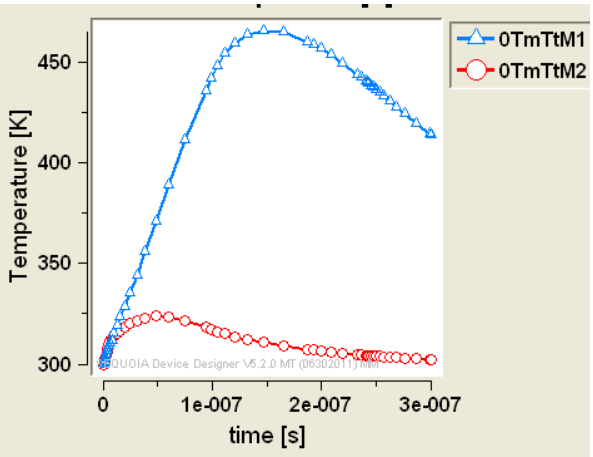

Fig. 7 Self-heating in FEM devices is monitored by examining the peak temperature versus time. The strongest heating in circuit Fig. 5 under HBM stress occurs in the I/O driver MOSFET M1, while the protection MOSFET M2 shows much less heating due to its larger width.

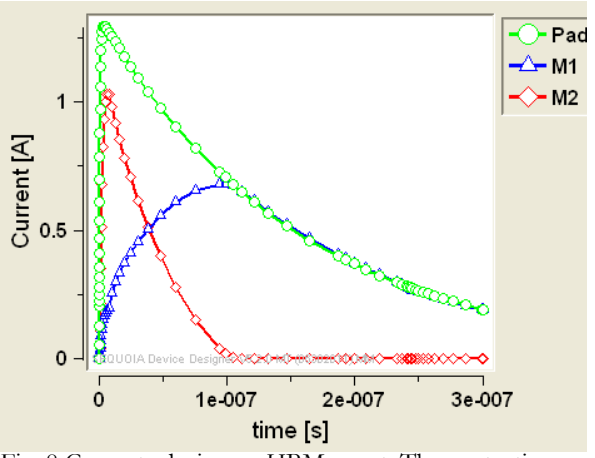

Fig. 8 Currents during an HBM event. The protection device M2 carries most of the discharge (Pad) current early on. However, for t>1ns the I/O driver MOSFET M1 triggers and conducts significant current leading to device heating as shown in Fig. 7. Damage due to overheating or current overstress may result.