

Characterization and Modeling of Self-Heating Effect on Transient Current Overshoot in Poly-Si TFTs Fabricated on Glass Substrate

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Abstract—Characteristics of transient drain current overshoot in poly-Si TFTs are measured, and an equivalent thermal circuit model is proposed based on the experimental results. By changing the terminals on which a step voltage is applied, two main mechanisms causing the transient current, i.e., the electron trapping effect and the self-heating effect, can be separately evaluated. Using this new technique, we discuss the heat conduction mechanisms in TFTs responsible for describing the transient current overshoot component induced by the self-heating effect.

Keywords- Poly-Si TFT; Overshoot Current; Self-Heating Effect; Heat Conduction Model

I. INTRODUCTION

Poly-Si thin film transistors (TFTs) are widely used as switching devices in active-matrix liquid crystal displays. Recently, their performance of Poly-Si TFTs has been significantly improved, enabling to realize more functional digital and analog circuits implemented on a glass substrate, i.e., system-on-panel [1]. Therefore, an accurate device modeling for poly-Si TFTs is now strongly required not only for the steady state [2] but also for the dynamic properties.

It is well-known that the drain current overshoot is observed in the transient turn-on characteristics of poly-Si TFTs [3-5]. One of the origins of this phenomenon has been attributed to the electron trapping to the defect sites in poly-Si grain boundaries and poly-Si/SiO₂ interfaces, causing the stretched-exponential type relaxation [4]. Furthermore, the self-heating effect also induces the transient current decay particularly under high bias conditions similarly to SOI MOSFETs. However, the thick glass substrate beneath the poly-Si film significantly impedes the thermal conduction and enlarges the time constant for the transient state (~ 1 sec [6]), which is orders of magnitude larger than that of SOI MOSFETs (~ 1 μ sec [7, 8]). Note that the time constant of the carrier emission and capture to the traps is considered to be 10^{-5} sec - 10^{-3} sec [4, 5], indicating that both the electron trapping effect and the self-heating effect simultaneously occur during the transient operation of TFTs. Hence, the mixture of these two mechanisms makes it difficult to understand the transient characteristics of TFTs.

In this work, we experimentally characterize the transient drain current in poly-Si TFTs, and try to separate the two main mechanisms causing the overshoot. Then, a simple equivalent circuit model is presented especially focusing on the self-heating effect, and the validity of the model is discussed through the comparison with the experimental and the numerical simulation results.

II. MEASUREMENT METHOD AND RESULT

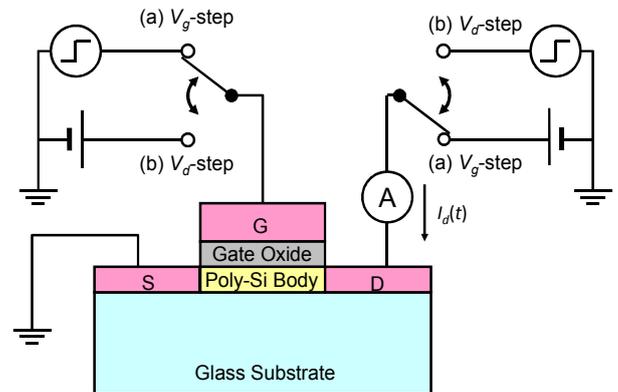


Figure 1 Schematic view of the measurement setup used in this study. The thicknesses of the gate oxide, the poly-Si body, and the glass substrate are 80 nm, 50 nm, and 1 mm, respectively. The switches were set to either (a) V_g -step or (b) V_d -step configurations.

The samples used were *n*-channel poly-Si TFTs with a gate length of $L = 4$ μ m and various gate widths W ranging from 1.3 μ m to 100 μ m. The measurement setup is presented in Fig. 1. In this study, all the data were obtained using an Agilent B1530A. The source terminal was grounded, and a step voltage (rise time = 0.1 μ sec) was applied to either of the gate (V_g -step) or drain terminals (V_d -step), while a constant voltage was applied to the other. Then, the time evolution of the drain current $I_d(t)$ was monitored until steady state was achieved ($t = 100$ sec).

Figure 2 shows the turn-on transient decays of drain current measured with V_g -step and V_d -step methods. The used bias condition was high enough to cause the self-heating effect, and the data are normalized to their steady-state values $I_d(100$ sec). The long time scale relaxation, which could hardly be described by an exponential function with a single time constant, was observed. Since a finite time is needed for electrons to be captured by the traps, the free electron density in the channel just after turning on V_g is larger than in the steady state condition. This is one of the origins of the transient decay of I_d in poly-Si TFTs containing high-density traps [3-5]. It is considered that widely distributed emission/capture time constants cause the stretched exponential relaxation [4].

The other possible origin is the self-heating effect [6]. If the step voltage is applied not to V_g but V_d , the effect of the electron trapping is expected to be suppressed, because trap states have been occupied by the electrons under the constant V_g before the drain current started to flow. The solid lines in Fig. 2 show the data obtained from V_d -step measurements; the

magnitudes of the overshoot are lower than V_g -step method (dashed lines). The difference between the two curves of these measurements (indicated by the double-headed arrows) is considered to represent the contribution of the traps, which is almost independent of W (this is a reasonable result). On the other hand, the self-heating effect, which can be evaluated from the data of V_d -step, is found to strongly depend on W , consistent with the previous report investigating the self-heating-induced TFT degradation [9]. The solid line curves in Fig. 2 suggest that in poly-Si TFTs the transient decay originating from the self-heating effect could not be modeled by the exponential relaxation with a single time constant unlike with the case of SOI FETs [8].

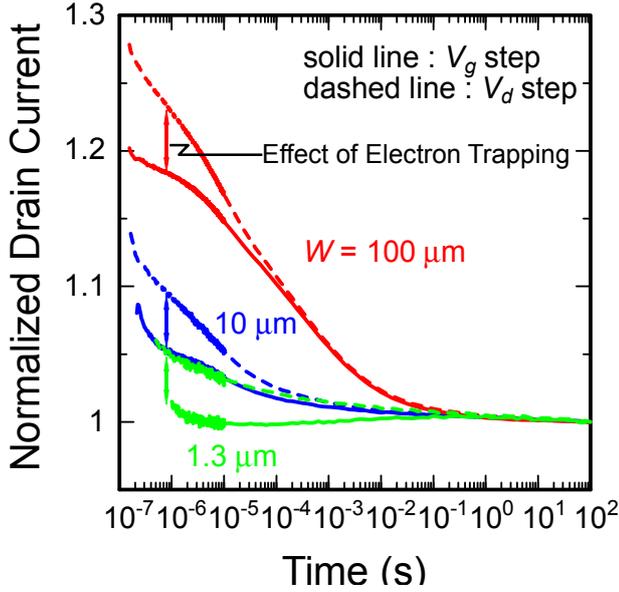


Figure 2 Turn-on transient decay of drain current $I_d(t)$ measured with V_g -step (dashed lines) and V_d -step (solid lines) methods. In this experiment, the poly-Si TFTs with $L = 4 \mu\text{m}$ and $W = 1.3, 10, 100 \mu\text{m}$ were used, and the applied voltages were $V_d = 5 \text{ V}$ and $V_g = 10 \text{ V}$. The data are normalized to their steady-state values $I_d(t = 100 \text{ sec})$.

III. MODELING OF SELF-HEATING EFFECT

In order to understand the transient decay behavior of $I_d(t)$ originating from the self-heating effect, a simple simulation based on the equivalent thermal circuit model was carried out. As shown in Fig. 3 (a), we considered the hemispherical volume of the glass substrate beneath the TFT, and its heating due to the power dissipation from the TFT was simulated. The region was divided into N shells, and their thermal resistances R_i and capacitances C_i were calculated according to the analytical formula [10] summarized in TABLE I. In the present study, the effective value of the thermal resistance in the innermost hemisphere R_0^* was given by hand, considering that it would contain the effect of the complex heat flow paths just below the device as well as the heating property in the poly-Si device region. Consequently, the equivalent thermal circuit solved by the SPICE simulator was as shown in Fig. 3 (b), where the power dissipation from the TFT was modeled by a constant current source, and each node voltage corresponds to the temperature rise.

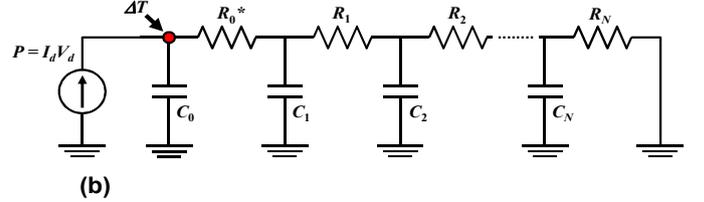
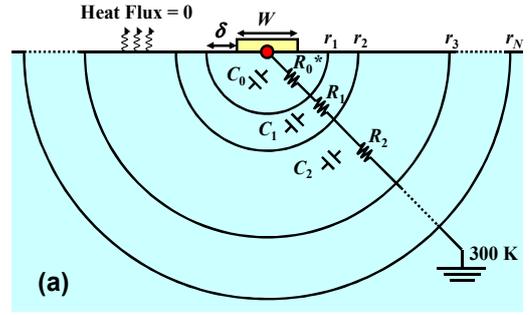


Figure 3 Schematic view of the equivalent thermal circuit model for heat conduction in the glass substrate beneath the poly-Si TFT. (a) Cross-sectional view. The glass substrate was divided into many hemispherical shells. (b) Thermal circuit solved in this study. The power dissipation from the TFT was modeled by a constant current source, and the node voltage indicated by an arrow corresponds to the temperature rise ΔT at the device.

TABLE I. EQUATIONS AND PARAMETERS USED IN THE EQUIVALENT THERMAL CIRCUIT MODEL SHOWN IN FIG. 3. THE VALUES OF R_i AND C_i ($i = 1 \dots N$) WERE CALCULATED ANALYTICALLY, WHILE THE EFFECTIVE THERMAL RESISTANCE OF THE INNERMOST HEMISPHERE WITH A RADIUS OF $r_i = W/2 + \delta$ (REPRESENTED AS R_0^*) WAS GIVEN BY HAND.

Input Power	$P = I_d V_d$
Thermal Registance	$R_i = \frac{1}{2\pi k} \left(\frac{1}{r_i} - \frac{1}{r_{i+1}} \right)$
Thermal Capacitance	$C_i = \frac{2\pi r \rho c_p}{3} (r_{i+1}^3 - r_i^3)$
Discretization along r	$r_i = (r_1 - 1) + (r_N - r_1)^{(i-1)/(N-1)}$
Thermal Conductivity, k (W/m·K)	1.4
Density, r (kg/m ³)	2,270
Specific Heat, c_p (J/kg·K)	1,000

To confirm the accuracy of this model, we compared the obtained results to the rigorous numerical solution of the heat diffusion equation as Fig. 4. The thermal circuit model with the larger N can yield the better results. The large number of RC components produces many poles in the circuit, and the stretched exponential behavior can be well described. As shown in Fig. 5 we measured the temperature dependence of the DC drain current under the bias condition with negligible self-heating effect, and then using this information the transient

decay of $I_d(t)$ was simulated as Fig. 6. Not only the long-time relaxation behavior, but also the W dependence of the experimental results was well reproduced by the simple equivalent thermal circuit analysis. It is well known that self-heating becomes more significant in the wider W devices [9]. There are two possible reasons for this observation. Firstly, the Joule heat generation, which is proportional to the input power $P (= I_d V_d)$, is larger in the wider devices, because I_d is proportional to W . Secondly, the heat removal efficiency from the hot spot in the drain would be worse in the wider TFTs, but this mechanism could not be fully included in our present model. Moreover, note that in Fig. 6 the measured data decreases rapidly compared to the simulation, indicating that the modeling accuracy near the hot spot is not enough. For example, around the drain region in TFTs, the generated heat would spread not spherically but rather cylindrically. For the improvement (and further including the trap-related effects), more RC components should be added, but it is a trade-off against the model simplicity and the computational time.

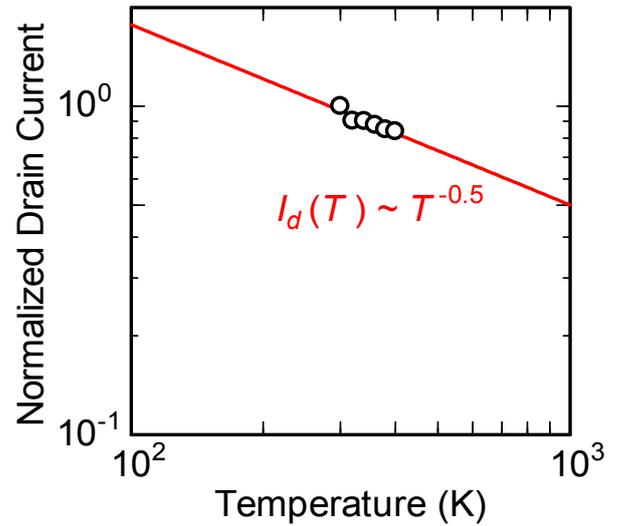


Figure 5 Temperature dependence of the drain current of the poly-Si TFT measured with $V_g = 10$ V and $V_d = 0.1$ V, where the self-heating effect is negligible. The data can be well fitted by a power law function $\propto T^{-0.5}$, which was used for the transient current simulation.

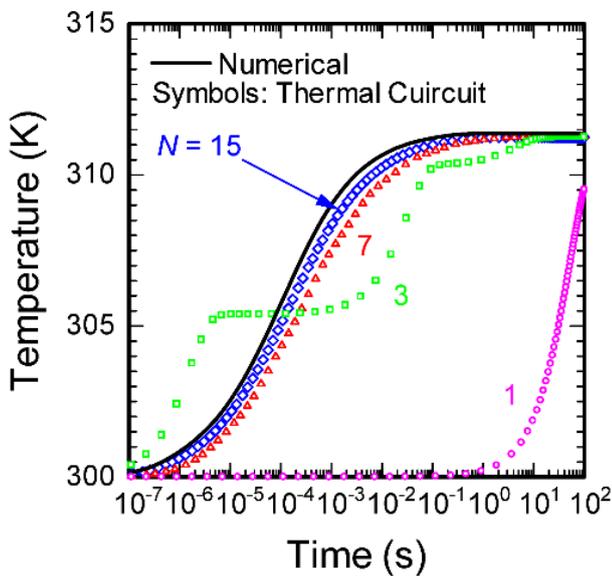


Figure 4 Temperature evolution in the glass substrate at $r = r_1$ obtained by solving the partial differential equation of heat conduction (solid line) and the thermal circuit with various N (symbols). The boundary conditions assumed were (i) the heat flux = $1 \text{ mW} / (2\pi r_1)$ at $r = r_1$ and (ii) $T = 300$ K at $r = r_N$, where $r_1 = 10 \mu\text{m}$ and $r_N = 1$ mm.

IV. SUMMARY

The turn on transient overshoot of $I_d(t)$ in poly-Si TFTs has been measured, and the effect of the self-heating was discussed using the equivalent thermal circuit model. By comparing the data obtained from V_g -step and V_d -step measurements, the current decay component associated with the self-heating was separated from that due to the transient electron trapping. It was revealed that the current relaxation in poly-Si TFTs could hardly be described by the exponential decay function with a single time constant, and the heat conduction modeling through the thick glass substrate beneath the TFT was proposed to understand the observed results.

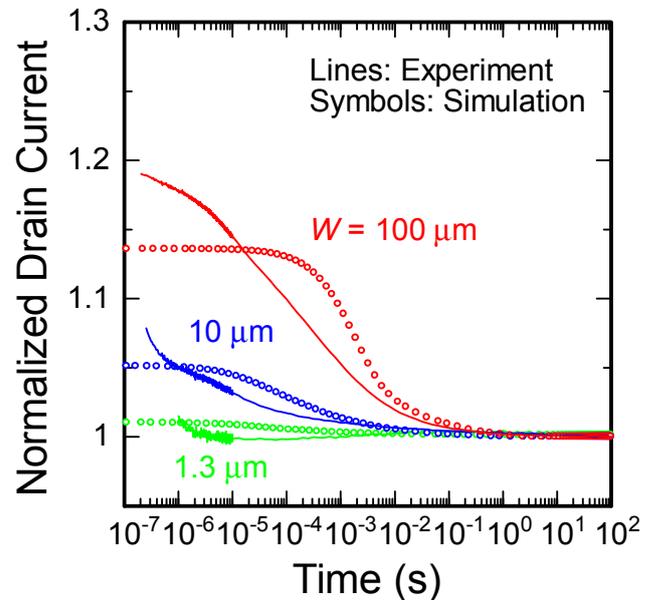


Figure 6 Turn-on transient decay of the drain current simulated by taking account of the self-heating effect (symbols) compared with the V_d -step measurements (solid lines). For all the calculations, regardless of W , the parameters $R_0^* = 2 \text{ K/W}$, $\delta = 5 \mu\text{m}$, $r_N = 1$ mm, and $N = 7$ were assumed.

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