Accurate and global model of SOI H gate body-tied MOSFET for circuit simulator

M. Mochizuki, H. Hayashi, S. Ishii, S. Ohira and I. Kurachi†
OKI SEMICONDUCTOR CO., LTD.
Yokohama, Japan
mochizuki877@mnf.okisemi.com

N. Miura
OKI SEMICONDUCTOR MIYAGI CO., LTD.
Miyagi, Japan

***Abstract*—Drain current of SOI H-type body-tied MOSFET can be modulated in gate length or width because of its additional gate region. It causes a serious problem especially in analog circuit design. There is, however, no model including the gate shape effect even in the newest release BSIMSOI [1]. An accurate and global model of SOI H-type body-tied MOSFET in circuit simulation has been proposed for the first time. It is confirmed that the simulation accuracy of the proposed model has greatly improved within 10% RMS error compared to the existing model.**

Keywords-SOI; body-tied; H gate; circuit simulation; compact model

I. Introduction

SOI MOSFETs have superior advantages such as small junction capacitance, good switching characteristic by low sub-threshold swing, and radiation hardness [2]. In addition, off-leakage control in a 22nm technology node becomes difficult and it is expected that the SOI MOSFETs are one of the candidates [3]. Moreover in power MOSFET field, they consider SOI MOSFETs are very attractive because of full dielectric isolated transistors and their latch-up free and robustness at high temperature operation [4, 5]. On the other hand, with consideration of analog operation by such the SOI MOSFETs, control of body potential is the most crucial problem because of their body-floating effect. To solve it, H-gate body-tied structure has been proposed [2]. In such structure which has additional gate region as shown in fig. 1, a predictable model is required for accurate circuit simulation. In fact, some compact models include a gate shape effect in the AC characteristic [1, 6, 7]. In contrast, DC current model which includes the H gate effect has not expressed precisely yet [1, 6]. In this paper, we propose a new global model for circuit simulation including the H gate effect in the DC characteristic.

II. Drain Current Channel Width Dependence

Figure 2 shows the channel width dependence of the drain current normalized by Wg, Ids/Wg, for the channel length Lg=0.7µm of the H-type SOI MOSFET. Ids/Wg extremely increases at narrow gate width. For Lg=0.7µm, the effective channel width Weff is expressed as Weff=Wg+0.74 which is ΔWg=0.74µm. However, ΔWg depends on Lg as shown in fig. 3. Therefore, ΔWg needs to be expressed by a formula with Lg as a parameter.

III. TCAD Exiperiment

In order to understand that phenomenon in physically, the 3D process/device simulation using HyENEXSS [8] is employed. Figure 4 shows the simulation structure. SOI thickness is 280 nm and buried oxide thickness is 1 µm. The simulation results show good agreement with measured data as shown in fig. 5. Fig. 6 shows the channel length dependence of

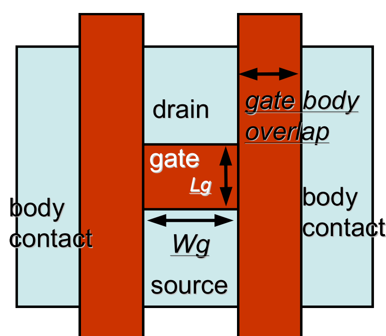

Figure 1. H-gate SOI MOSFET.

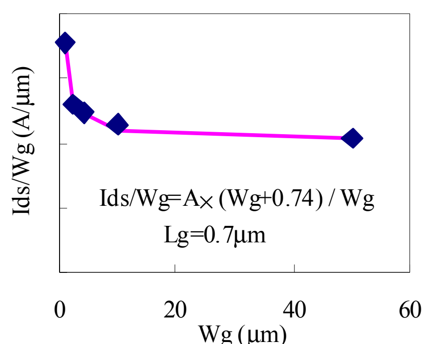

Figure 2. Channel width dependence of Ids per unit channel width. Symbols are measured. Solid line is approximate formula Ids/Wg=A×(Wg+0.74)/Wg, where A is proportionality constant.

†) Current address: Memory Operation Business Group, Powerchip Technology Corporation

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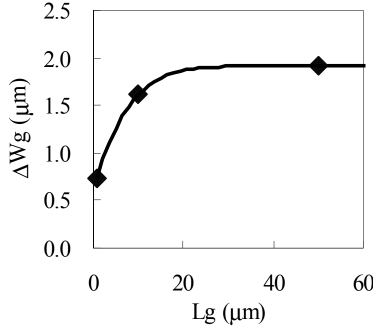

Figure 3. Channel length dependence of ΔWg. ΔWg equals 0.74μm at Lg=0.7μm, increases as a longer channel length, and approaches to 1.9μm in Lg>30μm.

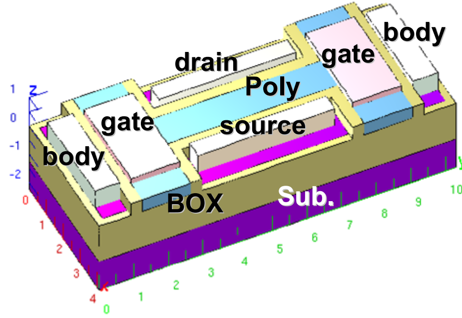

Figure 4. Simulated structure.

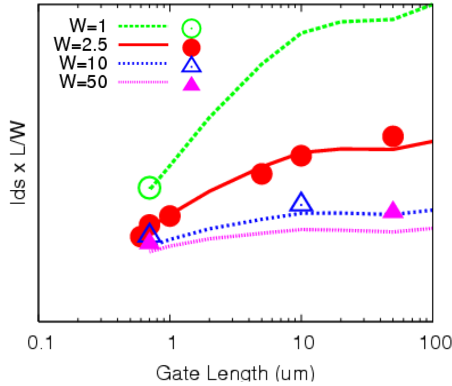

Figure 5. Channel length and width dimension dependence of the Ids normalized by L/W. Symbols are measured data, and lines are simulation. Vg=Vd=2.5V.

the channel center (Lg/2) electron current density at Si surface for Lg=0.7~20μm and Wg=1μm. When the gate width is enough longer as >5μm, the current density at the gate body overlap (GBO) region is almost the same as the channel current density. However, the current density at the region is decreasing compared to channel center one with the channel length decreasing. The channel width dependence of the channel center (Lg/2) electron current density at Si surface for Lg=0.7μm and Wg=1~10μm is also illustrated in fig. 7. The distributions of the current density in GBO region are same at various Wg, if Lg is same. It is confirmed again by the simulation that the current in the GBO region is only function

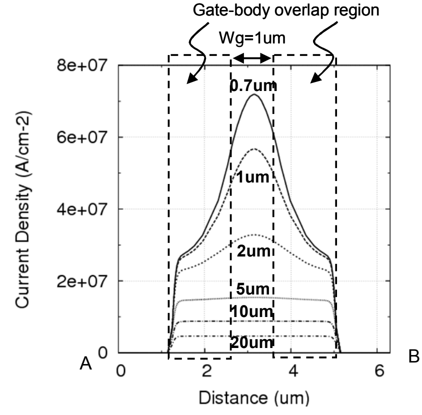

Figure 6. Gate length dependence of channel center electron current density distribution at Si surface. Wg=1μm. Vg=Vd=5V.

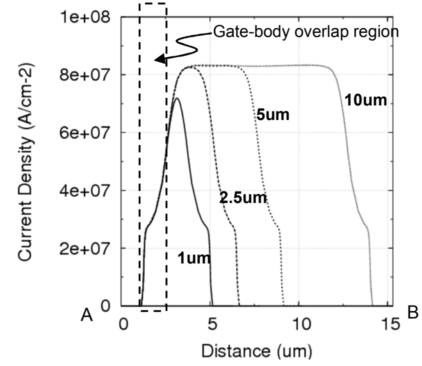

Fig. 7: Gate width dependence of electron current density distribution of Si surface at channel center. Lg=0.7um. Vg=Vd=5V.

of Lg but not Wg. This must be taken into accout in the proposed model.

IV. Model

The total drain current is assumed to flow the two regions which are the channel and the GBO regions through channel and source/drain resistors as shown in fig. 8. Because it can be assumed that the current of the channel region (Ids1 in fig.8) is proportional to Wg, the total drain current can be expressed as follows,

$$Ids = \frac{Vd}{Rch + Rsd} + \frac{Vd}{Rh + Rhsd} \quad (1),$$

$$= \frac{Vd}{\rho ch \times (Lg - \Delta Lch) + Rsd'} \times Wg + \frac{Vd}{Rh' \times (Lg - \Delta Lh) + Rhsd}$$

where ρch (Ω) is channel sheet resistance, Rsd' (Ω·μm) normalized SD resistance, Rh' (Ω/μm) normalized channel resistance at the GBO region, Rhsd (Ω) SD resistance at the GBO region. ΔLch and ΔLh are channel offset length of the channel region and the GBO region respectively. We confirmed that (1) is reasonable by using TCAD results. The collinear approximation error of the Ids-Wg characteristics of various Lg is less than 2.3% (fig. 9 - 10).

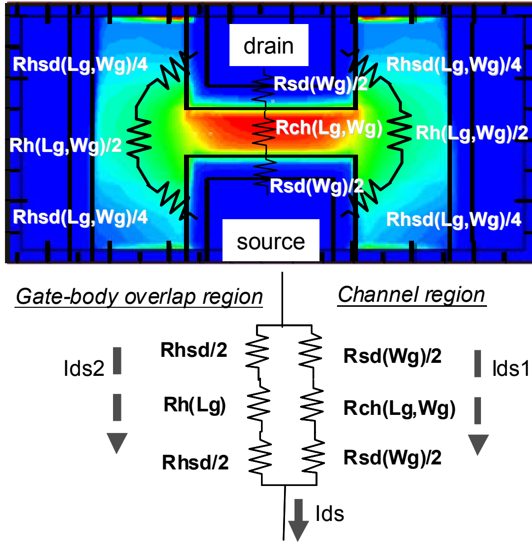

Figure 8. Electron current density distribution and schematic of equivalent circuit.

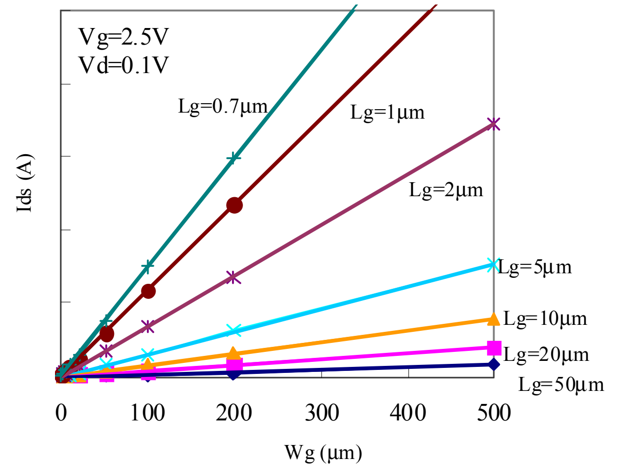

Figure 9. Ids-Wg characteristics of various Lg approximate to linear line

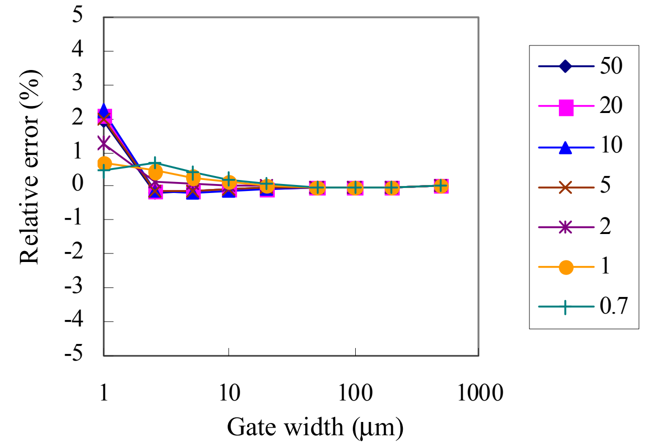

Figure 10. Ids-Wg characteristics of various Lg.

The channel resistance is also assumed to be inversely proportional to Vg-Vth. Consequently, the effective channel width can be written as follows,

$$\begin{aligned} Weff &= Wg + \Delta Wg \\ &= Wg + \frac{(\rho ch'/(Vg-Vth)+\alpha)\times(Lg-\Delta Lch)+Rsd'}{(Rh''/(Vg-Vth)+\beta)\times(Lg-\Delta Lh)+Rhsd} \end{aligned} \qquad (2),$$

where ρch' (Ω·V) is variation of channel sheet resistance by gate bias and Rh" (Ω·V/µm) normalized channel resistance variation at the GBO region. α and β are the fitting parameters.

V. Accuracy Improvement

All of the model parameters in (2) are extracted by using Terada's method [9] from measured IV data (Table 1). ΔLh of GBO region is -2.4um, and the effective channel length is extended because the current flows around GBO region. Rhsd is 368Ω and very small in comparison with ρch, 985Ω·µm. The effective gate width of GBO region current flow is boundary length between source/drain region and body contact region, and it is 2.7µm. Thus, the Rhsd becomes 368 × 2.7 = 994Ω and it is almost same as Rsd′.

Figure 11 shows the channel length dependence of ΔWg-(Vg-Vth) characteristics. The measured data are extracted from Ids-Wg characteristics using the least squares method as same as fig. 1. The calculated results with extracted parameters represent well the measured data.

To install the channel width modulation model as (2) in the BSIM3v3 model, a macro model is newly introduced. We use the analog behavior model to describe the gate voltage dependency of current amplification of GBO region in sub-circuit. Accuracy of the model is confirmed at wide range in gate length and width as shown in fig. 12 by comparison with simulated data by existing model. Because the parameter extraction has been performed on L=0.7µm and W=2.5µm for existing model, fitting error of longer gate length is too high as explained above. On the other hand, simulated data by the proposed model are well matched to measured ones and we can keep RMS error less than 9% with the range of 0.7-10µm in gate length and 2.5-10µm in gate width.

VI. Conclusion

We proposed the DC characteristic model which expresses the gate shape effect of H-type SOI MOSFET. In this model, the current through GBO region is expressed as the current flows in extra channel width ΔWg, which formula contains Lg and Vg as parameters. This model is implemented into SPICE simulator as a macro model. It is confirmed that this model improved the simulation accuracy from 27% to 8.4%.

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TABLE I. EXTRACTED PARAMETERS

ρch'	7730(Ω·V)
Rsd'	985(Ω·μm)
ΔLch	-0.27(μm)
Rh"	5767(Ω/μm·V)
Rhsd	368(Ω)
ΔLh	-2.4 (μm)

α and β are excepted.

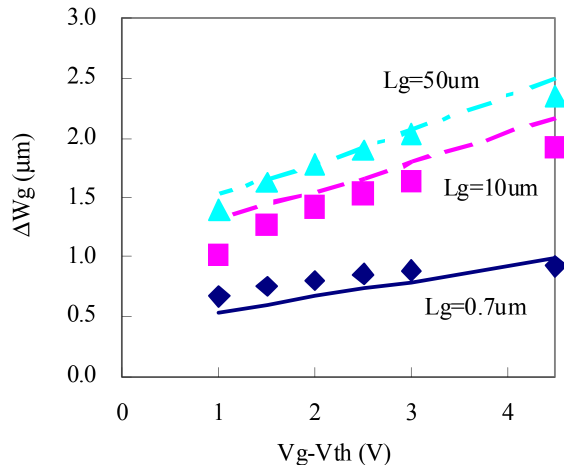

Figure 11. Drive voltage dependence of ΔWg. The lines are calculated data with proposed model and the symbols are measured data.

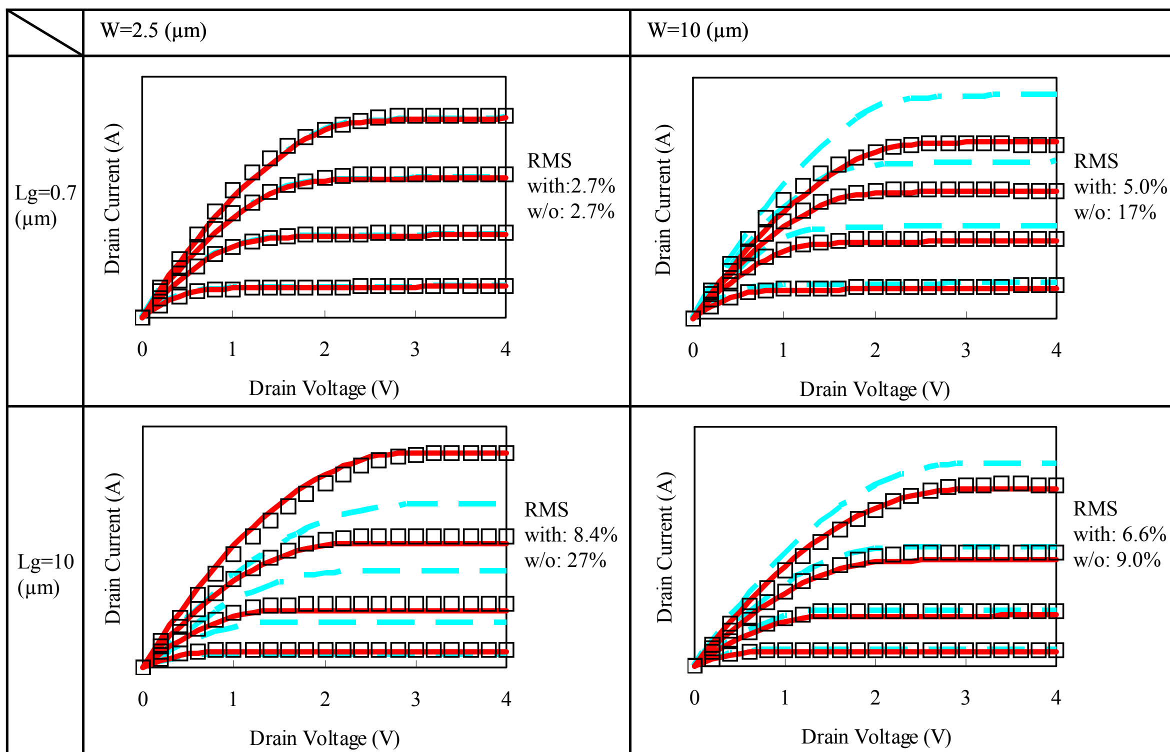

Figure 12. Id-Vd characteristics. Symbols are measured data. Lines are simulated; solid: with this model; dashed: w/o the model.