Analysis of Worst-Case Hot-Carrier Degradation Conditions in the Case of n- and p-channel High-Voltage MOSFETs

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***Abstract*—We have analyzed the worst-case conditions of hot-carrier induced degradation for high-voltage n- and p-MOSFETs with our model. This model is based on the evaluation of the carrier distribution function along the $\mathbf{Si/SiO_2}$ interface, i.e. on thorough consideration of carrier transport. The distribution function obtained by means of a full-band Monte-Carlo device simulator is used to calculate the acceleration integral, which controls how effectively the carriers are breaking $\mathbf{Si-H}$ bonds. Therefore, we analyze the worst-case conditions using this integral as a criterion. We compare the simulated picture with the experimental one and conclude that the model fits the experimental data precisely well for both transistor types.**

I. Introduction

The worst-case conditions (WCC) of hot-carrier degradation (HCD) in the case of a long-channel n-MOSFET are reached when the substrate current $I_{\rm sub}$ is at its maximum [1]–[4]. It is usually assumed that this maximum corresponds to the interrelation between gate and drain voltages: $V_{\rm gs} = (0.4 \div 0.5)V_{\rm ds}$. As for long-channel p-MOSFETs, WCC are achieved at the maximum gate current $I_{\rm g}$ and such an empirical link between the voltages is not established [5]–[7]. Although the experimental WCC was determined out some time ago, a detailed numerical analysis of the matter is still missing. This is related to lack of a comprehensive model for hot-carrier degradation. At the same time, a predictive diagram reflecting how detrimental these given stress/operating conditions are for the device performance would be of great significance for reliability engineers. Furthermore, representation of such experimental diagrams by an HCD model should serve as a criterion of the model soundness. In this work we apply our physics-based model for hot-carrier degradation [8], [9] in order to represent the experimental color maps depicting the device damage as a function of $\{V_{\rm gs}$,$V_{\rm ds}\}$ in the case of high-voltage n- and p-MOSFETs.

II. Experimental Details

5V n- and p-MOSFETs fabricated on a standard $0.35\mu{\rm m}$ process with a channel length of $0.5\mu{\rm m}$ (the device architectures and the net doping profiles are sketched in Figs. 1,2) have been employed for monitoring the criteria reflecting the severity of HCD. All lateral coordinates x refer to an origin placed at the left edge of the source contact for both devices. Together with a relatively high operation voltage this channel length ensures that the single-electron mechanism of the $\rm Si-H$ bond dissociation is the dominating one [4]. In the case of an n-MOSFET the substrate current as a function of varying $\{V_{\rm ds}, V_{\rm gs}\}$ was recorded and binned onto a color map (Fig. 3). For p-MOSFET we measured $I_{\rm g} = I_{\rm g}(V_{\rm gs}, V_{\rm ds})$, see Fig. 4.

III. The Approach

To analyze the worst-case conditions we employ our physics-based model for hot-carrier degradation which considers the interplay between single- and multiple-carrier modes of Si-H bond dissociation [8], [9]. Note that in [10] we consider also the damage produced by the channel holes. However, we showed that in the case of the channel length of $0.5\,\mu{\rm m}$ the linear drain current degradation is satisfactorily described only by the electron contribution. Both mechanism of Si-H bond-breakage are controlled by the carrier acceleration integral

$$I_{\rm SC/MC} = \nu_{\rm SC/MC} \int\limits_{E_{\rm th}}^{\infty} f(E)g(E)\sigma_{\rm SC/MC}(E)v(E){\rm d}E,$$

which is calculated as the reaction cross section $\sigma_{\rm SC/MC}$ multiplied on the density-of-states $g(E)$ and the carrier velocity $v(E)$, weighted with the carrier energy distribution

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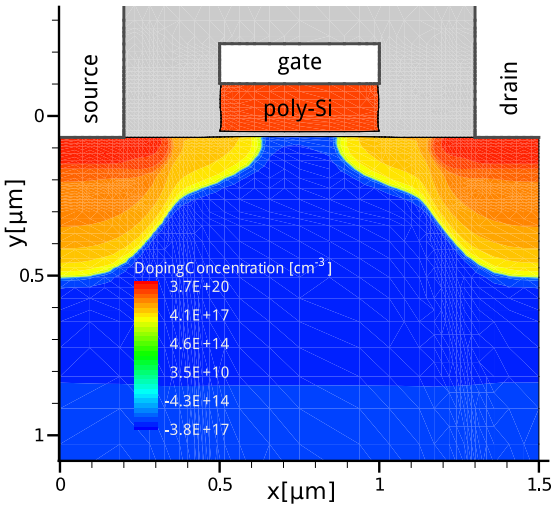

Fig. 1: The topology of 5V n-MOSFET with the net doping profile highlighted.

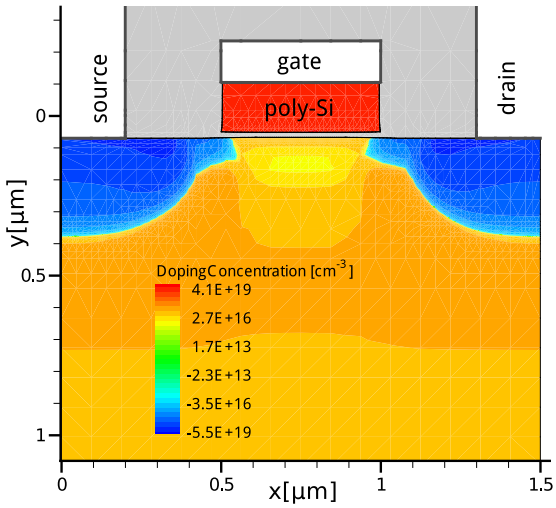

Fig. 2: The topology of 5V p-MOSFET with the net doping profile highlighted.

function (DF) $f(E)$ and integrated over energy starting from the threshold value typical for the bond dissociation reaction.

As we discussed in [8], [11] the dose of damage provided by the MC-component is homogeneously distributed over the lateral coordinate. This is because the prefactor in the MC-induced interface state concentration (see [8], [11]) defined by the acceleration integral is already saturated due to the high concentration of relatively "cold" carriers (represented by the low-energy fragment of the DF). As a result, the non-uniform nature of HCD is related to the single-carrier bond-breakage process with the corresponding contribution to the total interface state density $N_{\rm it}$ localized near the drain end of the gate. Therefore, in order to find the stress conditions corresponding to the worst-case scenario, we suggest to analyze the behavior of the acceleration integral, not considering the interaction between the SC and MC-mechanisms. In literature, one may find other criteria how efficiently carriers interact with the bond, such as the maximum of the electric field, the carrier dynamic temperature, position where the DF demonstrates most extended high-energy tales, etc. However, as we showed in [9], the $N_{\rm it}$ peak just corresponds to the maximum of the AI and is shifted away with respect to maxima of other quantities.

In order to create the numerical picture for the worst-case conditions the following computational procedure was used. As it was shown in [9] just the position of the AI peak defines the maximum of the interface state density ($N_{\rm it}$). Therefore, we use the acceleration integral as a criterion to judge how severe HCD is. In other words, we calculate the AI as a function of $\{V_{\rm gs}$,$V_{\rm ds}\}$ and produce the color maps (see Figs. 5,6) in the same fashion as Figs. 3,4. The computational procedure implies the following steps. Initially, we vary $V_{\rm gs}$ and $V_{\rm ds}$ in the range of 0..6 V and 0..7 (for p-MOSFET the $V_{\rm ds}$ range is of 0..8V) with the step of 0.2 V. For each pair $\{V_{\rm gs}, V_{\rm ds}\}$ we calculate the set of carrier DFs (i.e. at each point along the Si/SiO_2 interface) using a full-band Monte-Carlo device simulator MONJU [12]. This information is then used to calculate the dependences of the carrier acceleration integral vs. the lateral coordinate. After processing these dependencies we have plotted the maximum value of the acceleration integral $I_{\rm SC}$ as a function of $V_{\rm ds}$,$V_{\rm gs}$. Therefore, the whole computational routine contains about 1000 different combinations of stress voltages while each pair $\{V_{\rm gs}, V_{\rm ds}\}$ includes time expensive Monte-Carlo simulations of the carrier DF. These three-dimensional plots (discussed in details in the next Section) have been further compared with the experimental results and analyzed.

IV. Results and Discussion

The comparison between Figs. 3,4 and Figs. 5,6 demonstrates a good agreement between experimental and simulated color maps for both types of transistors. We also plotted the dependence of the gate voltage on the drain bias corresponding to the worst-case conditions, see Figs. 7,8. This data are extracted from Figs. 3,4 where $V_{\rm gs}$ is presented as a function of $V_{\rm ds}$ which is found as the value guaranteeing the maximum of either experimental data ($I_{\rm sub}$ for n-MOSFET and $I_{\rm g}$ for p-MOSFET) or $I_{\rm SC}$ (simulations with our HCD model) for the chosen value of $V_{\rm ds}$. At a drain voltage above 2.0V for the n-MOSFET this dependence follows the law $V_{\rm gs} = 0.4V_{\rm ds}$ typical for this device. Although for the p-MOSFET this dependence is more complicated (Fig. 8), the experimental and simulated pictures are in a good agreement. Finally, the position where the maximum AI is observed, is plotted vs. $\{V_{\rm gs}, V_{\rm ds}\}$, see Figs. 9,10. Since the peak of the acceleration integral determines the location of the most severe degradation spot, this graph can be used to predict where the most degraded section of the device is located. Note that these color maps presented in Figs. 9,10 reflect the pattern shown in Figs. 5,6. For instance, the orange area pronounced in Fig. 5 (and bordered by the right contour curve) corresponds to the light green spot in Fig. 9.

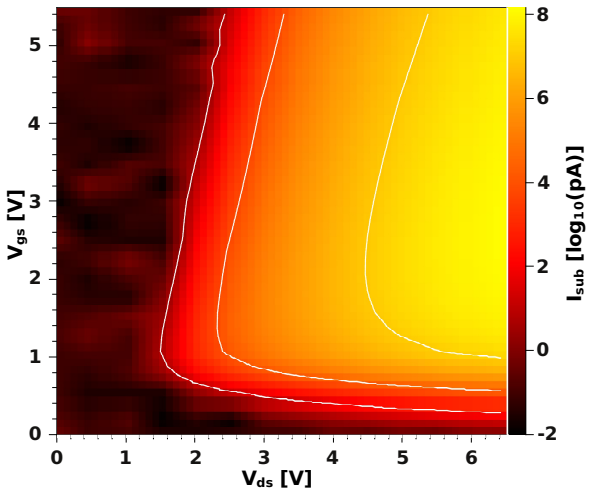

Fig. 3: Experimental I_{sub} as a function of V_{gs} and V_{ds} for the n-MOSFET.

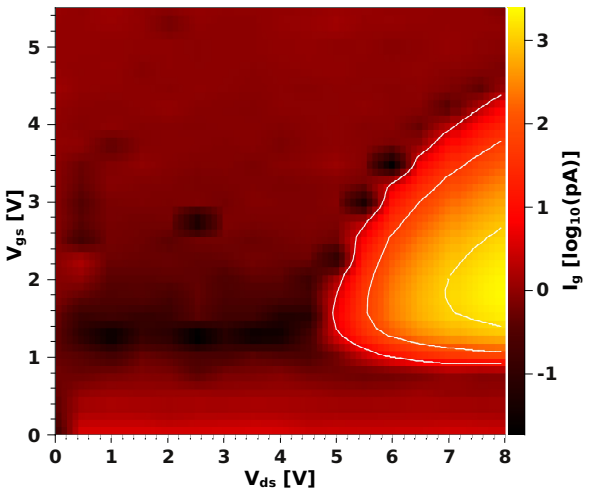

Fig. 4: Experimental I_{g} as a function of V_{ds} and V_{gs} for the p-MOSFET.

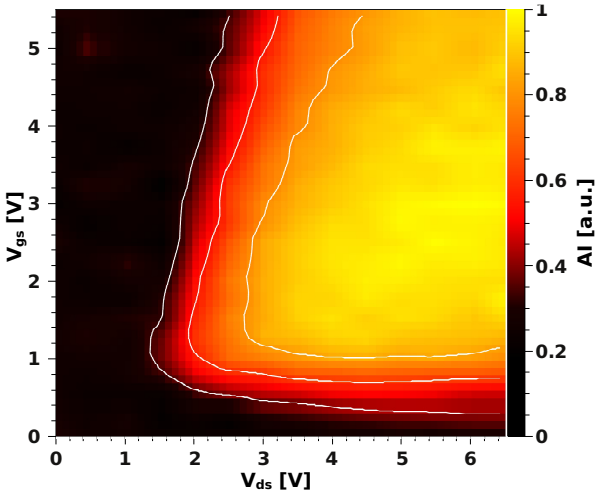

Fig. 5: Maximum value of the AI as a function of V_{gs} and V_{ds} for the n-MOSFET.

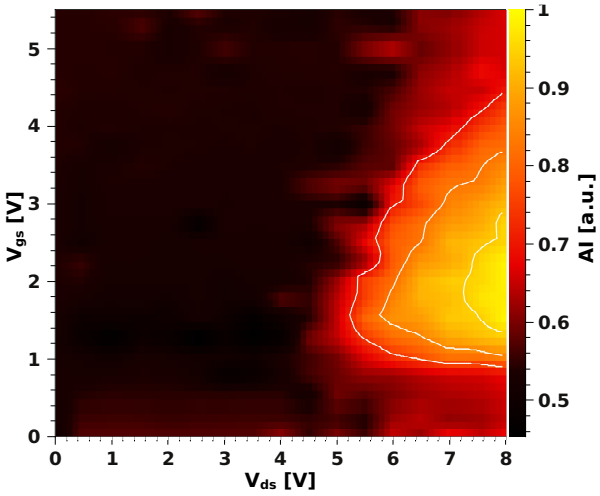

Fig. 6: Maximum value of the AI as a function of V_{gs} and V_{ds} for the p-MOSFET.

V. Conclusion

We have examined the worst-case conditions of hot-carrier degradation in the case of high-voltage n- and p-MOSFETs. For this purpose we employed our HCD model which is based on a thorough treatment of the carrier distribution function obtained using a full-band Monte-Carlo device simulator, i.e. relies on the direct solution of the Boltzmann transport equation. The carrier acceleration integral was used as a criterion of the degradation severity. We have concluded that our model reproduce the WCC with a reasonable accuracy. Simulated diagrams representing the maximum of the AI as a function of gate and drain voltages well agree with the color maps $I_{\mathrm{sub}} = I_{\mathrm{sub}}(V_{\mathrm{gs}}, V_{\mathrm{ds}})$ for n-MOSFET and $I_{\mathrm{g}} = I_{\mathrm{g}}(V_{\mathrm{gs}}, V_{\mathrm{ds}})$ for p-MOSFET. Finally, our HCD model predicts the position where the most degraded device section is localized (i.e. between the drain end of the gate and the drain).

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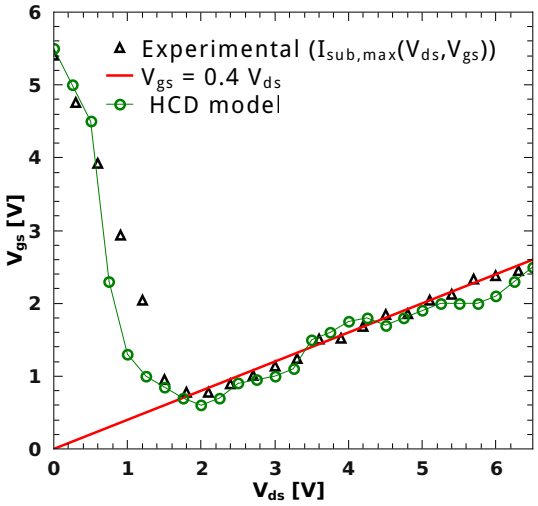

Fig. 7: The interrelation between V_{gs} and V_{ds} corresponding to the WCC (n-MOSFET).

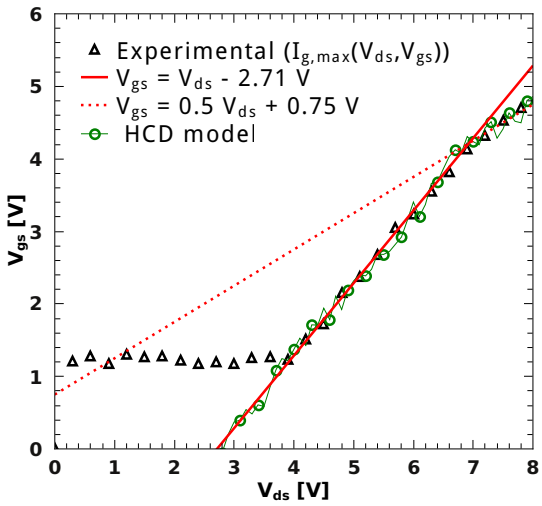

Fig. 8: The interrelation between V_{gs} and V_{ds} corresponding to the WCC (p-MOSFET).

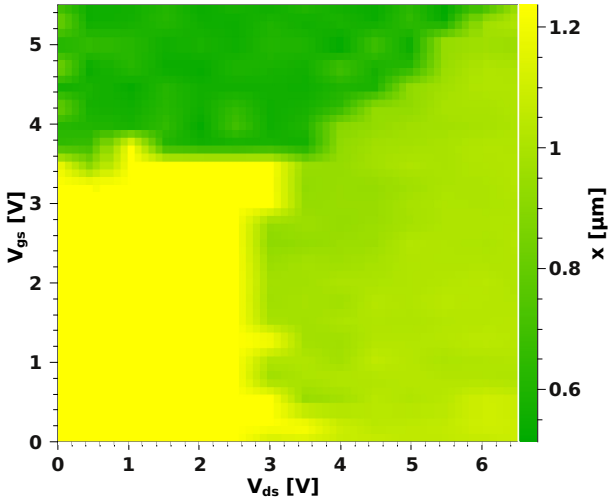

Fig. 9: The position of the maximum AI as a function of V_{gs} and V_{ds} (n-MOSFET).

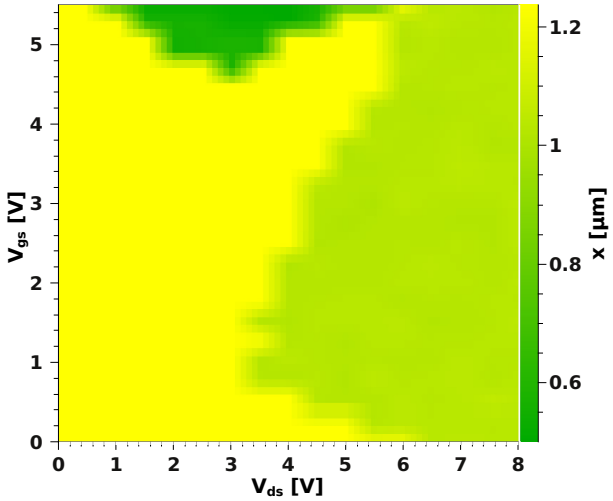

Fig. 10: The position of the maximum AI as a function of V_{gs} and V_{ds} (p-MOSFET).

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