Impact of Quantum Confinement on Stress induced nMOSFET Threshold Voltage Shift

H. Takashino, M. Tanizawa, T. Okagaki, T. Hayashi, M. Taya, H. Ishida, K. Ishikawa, Y. Inoue
Renesas Electronics Corp., 4-1 Mizuhara, Itami, Hyogo 664-0005, Japan
e-mail: hiroyuki.takashino.kx@renesas.com

Abstract

In this paper, we propose a comprehensive model to express nMOSFET threshold voltage shift induced by the stress, ranging from high tensile one to high compressive one. Using this model, the quantum confinement effect is shown to play an important role to cause the threshold voltage shift as large as about 80mV induced by high-film-stress CESL.

Introduction

The process-induced strain has given the big impact of MOSFETs' performance such as the mobility variation [1] and the threshold voltage(Vth) shift [2]. In this paper, the Vth shift($\triangle Vth$) of nMOSFETs is studied because it would largely affect the drive current as well as the off-leak current with the supplied voltage decreasing in low power LSIs.

In order to consider $\triangle Vth$ on TCAD, a simple model which can be easily implemented in DD simulator is proposed for the first time. This model is applied to highly strained Si-nMOSFET with contact etch stop layer(CESL) or shallow trench isolation(STI).

Model

The stress-induced $\triangle Vth$ is basically derived from both the conduction band edge shift($\triangle E_c$) and the valence band edge shift($\triangle E_v$). In nMOSFETs' inversion layer, $\triangle E_v$ is expressed as the well-known formula in bulk Si [3] because hole is not confined, on the other hand, $\triangle E_c$ should be expressed as the formula taking into account the quantum confinement effect.

The Si conduction band consists of six fold valleys. Considering the confinement effect and strain effect, the i-th valley conduction band shift $\triangle E_{c,i}$ is expressed as follows:

$$\begin{aligned} \triangle E_{c,i} &= \triangle E_{qm,i} + D(\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz}) \\ &\quad + U\epsilon_{ii}, \qquad (1) \\ \triangle E_{qm,i} &= C_{qm}(m_0/m_{zz,i})^{1/3}(qF)^{2/3}, \qquad (2) \end{aligned}$$

where ϵ_{ij} is conventional strain tensor, D and U are the deformation potential constants [3, 1]. $\triangle E_{qm,i}$ is the lowest subband energy of i-th valley where C_{qm} is a constant, $m_{zz,i}$ is the confinement mass of the i-th valley, F is the electric field vertical to Si surface [1]. The z-direction is taken as the confinement direction here. The effective conduction band shift $\triangle E_c$ is derived by using $\triangle E_{c,i}$ and $\triangle E_{qm,i}$.

$$\triangle E_c = -\ln \frac{\sum_i \frac{\exp(-\triangle E_{c,i}/k\mathrm{T})}{\sqrt{1-s^2\epsilon_i^2}}}{\sum_i \exp(-\triangle E_{qm,i}/k\mathrm{T})}, \qquad (3)$$

where s is a constant [3, 1], ϵ_i is the shear strain: $\epsilon_{i=x} = \epsilon_{yz}, \epsilon_{i=y} = \epsilon_{zx}, \epsilon_{i=z} = \epsilon_{xy}$.

Fig. 1 and Fig. 2 show the stress dependence of the E_c variation in bulk Si and in the inversion layer of <100> channel direction in (100)-surface orientation where the confinement field F is 0.5MV/cm. The quantum confinement induces the large difference between E_c in bulk and that in the inversion layer especially with out-of-plane stress Szz(Fig.2). Fig.3 also shows that the quantum confinement induces the difference between E_c in bulk and that in the inversion layer of <110> channel direction. The out-of-plane stress Szz dependence of the E_c variation in <110> channel direction is equal to that in <100> channel direction.

$\triangle E_c$ in the arbitrary surface orientation is derived from the eqs.(1-3) by the coordinate transformation of mass matrix and strain tensor to align the confinement direction with the z-direction. Figs.4-6 show the stress dependence of E_c variation in (110)-surface orientation. It is found that the difference between E_c in bulk and

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that in inversion layer is much smaller than the difference in (100)-surface orientation.

The proposed model is applied to nMOSFET structures by the implementation of it in the commercial DD simulator [4].

nMOSFET with STI

nMOSFETs with STI are studied using the present model. STI formed near MOSFETs induces the large compressive stress during a thick gate oxidation, so the stress dependent impurity diffusion in extension and halo region is also considered [6](Fig.7). The stress and dopant profile in 130-nm-node <110> channel nMOSFET in (100)-surface orientation with STI is calculated [5], and the gate length(Lg) dependence of each stress component is shown in Fig.9. The stress Sxx along the channel direction is much larger than Syy and Szz. Fig.10 shows the measured and calculated result of Lg dependence of $\triangle Vth$. We find that the $\triangle Vth$ is mainly determined by the impurity diffusion suppressed by the large STI compressive stress, because even compressive in-plane-stress with the range of GPa causes E_c to be shifted by a few millivolts(Fig.3).

nMOSFET with CESL

Since CESL is deposited after Source/Drain annealing, the stress induced by it doesn't affect the impurity distribution in extension, halo and Source/Drain regions. So the stress-induced Vth shift could be explained only by the proposed model. The structure of 65-nm-node nMOSFET is calculated [5](Fig.8), considering three different kinds of CESL such as 2.4GPa compressive CESL, almost zero stress CESL and 1.7GPa tensile CESL at room temperature, respectively. Fig. 11 shows Lg dependence of the stress component Sxx, Syy and Szz at the channel center on Si surface. The stress Sxx along the channel direction and out-of-plane stress Szz are increasing with Lg decreasing, while Syy is negligible.

The proposed model is applied to (100)-nMOSFETs. The Lg dependence of Vth shift for <100> channel is shown with the measured data in Fig.12, where the $\triangle Vth, comp$ is defined as the difference voltage between Vth with the high-compressive CESL and that with the CESL having small stress, and the $\triangle Vth, tens$ is defined similarly. The $\triangle Vth$ calculated by the conventional model, not taking into account the quantum confinement, is also plotted in Fig.12. It is clear that the present model well represents the measured $\triangle Vth$ while the conventional model underestimates the $\triangle Vth$, especially in the case of the compressive CESL. The present model also exactly represents the measured $\triangle Vth$ for <110> channel.

The proposed model is applied to (110)-nMOSFETs. The Lg dependence of Vth shift for <110> channel is shown in Fig.14, with the measured data. As expected from Fig.5 and Fig.6, the Vth shift is less than 20mV and smaller than that of (100)-nMOSFETs.

Conclusion

The conduction band shift model considering the quantum confinement is proposed to explain nMOSFETs' Vth shift induced by the stress.

We find that, in case of large uniaxial compressive stress along channel direction from neighboring STI, the stress dependent impurity diffusion model almost explains the Vth shift. Meanwhile, in case of the large stress vertical to the Si surface induced by CESL, it is shown that the quantum confinement have to be considered especially in (100)-nMOSFETs and the proposed model is essential to closely reproduce the measurement Lg dependence of the Vth shift.

The proposed model is also applied to (110)-nMOSFETs with CESL and shows that the Vth shift is much smaller than that of (100)-nMOSFETs.

References

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[3] G. L. Bir and G. E. Pikus,"Symmetry and Strain-Induced Effects in Semiconductors," *ed. Wiley, New York*, 1974.

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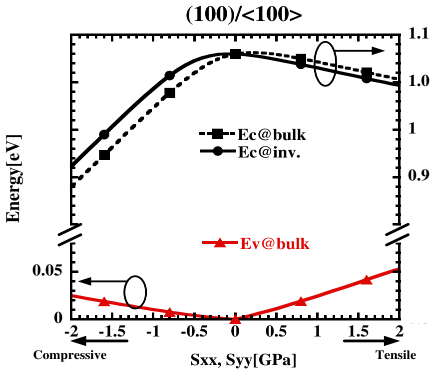

Fig. 1: The in-plane stress $S_{xx,yy}$ dependence of conduction band edge shift in (100)/<100> channel.

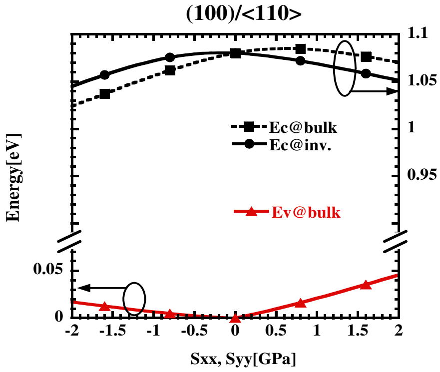

Fig. 3: The in-plane-stress dependence of conduction band edge shift in (100)/<110> channel.

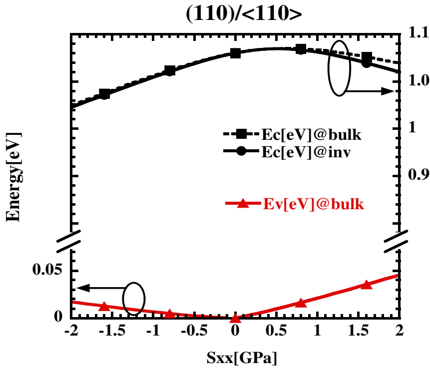

Fig. 5: The in-plane-stress dependence of conduction band edge shift in (110)/<110> channel.

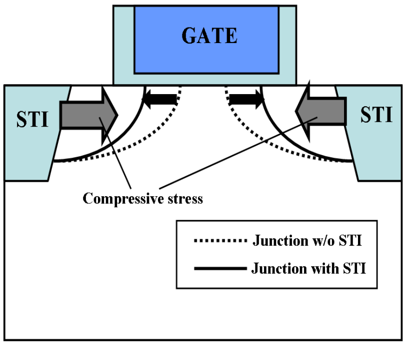

Fig. 7: The schematic structure of nMOSFET with STI. The diffusion in extension region is suppressed with the compressive stress induced by STI and the effective gate length becomes larger.

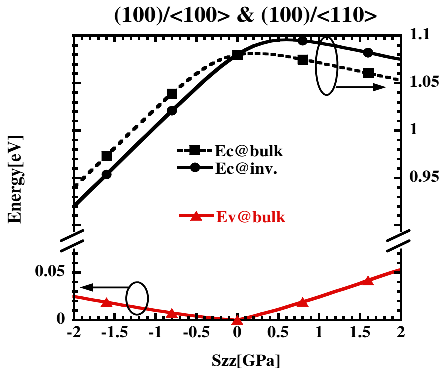

Fig. 2: The out-of-plane stress S_{zz} dependence of conduction band edge shift in (100)/<100> channel.

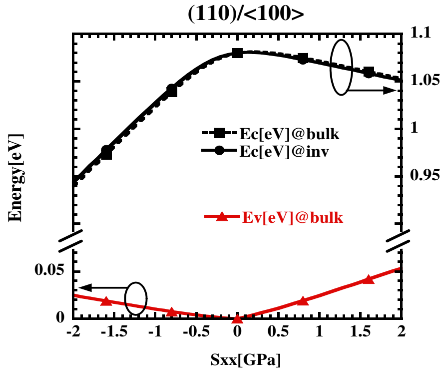

Fig. 4: The in-plane-stress dependence of conduction band edge shift in (110)/<110> channel.

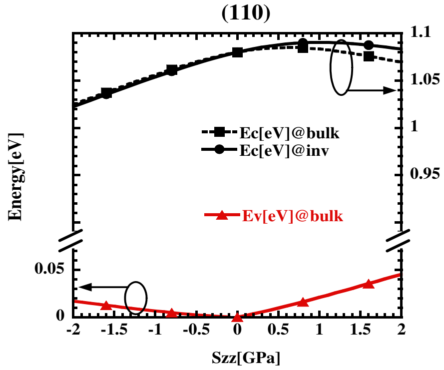

Fig. 6: The out-of-plane stress dependence of conduction band edge shift in (110)/<110> channel.

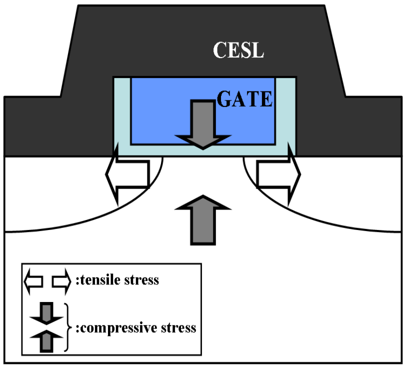

Fig. 8: The schematic structure of nMOSFET with tensile CESL which induces the tensile stress Sxx along the channel as well as the vertical compressive stress Szz.

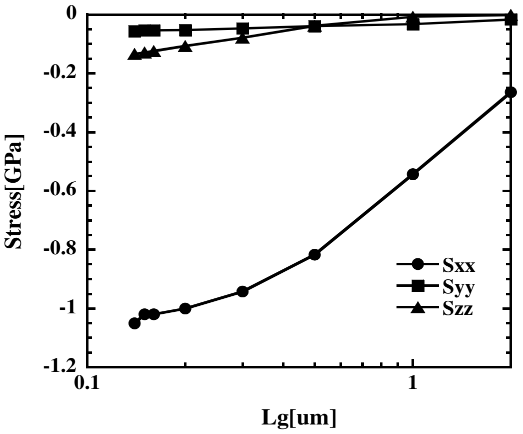

Fig. 9: Lg dependence of the each stress component induced by STI. The stress Sxx along channel is much larger than Syy and Szz.

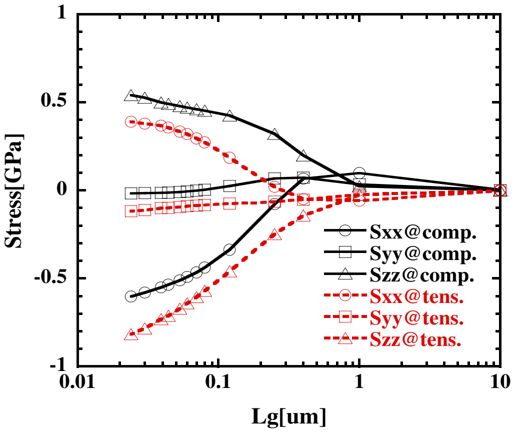

Fig. 11: Lg dependence of the each stress component induced by CESL. Sxx and Szz are large but the sign of them is opposite each other.

(100)/<110>

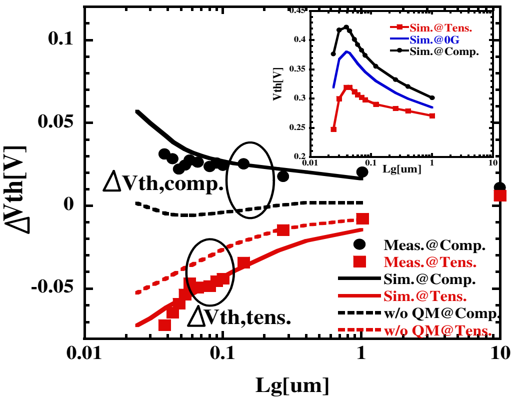

Fig. 13: The measured and calculated result about Lg dependence of $\triangle$Vth in (100)/<110> channel nMOSFET with tensile and compressive CESL. The inset figure is the calculated result about Lg dependence of Vth.

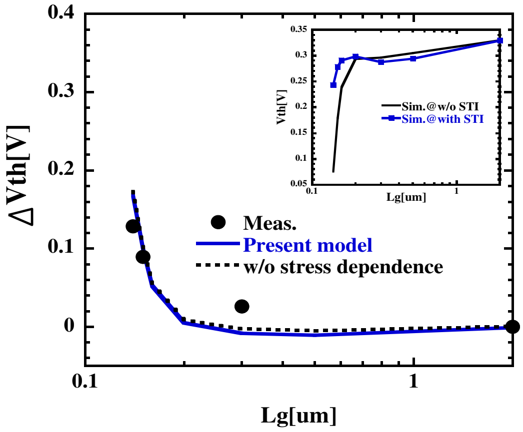

Fig. 10: The measured and calculated result about Lg dependence of $\triangle Vth$ in (100)/<110> channel nMOSFET with STI where $\triangle Vth = Vth,_{\text{STI}} - Vth,_{\text{w/o STI}}$. The inset figure is the calculated result about Lg dependence of Vth.

(100)/<100>

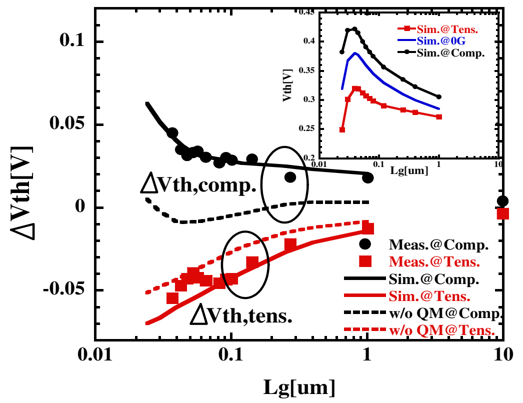

Fig. 12: The measured and calculated result about Lg dependence of $\triangle$Vth in (100)/<100> channel nMOSFET with tensile and compressive CESL. The inset figure is the calculated result about Lg dependence of Vth.

(110)/<110>

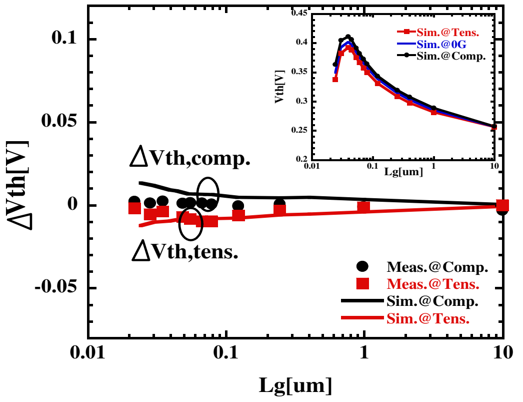

Fig. 14: The measured and calculated result about Lg dependence of $\triangle$Vth in (110)/<110> channel nMOSFET with tensile and compressive CESL. The inset figure is the calculated result about Lg dependence of Vth.