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Impact of Substrate Bias on GIDL for Thin-BOX ETSOI Devices

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***Abstract*— We present a detailed analysis of substrate bias (V_{bb}) impact on gate induced drain leakage (GIDL) for thin-BOX extremely thin silicon-on-insulator (ETSOI) with BOX thickness (T_{BOX}) ranging from 10 to 50 nm and inversion layer thicknesses (T_{INV}) ranging from 1.1 to 1.3 nm. The GIDL behavior for thin-BOX under various substrate biases (V_{bb}) and partially depleted SOI (PDSOI) devices with different body doping are compared.**

Keywords—UTBB; Thin-BOX ETSOI; GIDL; fully depleted; partially depleted; substrate bias; back bias; electric field.

I. INTRODUCTION

Extremely-thin silicon on insulator (ETSOI) devices have been proposed as an attractive option for 14nm low-power technology due to excellent short channel control (SCE), low threshold voltage (V_T) variability as a consequence of undoped body and its compatibility with planar CMOS [1-6]. However, a ETSOI channel in conjunction with a thin buried oxide (BOX) provides an even better SCE by virtue of reducing the electric field coupling between the source and drain junctions. Additionally, V_{bb} in combination with substrate doping can be exploited to affect the front-channel V_T and greatly simplify the gate-stack integration [3]. However, the impact of V_{bb} with different substrate doping on the SCE and its effect on GIDL has not been well understood. In this paper we investigate the GIDL effect in thin-BOX devices as function of V_{bb} and contrast it to that of partially-depleted SOI (PDSOI) devices.

II. SIMULATION SET-UP

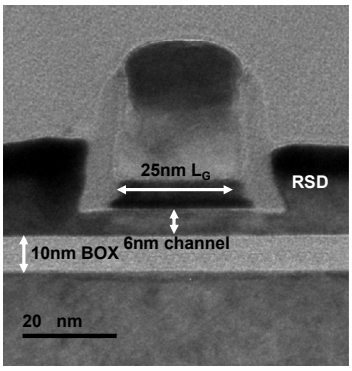

Figure 1. TEM cross-section of 10nm BOX UTBB device with a L_G = 25nm and channel thickness of 6nm used for calibration purposes.

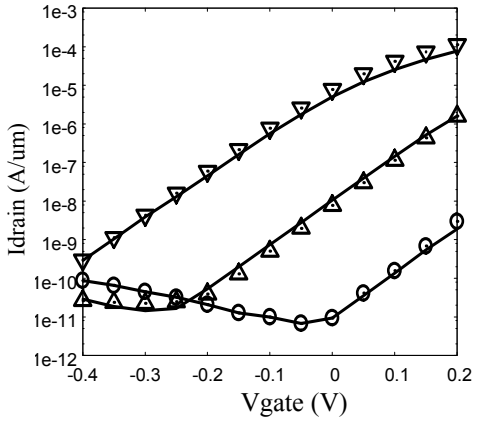

Figure 2. TCAD (symbols) model calibration based on the hardware data (lines) under the assumptions shown in Fig. 1. V_{bb} goes from -2, 0, +2V from left to right.

Two-dimensional Process and device simulation of thin-BOX ETSOI devices with 10nm T_{BOX} and 6nm channel thickness was set up according to the process flow described in [3] using TSUPREM-4 from Synopsys, Inc. and IBM's FIELDAY device simulator [7], respectively. For the purposes of the calibration, the spacer and raised source/drain thicknesses were in accordance with the cross section in Fig.1 using a T_{INV} = 12A. Dopant diffusion and device models were calibrated to match the hardware electrostatics and transport data at different V_{bb} (Fig. 2). To analyze the band-to-band tunneling current (BTBT) HURX model was used for both fully- and partially-depleted devices [8]. Furthermore, to account for high source/drain junction concentration band-gap narrowing model was also included.

III. RESULTS AND DISCUSSION

It has been shown that raising the channel V_T by increasing the body doping in PDSOI and bulk devices leads to higher GIDL. As shown in Fig. 3, the apparent GIDL current has primarily three components: (1) P-N junction leakage at the body/junction interface which gets exacerbated with increasing halo or well doping, (2) drain-side depletion leakage, and (3) gate-leakage. Raising the channel V_T by increasing the body doping reduces the drain-side depletion. However, since the PDSOI and bulk devices have fairly deep SD junctions (>35nm), the BTBT across the reverse-biased p-n junction

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from p-side valence band to n-type conduction band leads to higher junction leakage and therefore degrading GIDL. The PN junction leakage mechanism dominates GIDL current in the PDSOI and bulk devices due to the relatively deep junctions and considerably high body doping (~2-3e18 cm^3).

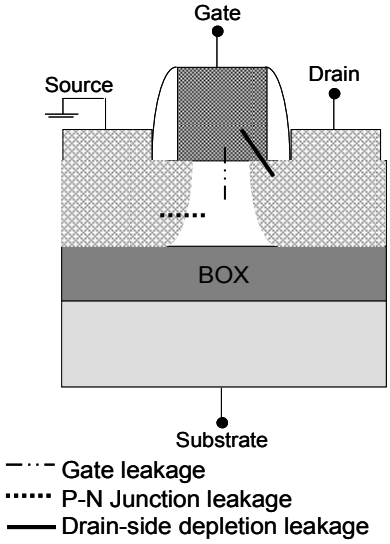

Figure 3. A schematic diagram showing leakage components contributing to GIDL current.

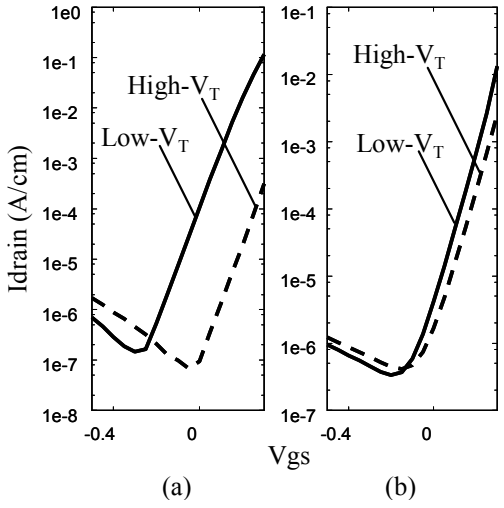

Figure 4. Simulation results showing lower $I_{off,min}$ for thin-BOX ETSOI devices when channel V_T raised by applying V_{bb} (a). When channel V_T raised for PDSOI device by increasing channel doping $I_{off,min}$ increases (b).

Gate leakage is common in all device types; it primarily depends on the material properties and the thickness of gate-stack. The PDSOI and thin-BOX ETSOI devices compared in this paper are at same T_{INV} and hence the magnitude of gate-leakage is assumed to be the same for both device types.

In thin-body devices such as ETSOI or FinFET devices, the PN junction leakage is vanishingly small due to naturally shallow junctions as a result of the thin – typically ≤ 10nm – undoped body. Hence, in ETSOI devices, the drain-side depletion is the dominant GIDL mechanism. Additionally, in the thin-BOX ETSOI NFET devices the front-channel V_T can be raised by doping the substrate P-type and applying a negative bias without changing the extension junctions, body doping, or the front-gate work-function.

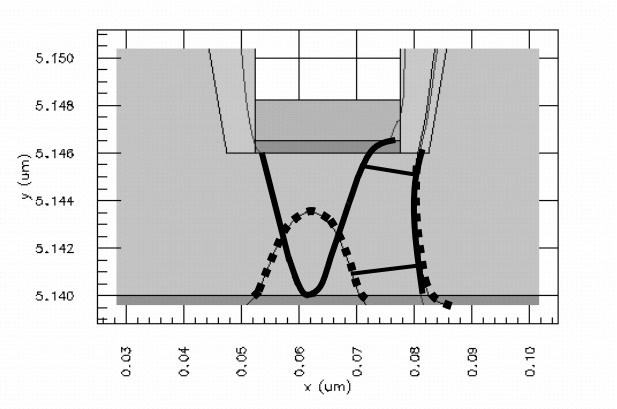

Figure 5. Potential contour lines for a 10nm Thin-BOX ETSOI device with 1V potential difference for V_{bb}=0, V_T= 0.4V (solid lines) and V_{bb} = -2V, V_T= 0.68V (dotted lines) at *constant gate under-drive* (V_T-Vg=0.3V) showing that higher V_T FET has a longer "tunneling distance". V_T for thin-BOX ETSOI device was modulated by back bias.

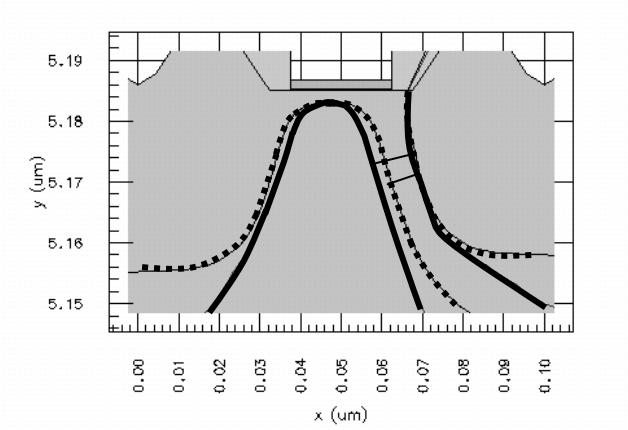

Figure 6. Potential contour lines for a 22nm PDSOI NFET device with 1V potential difference for V_T= 0.30V (solid lines) and V_T= 0.48V (dotted lines) at *constant gate under-drive* (V_T-Vg=0.3V) showing that higher V_T FET has a *shorter* "tunneling distance". V_T was modulated by channel doping.

Figure 4(a) shows the current-voltage characteristics (Id-Vgs curve) for a thin-BOX ETSOI NFET with V_{bb}=0 and -2V having an undoped SOI layer (p-type doping 5e15 cm^{-3}) and an n-type substrate (doping 1e18 cm^{-3}) with T_{BOX} = 10nm. As expected, the channel V_T is raised with the application of V_{bb}=-2V compared to the case where V_{bb}=0V. Correspondingly, Fig. 4(b) shows the Id-Vgs curve for PDSOI with different halo concentrations. Predictably, the channel V_T was found to increase with increasing the halo concentration. The off-state leakages for both these devices were nominally matched. Both the devices have the same L_G and device pitch. The minimum leakage ($I_{off,\ min}$) in PDSOI devices is higher for a high-V_T device in contrast to the thin-BOX ETSOI device wherein the

$I_{off,min}$ can be reduced when increasing the front-gate V_T using negative V_{bb}.

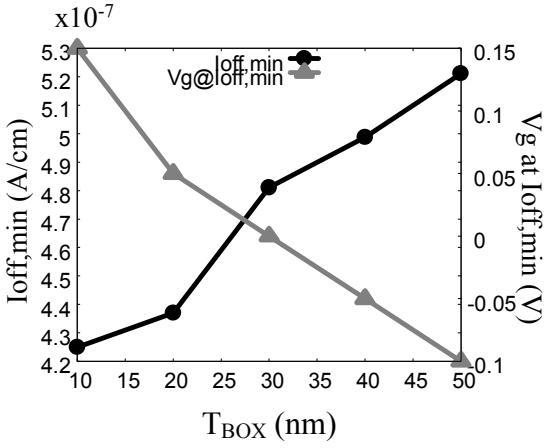

Figure 7. Effect of T_{BOX} on $I_{off,min}$ with V_{bb} = -2V. Note that the Vg at which $I_{off,min}$ occurs is a function of V_T shift and DIBL with V_{bb}.

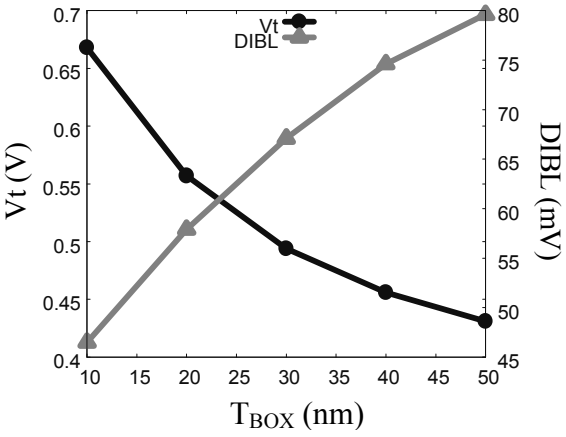

Figure 8. DIBL reduction and simultaneous V_T increase with V_{bb} = -2V for different T_{BOX}.

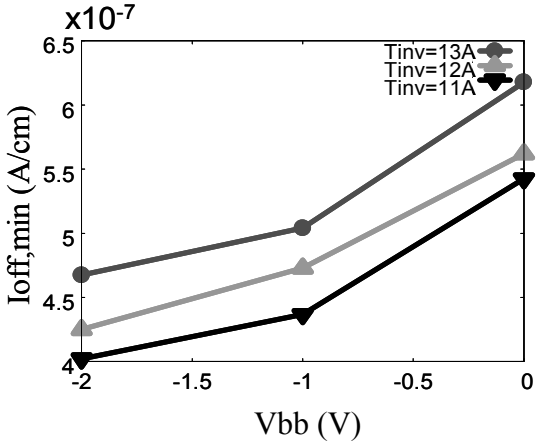

Figure 9. Effect of V_{bb} on $I_{off,min}$ at different T_{INV} for T_{BOX} = 10 nm.

To understand the V_T–I_{offmin} trends in partially- and fully-depleted devices, the electric potential contour lines at a constant gate under-drive of 0.3V were plotted and compared. The potential contour plots are for the devices whose Id-Vgs curves are shown in Fig. 4. Potential contour lines having 1V energy difference are shown. The silicon band-gap is 1.1 eV and shortest distance between potential contours separated by 1V could be assumed to be a good indicator of physical BTBT distance. The BTBT distance in turn is directly correlated to the tunneling/leakage current.

As seen in Fig. 5, in PDSOI the higher $I_{off,min}$ for a high-V_T device is a result of higher electric field (or smaller tunneling distance between the potential contours) which results in a higher BTBT at the PN junction and hence an overall increase in the GIDL current. Conversely, for a high-V_T thin-BOX ETSOI device, wherein the channel V_T is raised by applying negative V_{bb}, the electric field in the drain overlap region is reduced (higher tunneling distance between potential contours) as seen in Fig. 6. Since the PN junction leakage in ETSOI devices is vanishingly small, reduction in drain-side depletion leakage with substrate bias results in overall reduction of GIDL current. These simulation results show that high-V_T devices with low $I_{off,min}$ are possible with thin-BOX ETSOI architecture because of electric field reduction in the drain overlap region at the gate-edge and is consistent with the findings of [6].

Figure 7 shows the $I_{off,min}$ and the Vg at which $I_{off,min}$ occurs for different T_{BOX} at V_{bb}=-2V with the same device dimensions as shown in Fig. 1. The increase in $I_{off,min}$ with increasing TBOX can be explained by voltage drop occurring across the BOX thickness. Correspondingly, the Vg at which the $I_{off,min}$ occurs also reduces as T_{BOX} increases for a constant V_{bb}. This can be explained by the reduction in V_T as a function of T_{BOX} as shown in Fig. 8. Simultaneously, as the V_T of the device reduces with increasing T_{BOX}, the short-channel effect – quantified as drain-induced barrier lowering or DIBL – is found to increase. As the BOX thickness reduces the electric field lines terminate in the substrate and the source to drain electrostatic coupling is reduces. This phenomenon is primarily responsible for reduction of DIBL with reducing T_{BOX} (Fig. 8). Conversely, the V_T of PFET devices decreases and $I_{off,min}$ and DIBL worsen with negative V_{bb}. For such cases, the DIBL and $I_{off,min}$ increase can be mitigated by underlapping the PFET extension junctions. Figure 9 shows the effect of V_{bb} on $I_{off,min}$ for T_{BOX}=10nm as a function of front-gate T_{INV}. As expected, at a given V_{bb} and T_{BOX}, the $I_{off,min}$ reduces with reducing T_{INV}. Furthermore, T_{INV} downscaling can be relaxed in thin-BOX ETSOI devices by applying more negative V_{bb} to achieve the same $I_{off,min}$. This feature is not available to non-planar fully-depleted devices such as the FinFETs.

IV. CONCLUSIONS

The front-channel V_T in fully-depleted thin-BOX ETSOI devices can be raised by appropriate choice of gate workfunction, or increasing body doping, or by applying

appropriate $V_{bb.}$ In this letter, the effect of V_{bb} on SCE and GIDL was investigated. It was found that for NFET devices with negative V_{bb} has an effect of reducing both the GIDL current and DIBL in devices due to the reduction of electric field under the gate and reduced source-drain electrostatic coupling, respectively. These trends are valid for thin-body ETSOI PFET devices with positive V_{bb} but are not discussed here. GIDL reduction with channel-V_T increase for thin-BOX ETSOI devices with negative V_{bb} is contrary to the observations for cases where the channel V_T is increased by increasing channel doping. In PDSOI or bulk devices, typically, the body doping is increased to raise channel-V_T which exacerbates the junction leakage and leads to higher GIDL current due to their much deeper junctions compared to that of thin-body fully-depleted devices. V_T increase with BOX thickness scaling for thin-BOX ETSOI NEFT devices was quantified. Physical factors such T_{BOX}, V_{bb}, and T_{INV} that affect GIDL and DIBL reductions in thin-BOX devices are explored. Due to the unique geometry of thin-BOX ETSOI devices lower $I_{off,min}$ devices without T_{INV} downscaling or junction redesign can be realized.

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