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Analytical model of drain current in nanowire MOSFETs including quantum confinement, band structure effects and quasi-ballistic transport: device to circuit performances analysis

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***Abstract*-- This paper presents an analytical model of the drain current in nanowire MOSFETs (Fig. 1). This architecture is aimed for ultra-scaled devices up to technology nodes sub-11nm and uses silicon films of a few nanometers in thickness. At these dimensions, some emerging physical phenomena can no more be neglected: short-channel effects (SCE) and quasi-ballistic transport (both due to the channel length reduction) and quantum confinement and band structure effects (BSE), due to the strong silicon nanowire thinning. Our analytical model of the drain current includes all these physical phenomena. The proposed model is compared and validated on numerical simulations and experimental data. Finally, a study at the circuit level is performed to assess the impact of BSE and quasi-ballistic transport on the performances of small circuits such as CMOS inverters and ring oscillators based on ultimate nanowire MOSFETs.**

Keywords – **Nanowire MOSFET, modeling, quantum confinement, band structure effect, quasi-ballistic transport.**

I. INTRODUCTION

Due to the exploration of alternative solutions featuring high performances, nanoelectronic devices have evolved towards architectures allowing a much better electrostatics control of the device active region compared to conventional MOSFETs. GAA nanowires MOSFETs, regarding their particular shape, are one of the most promising architectures. This is due to the surface controlled by the surrounding gate which is significantly much higher than for planar devices. With this architecture (now considered as a realistic technology due to recent significant progress of technological processes [1-3]), it is possible to envisage ultra-scaled devices as required by the International Technology Roadmap for Semiconductor (ITRS, [4]). Nanowires are predicted to be relevant for technology nodes below 11nm implying a silicon film of some nanometers in diameter [4]. At these dimensions, several physical phenomena are no more negligible and sensibly impact the transistor behavior, such as quantum short channel effects and quasi-ballistic transport (both due to the channel length reduction) and quantum confinement and band structure effect by thinning the active region film. Indeed, the dimensions targeted for the end-of-roadmap devices are of a few tens atomic layers, which will impact the material properties because the band structure is strongly modified at these ultimate dimensions. In this paper, we will focus especially on this phenomenon by considering the thickness dependence of the silicon bandgap and effective masses but also the modification of the transport regime expected for ultra-short devices. The objective is to provide an analytical model for the drain current in GAA nanowires to bring the physics accuracy of numerical simulations at the circuit level.

In the following, a cylindrical nanowire of diameter D depicted in figure 1 is considered with a low-P-doped (10^{15}cm^{-3}) silicon channel delimited by highly N-doped source and drain regions. The wire is oriented along the [001] silicon lattice direction. A 1 nm-thick oxide and a metal (Al) gate work function are also considered (4.3eV).

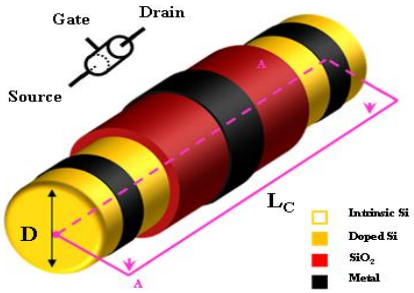

Figure 1. *Schematic of the GAA nanowire architecture and geometrical parameters definition.*

II. THE DRAIN CURRENT MODEL

Our model of drain current is derived from the flux method initiated by McKelvey *et al*. [5]. Later, this concept has been developed by Natori [6] and Lundstrom [7] doing a balance in the active region between the different carriers fluxes at the maximum of the energetic barrier called the "virtual source". All these approaches have been investigated and transposed to 1-D system (1-D electron gas) leading to the following expression of the drain current in the degenerate case:

$$I_D = \pi.D.C_{ox}.(V_{GS}-V_T).\frac{\ln\left(1+e^{\eta_F}\right)}{\Im_{-1/2}(\eta_F)}.v_{th}.\frac{1-R}{1+R}.\frac{1-\dfrac{\ln\left(1+e^{\eta_F-\frac{q.V_{DS}}{k_B.T}}\right)}{\ln\left(1+e^{\eta_F}\right)}}{1+\dfrac{1-R}{1+R}.\dfrac{\Im_{-1/2}\left(\eta_F-\frac{q.V_{DS}}{k_B.T}\right)}{\Im_{-1/2}(\eta_F)}} \quad (1)$$

where V_{GS} is the gate to source voltage, V_T is the threshold voltage, C_{ox} is the oxide capacitance (calculated as in [8]), η_F is the normalized Fermi level, V_{DS} is the drain to source voltage, v_{th} is the thermal velocity, k_B is the Boltzmann constant, q is the electron charge, T is the temperature, $\Im_{-½}$ is the *-1/2* Fermi integral derived analytically from [9] and R is

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the reflexion coefficient which defines the transport regime as exposed in part IV. The ballistic rate refers to the term (1-R)/(1+R).

III. THE ELECTROSTATIC DESCRIPTION

A. The mathematical formalism

The threshold voltage is a parameter essentially dependent on the electrostatic characteristics of the transistor and its capacity to switch from one state to the other one. An analytical expression of this parameter has been found out in [8] based on previous developments [10]:

$$V_T = V_{FB} + \frac{\varepsilon_{Si}}{C_{ox}}.\beta.D + \psi_{s,th} + \phi_F \tag{3}$$

$$\text{with} \quad \beta = \frac{q.N_A}{4\varepsilon_{Si}} + \frac{kT}{q}\frac{C_{ox}}{\varepsilon_{Si}.D} \tag{4}$$

where V_{FB} is the flat-band voltage, ϕ_F is the Fermi potential, N_A is the channel doping, ε_{Si} is the silicon permittivity and $\Psi_{s,th}$ is the surface potential at threshold dependent on the charge of the system. For a 1-D electron gas, the analytical quantum charge is expressed by [11]:

$$Q_{quantum} \approx Q^*.e^{-\frac{q.\psi_S}{kT}} \tag{5}$$

$$\text{with} \quad Q^* = q\sum_j\sum_i\left(\frac{2}{\pi}.\sqrt{\frac{2m_j}{\hbar^2}}\right).\sqrt{\frac{kT}{q}}.\sqrt{\pi}.e^{-\frac{q}{kT}\left(E_j^i+\frac{Eg}{2}\right)} \tag{6}$$

where m_j is the 1-D effective mass in the j^{th} valley, E_g is the silicon bandgap and E^i_j is the i^{th} energy level of the j^{th} valley. In the case of the nanowire, two valleys have to be considered; the longitudinal and the transverse one analytically calculated by the following equations [12]:

$$\begin{aligned} E_t^i &= E_{1,2}^i = \frac{(2\alpha.\hbar.i)^2}{4.q.D^2}.\left(\frac{1}{m_t}+\frac{1}{m_l}\right) \\ E_l^i &= E_3^i = \frac{(2\alpha.\hbar.i)^2}{2.q.D^2}.\frac{1}{m_t} \end{aligned} \tag{7}$$

where α is a numerical parameter fixed to 2.1 to have a perfect agreement with energy levels obtained using a self consistent Schrödinger-Poisson solving. The quantum confinement leads to a strong increase of the threshold voltage when reducing the nanowire diameter [8].

B. Band structure effects (BSE)

As stated previously, a strong reduction of the silicon thickness impacts the material properties by modifying the band structure [13,14]. In [15], atomistic Tight Binding (TB) Schrödinger-Poisson simulations have been performed for the case of [001] oriented silicon in order to highlight the variation of the band structure with the nanowire diameter. The modification of the band shape modifies the band gap and the effective masses of each silicon valley. Under this configuration, the "effective mass" approach is still valid but the values of bulk material cannot be used anymore.

In figure 2, the variation of the silicon band gap and effective masses is plotted with respect to silicon nanowire diameter. Diameter-dependent analytical functions have been found where A_i, B_i and K_i are fitting constants on numerical simulations.

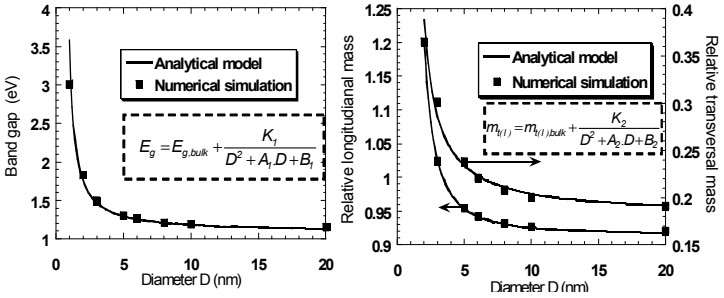

Figure 2. *Variation of the silicon band gap (left) and relative longitudinal and transversal masses (right) with respect to the silicon nanowire diameter. Comparison with atomistic simulations performed in [15].*

These variations impact the quantum confinement (higher masses so lower quantized levels) and the injection velocity [16] when considering BSE. Figure 3 exposes the difference between quantum and classical threshold voltage with and without BSE as a function of the nanowire diameter. A good agreement is shown in figure 3 between the analytical model, numerical simulations [15] and experimental data [3].

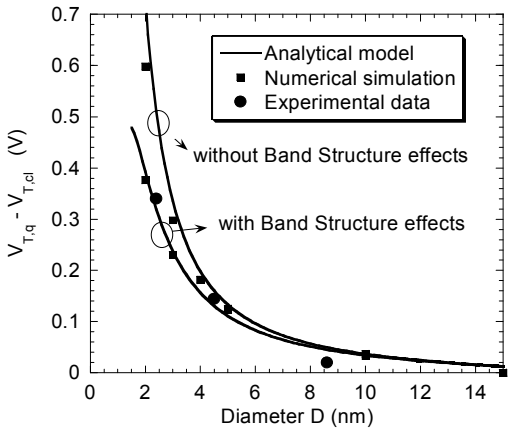

Figure 3. *Difference between quantum ($V_{T,q}$) and classical threshold voltage ($V_{T,cl}$) with and without BSE versus the nanowire diameter for long channel transistors. Comparison between the analytical model, atomistic simulation [15] and experimental data [3].*

IV. THE TRANSPORT REGIME – THE REFLEXION COEFFICIENT

Several previous works focused on the reflexion coefficient [7,17,18]. They all converge toward the concept of "kT-layer" which defines the region where the scattering mechanisms are most limiting for the current. In practice, it represents the portion of the channel length where the potential has decreased by kT/q with respect to the maximum of the energetic barrier. The conventional expression of the reflexion coefficient is:

$$R = \frac{L_{kT}}{\lambda + L_{kT}} \tag{8}$$

where λ is the mean free path.

However, the main problem of these approaches is the continuity between the different working regimes. In this paper, we propose an improved expression based on [5] and inspired from [19] to fix this issue:

$$R = \frac{dfp^{-1}}{\frac{1}{2}.L_{kT}^{-1}.\left(1 + \mathbf{coth}\left(\frac{1}{2}.\frac{L_c}{L_{kT}}\right)\right) + dfp^{-1}} \tag{9}$$

where *dfp* is the dynamical mean free path [20].

A. *The "kT-layer"*

The "kT-layer" model is based on the empirical approach of the power initiated by [7]. Its expression is:

$$L_{kT} = L_C \cdot \left(\frac{k_B T}{q.V_{DS}} \right)^{1/\alpha} \quad (10)$$

The parameter α is extracted from TCAD simulations [21]. Figure 4-a) shows the "kT-layer" versus the channel length for different dfp.

We can note that, as expected, when increasing the number of interactions (lowering dfp), the potential drop of the energetic barrier also increases (lower "kT-layer"). Finally, the analytical expression of the power α is:

$$\alpha = 1.9 + \left(\frac{dfp}{L_C} \right)^{0.7} \cdot \frac{1.7}{1 + e^{-\frac{L_C - 2.D}{D}}} \quad (11)$$

Figure 4-b) shows the reflexion coefficient and the ballistic rate with respect to the dfp. Results have been compared to a deterministic Wigner solver [3]. So, depending on the value of the dfp, the current will be impacted through the reflexion coefficient.

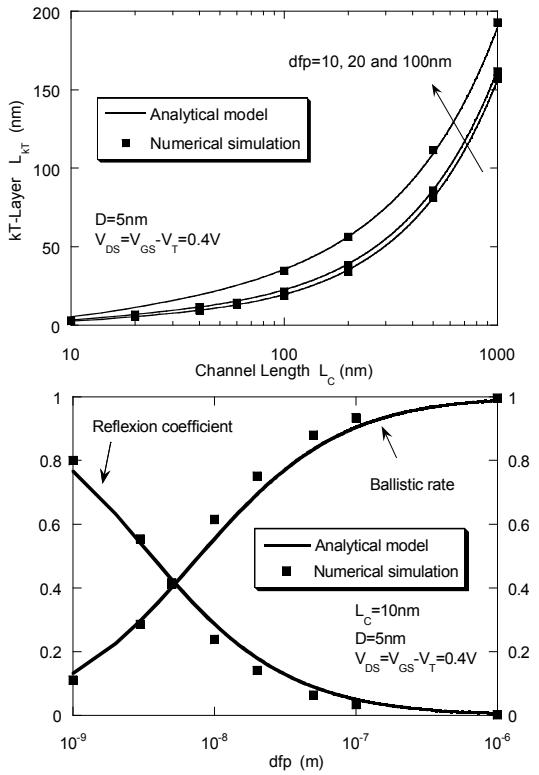

Figure 4. a) *Validation of the L_{kT} model for different dfp vs. the channel length. Comparison with numerical TCAD simulations [21].* b) *Reflexion coefficient and ballistic rate function of the dfp. Comparison with numerical simulations obtained with a deterministic Wigner equation solver [22].*

B. *The dynamical mean free path*

The dynamical mean free path is directly proportional to the mobility of carriers in the silicon film.

$$dfp = \frac{2.k_B.T}{q.v_{inj}} . \mu_{tot} \quad (12)$$

where v_{inj} is the injection velocity and μ_{tot} is the total mobility, which includes all the scattering mechanisms (phonons *ph*, surface roughness *sr* and remote coulomb scattering *rcs*) by using the Matthiessen law:

$$\mu_{tot}^{-1} = \mu_{ph}^{-1} + \mu_{sr}^{-1} + \mu_{rcs}^{-1}$$

$$= \left(\frac{\mu_{0,ph}}{(E_{eff})^{\theta_{ph}}} \right)^{-1} + \left(\frac{\mu_{0,sr}}{(E_{eff})^{\theta_{sr}}} \right)^{-1} + \left(\frac{\mu_{0,rcs}}{\left(E_{eff} / q.N_{fix} \right)^{\theta_{rcs}}} \right)^{-1} \quad (13)$$

where E_{eff} is the effective field, N_{fix} is the charge trapped in the gate oxide, μ_0 is the low-filed mobility and θ is the field-dependence.

Figure 5 shows the experimental dfp and the analytical model versus the inversion charge for a 15nm-thick nanowire.

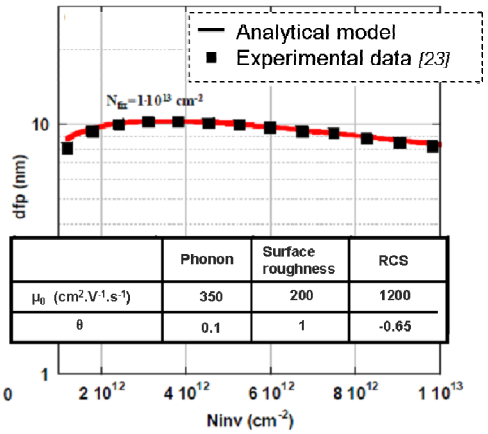

Figure 5. *dfp vs. inversion charge density (N_{inv}) for $Ti N/HfO_2$=3nm/SiO_2=2nm gate stack. Comparison with experimental data [23]; the model includes Remote Coulomb Scattering (RCS), phonon and surface roughness scattering.*

Figure 6 shows the result at the device level; this figure plots the quasi-ballistic drain current (using the experimental dfp) with respect to the gate voltage with and without BSE. A comparison between the model and simulation data obtained using deterministic Wigner solver has also been performed with a good agreement.

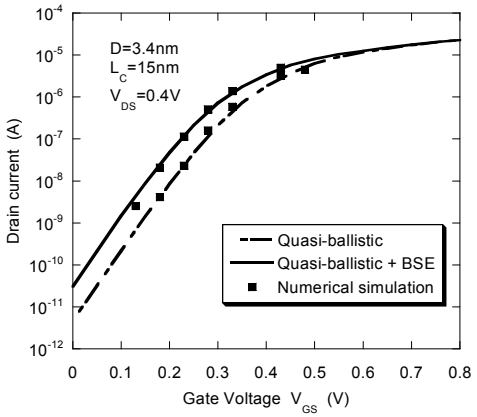

Figure 6. *Drain current versus V_{GS} for D=3.4nm and L_c=15nm for quasi-ballistic and quasi-ballistic with band structure effect. Comparison with numerical simulations obtained with deterministic Wigner equation solver [3].*

V. RING OSCILLATOR SIMULATION

After implementation in a Verilog-A environment, the model presented above has been used to simulate a CMOS inverter and then a complete 11 stages-ring oscillator. In

order to build-up the CMOS inverter a p-type nanowire MOSFET is considered symmetrically to the n-type transistor in the inverter setup.

Figure 7 shows the input/output characteristics of the inverter for the ballistic (R=0), quasi-ballistic (experimental dfp) and quasi-ballistic with BSE case. We can note that the inverter characteristic is not really sensitive to the transport regime. Only BSE impacts the inverter switch. This is coherent with the theory because the inverter operation essentially depends on the electrostatics behavior of individual transistors.

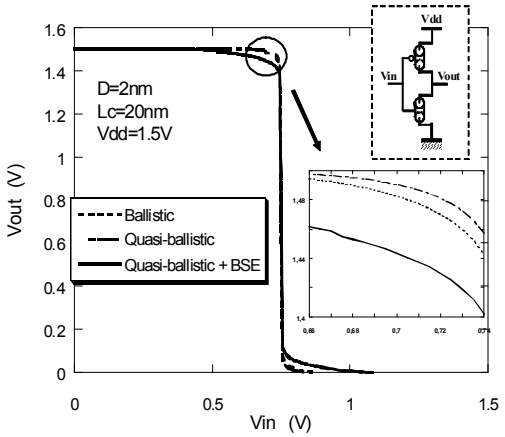

Figure 7. *V_{out} vs V_{in} of CMOS inverter based on nanowire MOSFETs; comparison between ballistic (R=0), quasi-ballistic transport (using experimental dfp) and quasi-ballistic transport with BSE.*

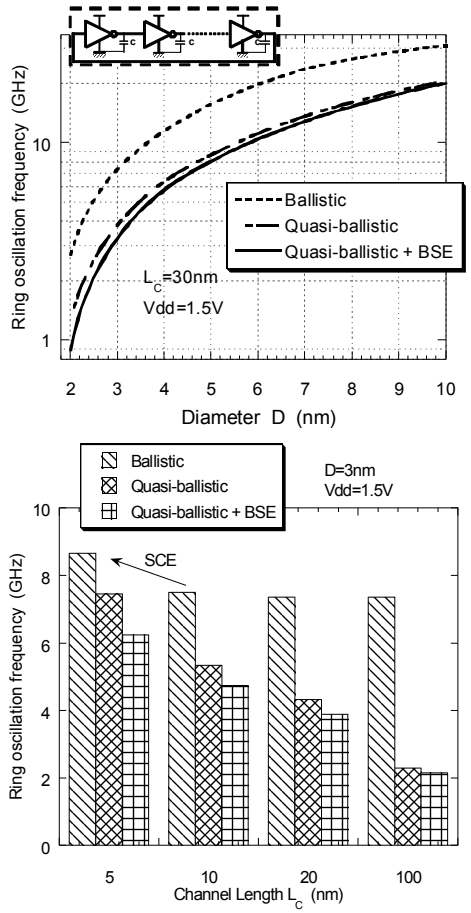

Figure 8. *Oscillation frequency of an 11-stages ring oscillator: (a) versus the nanowire diameter for L_C=30nm and Vdd=1.5V; (b) versus the channel length for D=3nm and Vdd=1.5V. Comparison between ballistic transport (R=0), quasi-ballistic transport (using experimental dfp) and quasi-ballistic transport with BSE. The value of the ring charge capacitance is 1fF.*

Figure 8 shows the oscillation frequency of an 11-stages ring oscillator. Figure 8.a shows the impact of the nanowire diameter: the oscillation frequency is directly proportional to the ON-state current of the nanowire MOSFET, and then, reducing the nanowire diameter decreases the oscillation frequency. This effect is enhanced by BSE which, as stated before, reduces the injection velocity. Figure 8.b highlights the strong impact of the quasi-ballistic transport on the ring performances. Reducing the channel length increases the oscillation frequency in the quasi-ballistic case which becomes closer to that obtained for the theoretical case of a pure ballistic transport.

VI. CONCLUSION

A complete analytical description of quasi-ballistic current has been derived for GAA nanowire MOSFETs including band structure effects. A study of the impact of the transport regime and BSE has been performed on both device and circuit performances. The increase of the band gap and effective masses when thinning the nanowire diameter below 5 nm has been considered in our model based on analytical expressions calibrated on numerical tight-binding simulations. This band structure modification leads to a reduced effect of the quantum confinement on the threshold voltage and to a reduction of the injection velocity. Regarding the transport, we have seen that the reflexion coefficient depends on the channel length. At the circuit level, the inverter switch is less abrupt when BSE is taken into account due to the electrostatics modification. The ring oscillator performances are affected by scattering and BSE by reducing the oscillation frequency.

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