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Correlation between Interface Traps and Random Dopants in Emerging MOSFETs

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***Abstract*—In this work, we for the first time study the fluctuation and interaction between interface traps (ITs) and random dopants (RDs) of 16 nm MOSFETs. Totally random devices with 2D ITs at Si/high-κ oxide interface and 3D RDs inside channel are simultaneously examined using an experimentally validated 3D device simulation. Pure random ITs at Si/high-κ oxide interface will increase the threshold voltage (V_{th}) due to enlarge potential barrier resulting from accept-like ITs. However, the fluctuation of V_{th} (σV_{th}) induced by ITs is smaller than the result of RDs. Considering the effect of ITs and RDs at the same time will result in coupled localized spikes of potential barrier and induced characteristics are much more correlated to each other which can not be estimated using adiabatic statistical sum calculation. Consequently, the effect of random ITs and RDs on device variability should be counted simultaneously for high-κ / metal gate devices.**

Keywords-hig-κ/metal gate; interface trap; random dopant; threshold voltage fluctuation; interaction; 3D device simulation; effective oxide thickness; potential barrier.

I. INTRODUCTION

The RD-induced threshold voltage fluctuation (σV_{th}) up to 40 mV for 20 nm planar MOSFET was experimentally quantified [1]. RD fluctuation (RDF) [1-6] has been one of challenges in device scaling; recently, high-κ/metal gate (HKMG) technology was adopted to reduce intrinsic parameter fluctuation and leakage current for sub-45 nm generations [7-22]. However, random ITs appearing at Si/high-κ oxide interface may introduce a new fluctuation source for device degradation [23-28]. Unfortunately, the interaction and effect of ITs and RDs on characteristic fluctuation have not been fully explored yet.

In this work, we estimate the fluctuation and interaction of random ITs and RDs of 16 nm MOSFETs using an experimentally calibrated 3D device simulation [1,10,28]. Completely random ITs, RDs, and "ITs&RDs" (i.e., 3D device simulation with including random ITs and RDs at the same time) are generated and simulated to assess the variability of I_{on}/I_{off} and σV_{th} for device with respect to various high-κ oxides. This paper is organized as follows. In Sec. II, we brief the simulation for device with RDs and ITs. In Sec. III, the σV_{th} calculated by 3D simulation with RDs, ITs, "ITs&RDs" and statistical sum of $\sigma V_{th,RDs}$ and $\sigma V_{th,ITs}$ with different EOT are investigated, respectively. Further, the interaction between RDs and ITs is explored. Finally, conclusions are drawn.

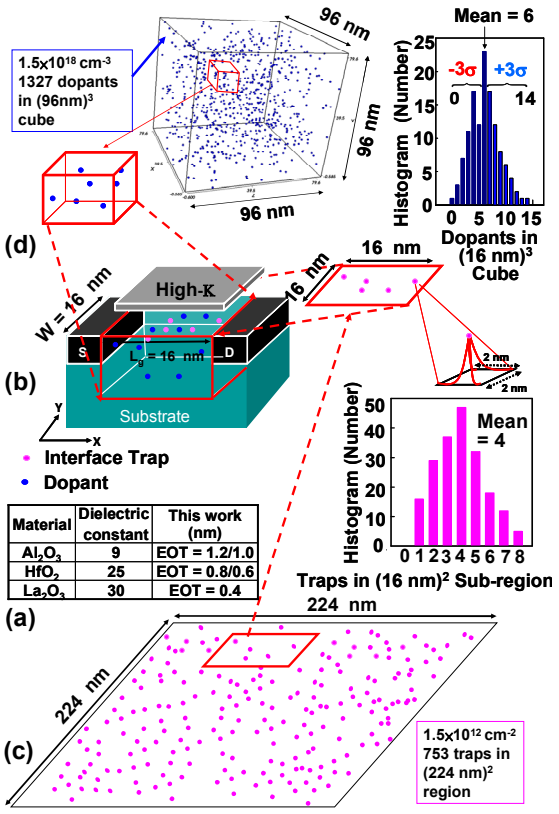

Figure 1. (a) The studied high dielectric constant gate insulators with the corresponding EOT. (b) The source of randomness (pink dots are interface traps and blue dots are discrete dopants) and simulation settings for fluctuations of random ITs and RDs. (c) We first generate 753 acceptor-like traps in a large plane, where the trap's concentration in the plane is around 1.5 x 10^{12} cm^{-2} and the number follows the Poisson distribution. The energy of each trap on the plane is assigned according to distribution of trap's density. Then the entire plane is partitioned into sub-planes (size: 16 nm x 16 nm), where the number of traps in all sub-planes may vary from 0 to 8 and the average number is 4. (d) Discrete dopants randomly distributed in $(96\ nm)^3$ cube with the average concentration of 1.5 x 10^{18} cm^{-3}. There will be 1327 dopants within the cube and dopants vary from 0 to 14 (the average number is 6) for all 216 sub-cubes. The size of each sub-cube is $(16\ nm)^3$. The total sub-cubes and sub-planes are then mapped into device's 3D channel and 2D surface for RDs and ITs' position/number-sensitive simulation (b).

II. THE "ITS&RDS" SIMULATION METHODOLOGY

We first calibrate the nominal characteristic of the studied HKMG device according to ITRS Roadmap in low operating power application [1]. The high dielectric constant gate insulators and approximated EOT are listed in Fig. 1(a). The

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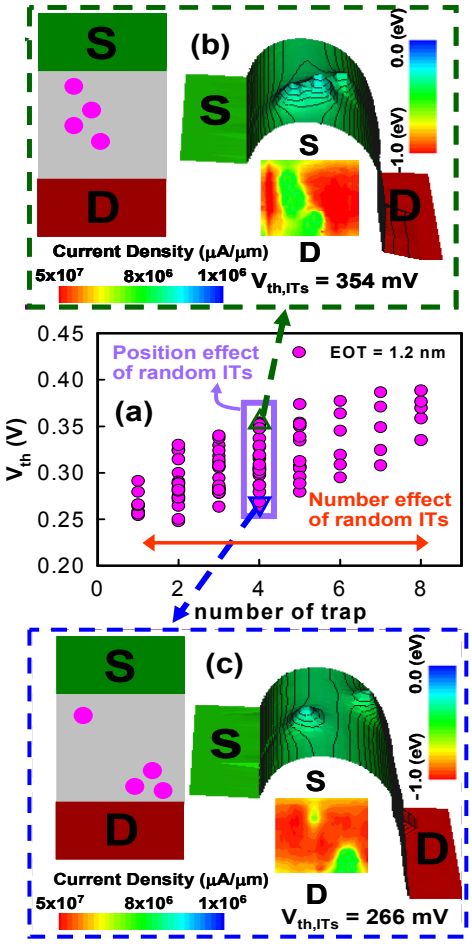

Figure 2. The $V_{th,ITs}$ as a function of traps' number of the N-MOSFET device with Al_2O_3 oxide (EOT = 1.2 nm is used). The random position effect of ITs induces rather different fluctuation in spite of the same number of traps, as marked in inset of (a). The off-state potential and the on-state current density of (b) high and (c) low V_{th}, respectively, despite the same number of traps (4 ITs at Si/Al_2O_3 oxide interface).

devices we examined are the 16 nm N-MOSFETs (width: 16 nm) with amorphous-based TiN/HfO_2 gate stacks, as shown in Fig. 1(b); P-MOSFETs are also studied. For the simulation of IT fluctuation (ITF), we first generate 753 acceptor-like traps (pink dots) in a large 2D plane as shown in Fig. 1(c), where the trap's concentration in the plane is around $1.5x10^{12}$ cm^{-2} based on experimental characterization, and the total number of traps follows the Poisson distribution. Then, the whole plane (with the statistically generated random ITs) is partitioned into many sub-planes, where the number of traps in each sub-plane (area: 16 nm x 16 nm) may vary from 1 to 8 and the average is 4. Energy of each IT is assigned according to the distribution of trap's density [24, 27-28]. We test the density of ITs varying from $5x10^{11}$ to $5x10^{12}$ cm^{-2}. The procedure above is repeated until all sub-regions are assigned at Si/HfO_2 interface. We do apply the similar way for other high-κ insulators. Notably the approach enables us to examine ITs' influence concurrently capturing the random traps' position and number effects over 2D interface. Second, for the 3D device simulation of RDF (blue dots), we follow the method in [1,10,28], as shown in Fig. 1(d). For the 3D device simulation with "ITs&RDs", we include random ITs and RDs in the settings at the same time.

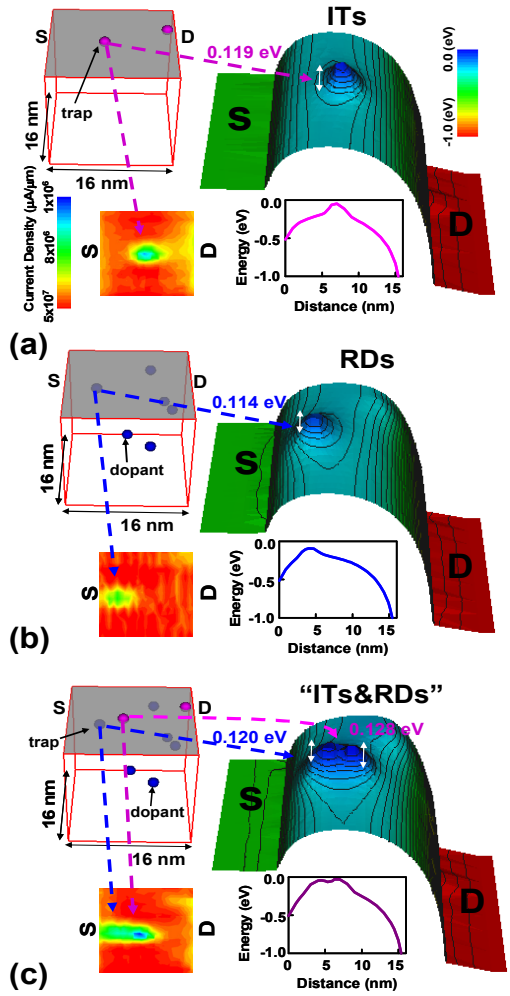

Figure 3. The on-state (V_G =V_D = 0.8 V) current density and the off-state (V_G = 0 V and V_D = 0.8 V) potential distribution of the channel surface from one of simulated transistors, where EOT = 0.8 nm. The device fluctuated by (a) 2 random ITs at Si/HfO_2 oxide interface, (b) 6 RDs locating inside the silicon channel below the channel surface, and (c) 8 random "ITs&RDs" simultaneously. The fluctuated potentials measuring from the source (S) to drain (D) are shown in inset.

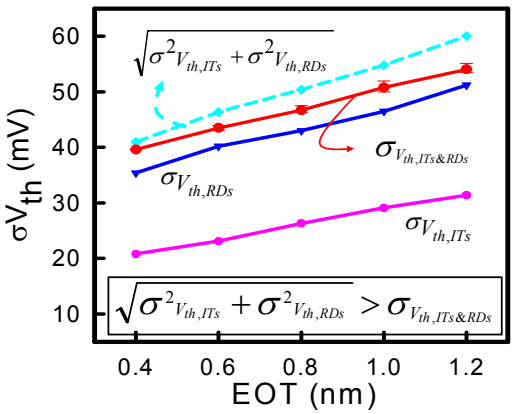

Figure 4. The σV_{th} as a function of EOT with different fluctuation sources: ITs only (pink line), RDs only (blue line) and 3D simulation with considering ITs and RDs simultaneously (i.e., "ITs&RDs" in the red line). Owing to gate capacitance variation and interaction of surface potentials resulting from ITs and RDs, the $\sigma V_{th,ITs\&RDs}$ is smaller than the result of adiabatic statistical sum calculation via $(\sigma^2 V_{th,ITs}+\sigma^2 V_{th,RDs})^{0.5}$.

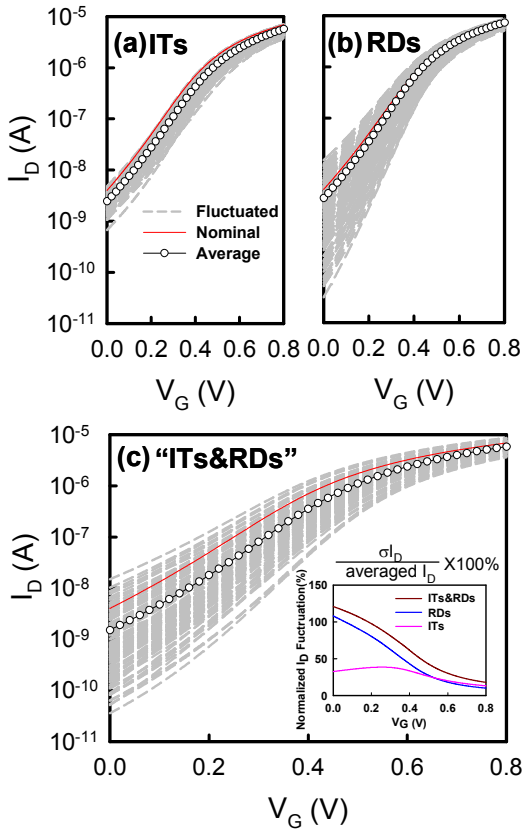

Figure 5. The fluctuated I_D-V_G curves with respect to (a) the ITs only, (b) the RDs only and (c) the "ITs&RDs", respectively. The EOT of studied device is equal to 0.8 nm. The red line is the nominal data, the open-circle line is the average I_D-V_G and the grey dash line is the fluctuated I_D-V_G curves. The inset of (c) shows the normalized I_D fluctuation versus V_G. The normalized I_D fluctuation is dominated by RDs in the subthreshold regions and by ITs in the saturation region.

III. Results and Discussion

Notably, not only RDs [1-6], but also the random ITs exhibit interesting random position and number effects on device's physical characteristics. The random position effect of ITs induces rather different fluctuation in spite of the same number of traps. As marked in inset of Fig. 2(a), those different devices (EOT = 1.2 nm) are with the same 4 ITs, but they have different V_{th}. The random ITs result in distinct high and low threshold voltages, as shown in Figs. 2(b) and 2(c), respectively, despite the same number of traps. Compared with the off-state potential in Fig. 2(c), the large number of ITs near source side resulting in relatively higher barrier has higher V_{th} for potential profile shown in Fig. 2(b). The random ITs do not only twist off-state potential but also alter the on-state current flow. As shown in Figs. 2(b) and 2(c), the conducting path of the on-state current is restricted to some extent by different locations of ITs. For the random ITs' number effect, the devices with the same value of V_{th} have different number of ITs, as shown in Fig. 2(a). Note all values of fluctuated V_{th} are almost larger than the nominal case owing to accept-like ITs in the N-MOSFETs.

Selecting from one of simulated transistors (total transistors: 216), Figs. 3(a)-3(c) show the off-state (EOT = 0.8 nm, V_G = 0 V and V_D = 0.8 V) potential distributions and the on-state (V_G = V_D = 0.8 V) current densities for the device with three different fluctuation settings: the ITs only, the RDs only, and the "ITs&RDs", respectively. The surface potential fluctuated by the random ITs (pink traps), as shown in the right plot of Fig. 3(a), results in a spike of 0.119 eV. Inside the silicon channel (just below the channel surface), RDs (blue dopants) induced potential distribution is shown in Fig. 3(b), where the peak of barrier is 0.114 eV. In Fig. 3(c), the 3D simulation with random "ITs&RDs" possesses rather different potential profile and current density. The potential has an enlarged peak of localized spikes. The potential profile has about 7.6% enhancement, where the calculations of barrier's peak are 0.128 eV and 0.12 eV for ITs and RDs, respectively. Cutting from the source (S) to drain (D), the 1D shapes of potential passing through the peaks of spike are shown in inset of Fig. 3, with respect to the aforementioned three cases. Note the range of localized spikes in Fig. 3(c) is broadened due to potential's interaction resulting from the "ITs&RDs". Consequently, the whirlpool-like on-state current density spreads apart from S to D, as shown in Fig. 3(c).

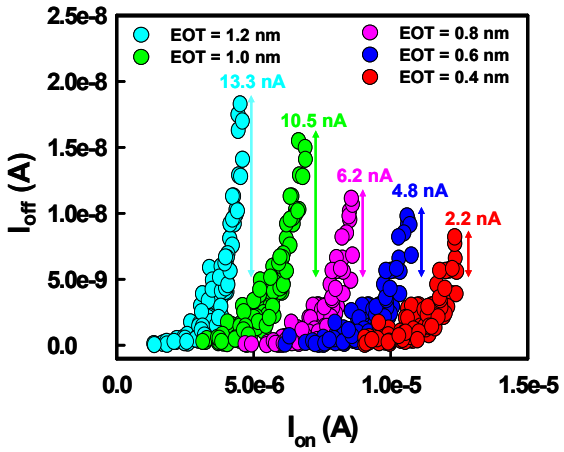

Figure 6. The I_{on}-I_{off} characteristics induced by the random "ITs&RDs" of simulated transistors with EOT = 0.4, 0.6, 0.8, 1.0 and 1.2 nm, respectively.

According to the observations above, the random ITs- and/or RDs-induced σV_{th} as a function of EOT for all simulated samples with different EOTs is shown in Fig. 4, respectively. According to statistical identity for two random variables $V_{th,ITs}$ and $V_{th,RDs}$ with identical independent distributions, our results indicate that $\sigma V_{th,ITs\&RDs} < (\sigma^2 V_{th,ITs} + \sigma^2 V_{th,RDs})^{0.5}$ holds for all EOTs because the interaction between ITs and RDs does not vanish. For example, $\sigma V_{th,ITs\&RDs}$ = 53 mV and $(\sigma^2 V_{th,ITs} + \sigma^2 V_{th,RDs})^{0.5}$ = 60 mV for device with EOT = 1.2 nm.

Fig. 5 shows the fluctuated I_D-V_G curves with respect to the ITs only, the RDs only and the "ITs&RDs", respectively. The simulation is with a 0.8-nm EOT of studied devices. As shown in Fgi. 5(a), the red line is the nominal data, the open-circle line is the average I_D-V_G and the grey dash line is the fluctuated I_D-V_G curves. Pure random ITs at Si/high-κ oxide interface increase V_{th} and degrade the drain current resulting from accept-like ITs. However, the fluctuation of I_D-V_G induced by ITs is smaller than the result of RDs due to moderate ITs' density, as shown in Fig. 5(b). The inset of Fig. 5(c) shows the normalized I_D fluctuation versus V_G. The

normalized I_D fluctuation is dominated by RDs in the subthreshold regions and by ITs in the saturation region. The fluctuated I_{on}-I_{off} characteristic induced by the random "ITs&RDs" of simulated transistors with different EOT, as shown in Fig. 6, indicates the maximum difference of I_{off} is reduced approximately from 13.3 nA to 2.2 nA as the EOT is scaled from 1.2 nm to 0.4 nm. (I_{off} drops by 6 times if EOT is reduced by 3 times). Not shown in here, we also estimate the interaction for P-MOSFETs, $\sigma V_{th,ITs\&RDs}$ = 45 mV which is smaller than the adiabatic statistical sum calculation $(\sigma^2 V_{th,ITs} + \sigma^2 V_{th,RDs})^{0.5}$ = 49 mV for EOT = 0.8 nm.

IV. CONCLUSIONS

In this study, we have examined the DC characteristic fluctuation and interaction between ITs and RDs for 16 nm devices with different high-κ oxides. The "ITs&RDs" has an enlarged peak of localized spikes, compared with results of individual ITs and RDs, respectively. Consequently, the inequality $\sigma V_{th,ITs\&RDs} < (\sigma^2 V_{th,ITs} + \sigma^2 V_{th,RDs})^{0.5}$ holds for HKMG N- and P-MOSFET devices. The effect of random ITs and RDs on device variability should be counted simultaneously for high-κ / metal gate devices. We are currently experimentally extracting the concentration of random ITs with fabricated nano-CMOS devices.

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