Nanosized Metal Grains Induced Electrical Characteristic Fluctuation in 16 nm Bulk and SOI FinFET Devices with TiN/HfO_2 Gate Stack

Hui-Wen Cheng[1], Yiming Li[1,2,*], Chun-Yen Yiu[1], and Hsin-Wen Su[2]
[1]Institute of Communications Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[2]Department of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[*]Corresponding author. Email: ymli@faculty.nctu.edu.tw

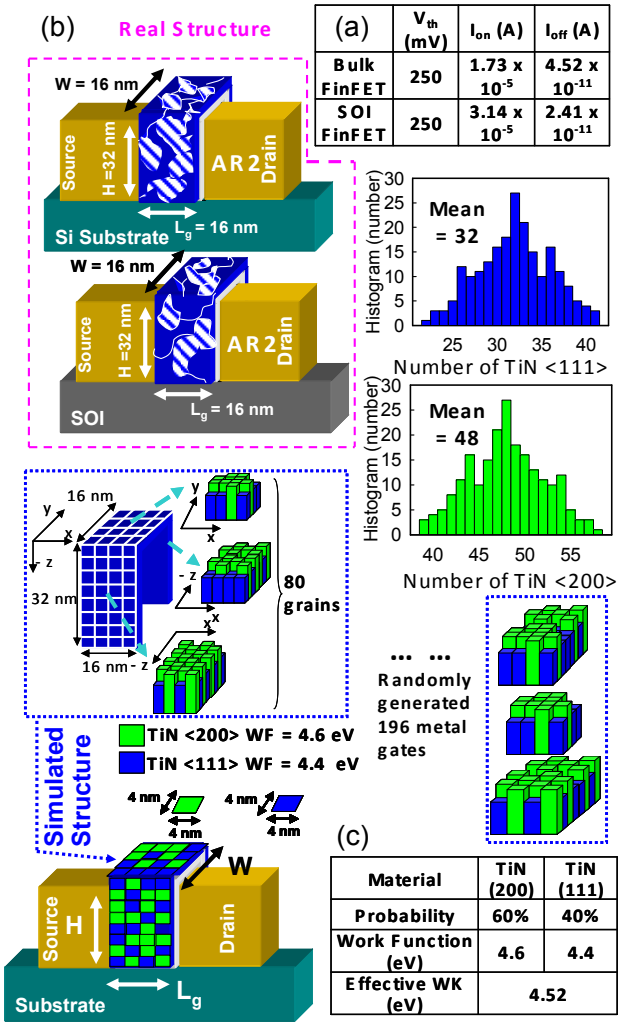
***Abstract*—In this study, the work function fluctuation (WKF) induced device variability in 16-nm-gate bulk and SOI FinFETs is for the first time explored by using an experimentally calibrated three-dimensional (3D) device simulation. Random nanosized grains of TiN gate are statistically positioned in the gate region of device to examine the associated electrostatic and carriers' transport properties, concurrently capturing random grain's size, number and position fluctuations. Both bulk and SOI FinFETs with TiN/HfO_2 gate stack are simulated, based upon experimentally available data. The approach of localized WKF simulation method is thus intensively performed to explore the device's variability including comparison between bulk and SOI FinFETs. The results of this study enable us to get an even reasonably accurate account of the random grain's number, position and size effects.**

Keywords-localized work function fluctuation; size of metal grain; random grain number, random grain position, bulk FinFET; SOI FinFET; aspect ratio; threshold voltage fluctuation; on/off-state current fluctuation; 3D device simulation

I. INTRODUCTION

Devices with vertical channel possess diverse fascinating characteristics [1-9, 13, 18-20]. High-κ/metal gate stacked fin-type field-effect-transistor (FinFET) [2-9] is promising technology in sub-22 nm device era. However, metal gate may introduce random fluctuation source, so-called the work function fluctuation [10-15] owing to the dependency of work function (WK) on metal grain's size, number and position [16]. Such uncontrollable grain orientations result in random WK of metal during fabrication period. Many studies concerning WKF on planar CMOS technology have been reported [10-12, 16]. Unfortunately, the effects of localized WKF (LWKF) on electrical characteristics with respect to the bulk and SOI FinFETs [17-20] have not been explored yet.

In this study, an experimentally validated device simulation [21] is advanced to assess the WKF on characteristics of bulk and SOI FinFETs with TiN/HfO_2 gate stack. This approach of LWKF simulation methodology enables us to study localized nanosized metal grain's effect including random grain's size, number and position on device's characteristics. The preliminary results of our study indicate the SOI FinFET exhibits relatively smaller σV_{th}, σI_{on}, and σI_{off}, and stronger immunity of WKF resulting from nanosized metal grain of TiN gate. This paper is organized as follows. In Sec. II, we brief the



(a)

	V_{th} (mV)	I_{on} (A)	I_{off} (A)
Bulk FinFET	250	1.73 x 10^{-5}	4.52 x 10^{-11}
SOI FinFET	250	3.14 x 10^{-5}	2.41 x 10^{-11}

(c)

Material	TiN (200)	TiN (111)
Probability	60%	40%
Work Function (eV)	4.6	4.4
Effective WK (eV)	4.52	

Figure 1. (a) Achieved device performance for low operating power. (b) We adopt the LWKF method [16]; we first directly partition the area of device's metal gate into 80 sub-regions following Gaussian distribution, where the average number of total generated TiN <200> and <111> orientations are 48 and 32, respectively. The schematic of N-FinFET with random (real structure) and 80 generated grains (simulation structure) in each bulk and SOI FinFET, respectively. (c) The material property of TiN. Then, we randomly assign WK in each sub-region according to stochastic property of TiN, where the probabilities of <200> and <111> grain orientations of TiN gate are 60% and 40%, respectively, and the corresponding WKs are 4.6 and 4.4 eV. Then, 196 cases are generated and mapped into device gate area for 3D device simulation.

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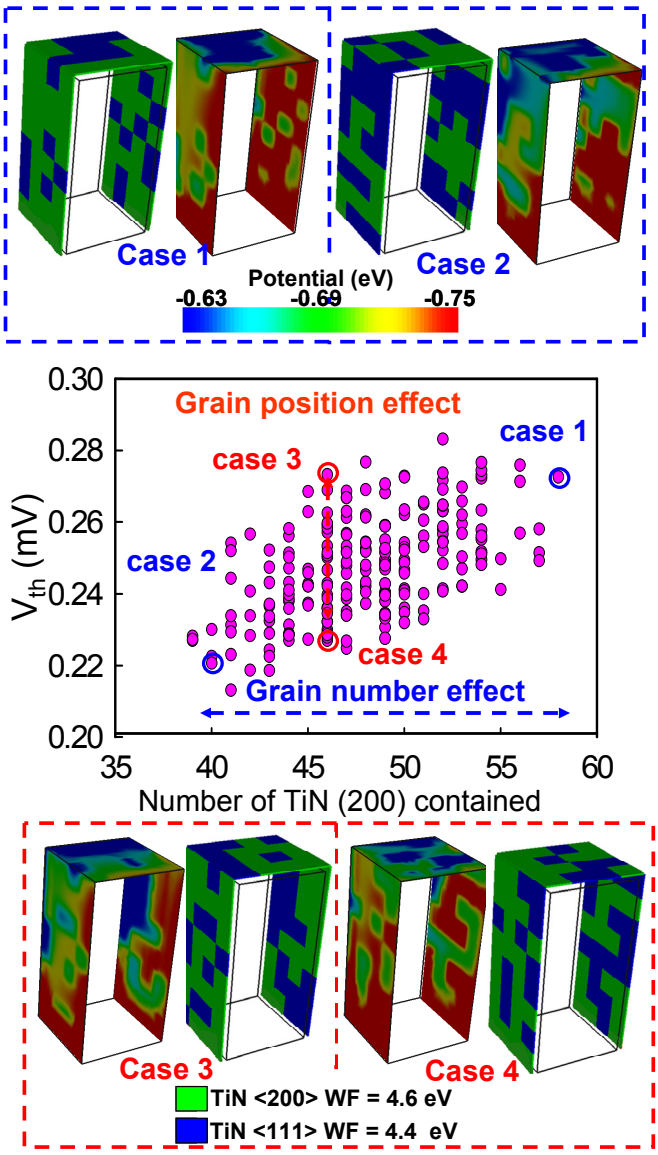

Figure 2. The V_{th} versus the number of TiN <200> orientation of the 16-nm-gate n-type bulk FinFET with (4 x 4) nm^2 grain size. The distributions of potential profiles of the case 1 and case 2 are with different number of <200> orientation (grain number effect); similarly, the distribution of potential profiles of the case 3 and case 4 are with the same number but different position of <200> orientation (grain position effect).

simulation methodology for bulk and SOI FinFET with metal grain on the gate, respectively. In Section III, we study the threshold voltage (V_{th}) and on-state and off-state current (I_{on} and I_{off}) fluctuations simulated by the 3D device simulation with random distributed nanosized WKs in bulk and SOI FinFET devices, respectively, where the fluctuation is induced by random grain's size, number and position effects. The magnitude of fluctuations between bulk and SOI FinFET is also explored. Finally, we draw conclusions.

II. The LWKF Simulation Methodology

The devices we examined are the 16-nm-gate bulk and SOI FinFETs with amorphous-based TiN/HfO_2 gate stack and the oxide thickness is fixed at 0.8 nm. The inset of Fig. 1(a) shows

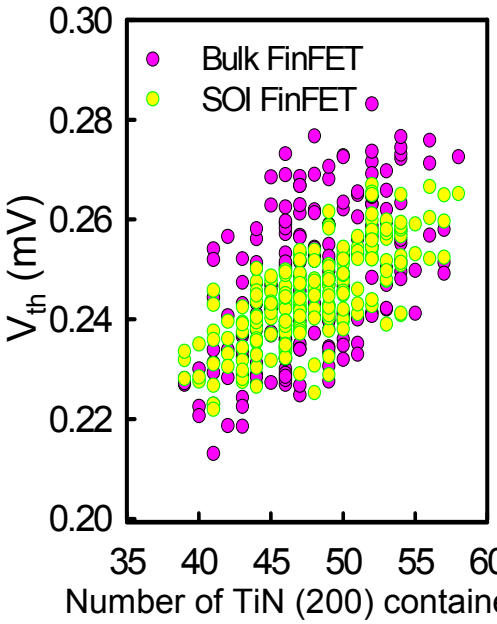

Figure 3. The V_{th} versus number of TiN <200> orientation of the 16-nm-gate n-type bulk and SOI FinFET with (4 x 4) nm^2 grain size, where the pink and yellow colors indicate value of V_{th} for bulk and SOI FinFET, respectively.

the achieved performance of the nominal bulk and SOI FinFETs, as shown in Fig. 1(a), according to ITRS Roadmap for low operating power. Different from recently reported average WKF (AWKF) method [10-12] and the compact model approach [22], we adopt the LWKF method following our recent work in planar devices [16]. For realistic structure, there have a lot of grains in the triple metal gate for both bulk and SOI FinFET devices which can not be controllable during the fabrication processes. Based upon this concept, we experimentally observed silicon data, we assume the grain size is equal to 4 x 4 nm^2 and the total area of triple gate is (2 x 32 + 16) nm^2. Then we partition the gate area into 80 sub-regions to estimate the nanosized work function's variation, as shown in Fig. 1(b), where the <200> and <111> orientations with green and blue colors indicate the values of WK = 4.6 and 4.4 eV, respectively. We randomly assign WK in each sub-region according to stochastic property of TiN listed in Fig. 1(c). The probabilities of <200> and <111> grain orientations of TiN gate are 60% and 40%, respectively. We notice that the distribution of totally generated <200> and <111> orientations are following Gaussian distribution, where the mean value of <200> and <111> orientations are 48 and 32. Finally, 196 cases with different grains in the gate area are generated and mapped into device gate area for 3D device simulation.

III. Results and Discussion

Figure 2(a) shows the distribution of threshold voltage (V_{th}) versus the number of TiN <200> orientation of the bulk FinFET, where the grain size is (4 x 4) nm^2. As the number of TiN <200> orientation increases, V_{th} becomes higher. In other words, the potential induced by local WK dominates the V_{th}. For example, the case 1 and case 2 with 58 and 40 <200> orientations result in different V_{th} owing to the random grain's number effect, where the potential profiles are altered (raised or lowered) locally by the high or low WKs. Even the number

	(2 x 2) nm^2	(4 x 4) nm^2	(8 x 8) nm^2
$\sigma V_{th,\ Bulk\ FinFET}$	8.71 mV	14.6 mV	21.5 mV
$\sigma V_{th,\ SOI\ FinFET}$	6.68 mV	9.7 mV	19.2 mV

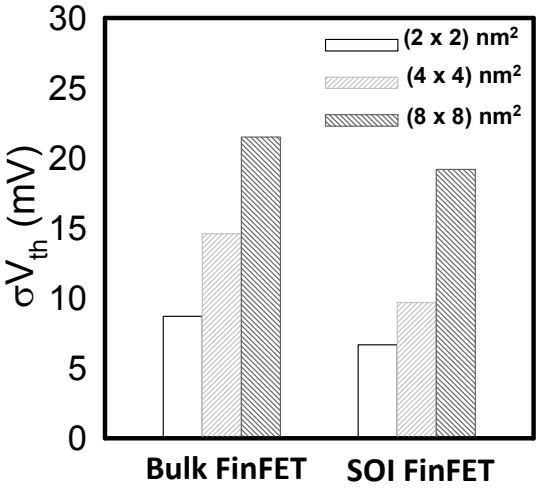

Figure 4. The σV_{th} with respect to (2 x 2), (4 x 4) and (8 x 8) nm^2 grain sizes for bulk and SOI FinFETs, respectively. The comparison of σV_{th} between bulk and SOI FinFETs is summarized in the table.

of <200> orientation is the same, the position of random grain also induce rather different V_{th}, as shown in the case 3 and case 4, respectively, where the total number of <200> orientation is 46. Similarly, for SOI FinFET, the V_{th} variation is affected by number and position effect of WKs, but the distribution of V_{th} is smaller than the results of bulk FinFET owing to almost fully depleted channel, as shown in Fig. 3, where the pink and yellow colors indicate bulk and SOI FinFETs, respectively. The estimated V_{th} fluctuation (σV_{th}) is summarized in Fig. 4. The results show that the σV_{th} of SOI FinFET is 1.5 (i.e., 14.6 mV / 9.7 mV) times smaller than that of bulk FinFET with (4 x 4) nm^2 grain size, where the values of σV_{th} for different gain size are summarized in the inset of Fig. 4.

The *x*-*y* and *y*-*z* cross-sectional views of SOI FinFET in Fig. 5(a) are shown in Fig. 5(b). A plot of the source-to-drain potential barrier of SOI and bulk FinFETs ares shown in Fig. 5(c). The on-state current fluctuation of the SOI FinFET has smaller leakage current than that of bulk FinFET near the substrate. The difference can be investigated from the channel region. Inside the channel region, although the potentials (*x*-*y* cross-sectional view) are disturbed by different WK locally for both bulk and SOI FinFETs, the potential is weaker at the middle and bottom for bulk FinFET, as shown in Figs. 5(d) and 5(e), respectively. The distribution of conducting current (*y*-*z* cross-sectional view) is strongly dependent on different WK on the channel surface for SOI FinFET. However, the weak potential (blue color) can not control the disturbance from grain orientation locally and increase the leakage current for bulk FinFET, especially at the bottom of channel, as shown in Figs. 5(f) and 5(g). Therefore, the SOI FinFET has smaller (σI_{on}), and off-state current fluctuation (σI_{off}), as shown in Fig. 6. Note the effect of (2 x 2) and (8 x 8) nm^2 grain sizes on both bulk and SOI FinFETs are shown in Fig. 4. The results show that the σV_{th} induced by the (2 x 2) nm^2 grain size are 8.71 and

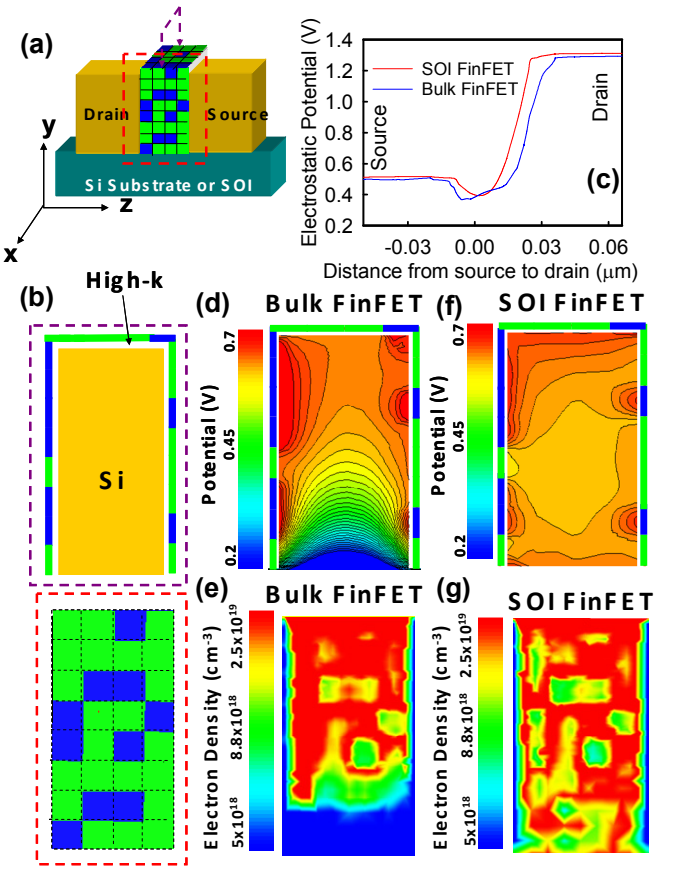

Figure 5. (a) Schematic of selected lateral gate, where (b) are the corresponding *x*-*y* and *y*-*z* cross-sectional views with (4 x 4) nm^2 grain size. (c) The on-state (V_D = V_G = 0.8 V) profile of electrostatic potential from the source to drain. The on-state potential profile of x-y cross-sectional view for both (d) bulk and (e) SOI FinFETs. (f) The on-state electron distribution of *y*-*z* cross-sectional view for both (f) bulk and (g) SOI FinFETs, where the higher WK results in higher potential and electron density.

6.68 mV for bulk and SOI FinFETs, respectively. And, its σV_{th} is 2.5 and 2.9 times smaller, compared with the results of (8 x 8) nm^2 grain size in bulk and SOI FinFETs, respectively. The σV_{th} increases as the grain size increases. Figure 6 shows the adopted SOI FinFET with small grain size suppresses the on-/off-state current fluctuations.

IV. Conclusions

Based on the localized work function simulation, the DC characteristic fluctuations of 16 nm bulk and SOI FinFET devices have been simulated and compared. The later one exhibits relatively smaller threshold voltage fluctuation, on-state current fluctuation and off-state current fluctuation. A stronger immunity of WKF of SOI FinFET device resulting from nanosized metal grains of TiN gate is observed, compared with bulk FinFET one. The engineering findings of localized WKF have been observed in terms of random grain's number, position and size effects. The σV_{th} for bulk and SOI FinFETs with (4 x 4) nm^2 grain size are 14.6 and 9.7 mV. The difference (they are 8.71 and 6.68 mV) is reduced when bulk and SOI FinFETs are with (2 x 2) nm^2 grain size. We are studying the fluctuation resulting from process variation effect (PVE) and WKF and comparing with silicon data of FinFET devices.

	(2 x 2) nm^2	(4 x 4) nm^2	(8 x 8) nm^2
$\sigma I_{on,\ Bulk\ FinFET}$	$1.49x10^{-7}$A	$6.59x10^{-7}$A	$1.7x10^{-6}$ A
$\sigma I_{on,\ SOI\ FinFET}$	$1.44x10^{-7}$ A	$6.09x10^{-7}$ A	$6.28x10^{-7}$A
$\sigma I_{off,\ Bulk\ FinFET}$	$2.53x10^{-11}$A	$2.73x10^{-11}$ A	$9.88x10^{-11}$ A
$\sigma I_{off,\ SOI\ FinFET}$	$2.05x10^{-11}$A	$2.18x10^{-11}$ A	$4.84x10^{-11}$ A

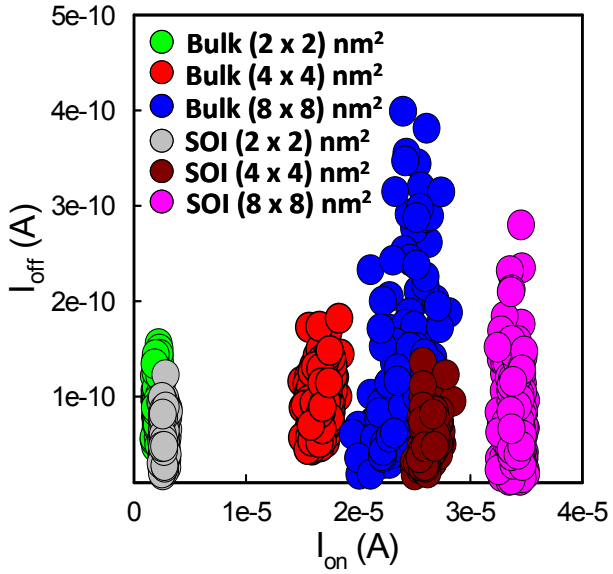

Figure 6. The I_{on}-I_{off} curve of bulk and SOI FinFETs with (2 x 2), (4 x 4) and (8 x 8) nm^2 grain sizes of TiN gate, where the corresponding σI_{on}, and σI_{off} are summarized in the table.

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