FinFET SRAM Cell Optimization Considering Temporal Variability due to NBTI/PBTI and Surface Orientation

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***Abstract*—This paper analyzes the impact of intrinsic process variation and NBTI/PBTI induced time-dependent variations on the stability/variability of 6T FinFET SRAM cells with various surface orientations. Due to quantum confinement, (110)-oriented pull-down devices with fin Line Edge Roughness (LER) show larger Vread,0 and Vtrip variations, thus degrading RSNM and its variability. (100)-oriented pull-up devices with fin LER show larger Vwrite,0 and Vtrip variations, hence degrade the variability of WSNM. The combined effects of intrinsic process variation and NBTI/PBTI induced variations have been examined to optimize the FinFET SRAM cells. Pull-up devices with (110) orientation suffer larger NBTI, resulting in large Vtrip variation and significant degradation of RSNM. Our study indicates that consideration of NBTI/PBTI induced temporal variation changes the optimal choice of FinFET SRAM cell surface orientations in term of µRSNM/σRSNM.**

I. Introduction

Multi-gate FinFETs are promising device candidates for post-22 nm CMOS technology generations due to their superior short channel effects, better subthreshold slope, and reduced random dopant fluctuation. The sidewall surface (conducting channel) orientation of FinFET devices can be easily changed by rotating the layout of the devices to improve electron and hole mobility [1]. Negative and Positive Bias Temperature Instabilities (NBTI (for PFET) and PBTI (for NFET)) have become major long-term reliability concerns as they weaken MOSFETs over time, thus resulting in temporal degradation in the stability of the SRAM cells [2-4]. FinFET devices with different surface orientations exhibit distinct threshold voltage variations resulting from intrinsic process variations and NBTI/PBTI induced temporal variations. Fig. 1 (a) and (b) illustrate the 6T FinFET SRAM cells with (110)/(100) surface (conducting channel) orientations by rotating the FinFET devices. The layouts are based on scaled ground rules from 32 nm node according to ITRS projection. In this work, for the first time, the combined effects of short-term intrinsic process variability and long-term temporal variability (due to NBTI/PBTI) are considered for optimizing the FinFET device orientation combinations to improve the stability/variability of 6T FinFET SRAM cells.

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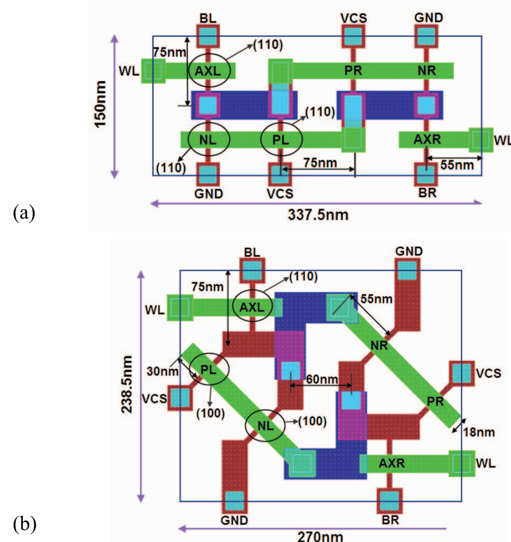


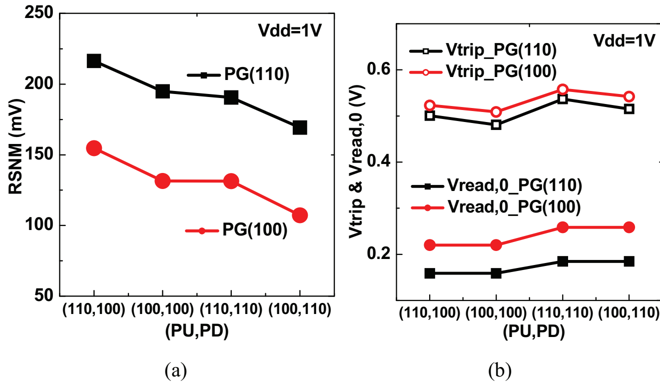
Fig. 1. (a) Pull-up (PL/PR), pull-down (NL/NR) and pass-gate transistors (AXL/AXR) all with (110) orientation. (b) (100) pull-up, (100) pull-down and (110) pass-gate transistors.

II. Device Design and Simulation Methodology

In this work, 6T FinFET SRAM designed with 18nm (L_g) FinFET devices (W_{fin}=5nm, T_{ox}=1nm, H_{fin}=15nm, channel doping=1e17cm^{-3}, V_{dd}=1V) are analyzed using mixed-mode simulation [5]. The quantum-confinement effect is calibrated with exact solution of Schrödinger's equation to accurately consider the threshold voltage sensitivity to process variation for (100)/(110) N/PFETs. Reaction-Diffusion model [6] is used to calibrate the threshold voltage drift due to NBTI/PBTI [7, 8]. To assess the dominant process variation source, fin LER [9], the line edge patterns have been derived using Fourier synthesis [10], and then, the Monte Carlo simulations with 200 samples were performed for each case.

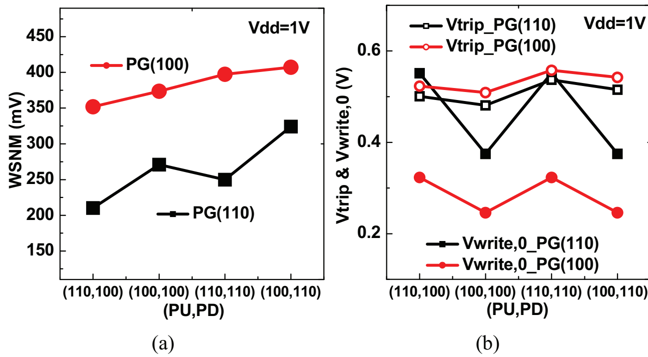
III. 6T FinFET SRAM Cells with (110)/(100) Surface Orientations

Pull-up (PU), pull-down (PD) and pass-gate (PG) transistors with (110) and (100) orientations can be combined for 8 types of 6T FinFET SRAM cells. Fig. 2(a) and (b) show the RSNM (Read Static Noise Margin) and Vread,0/Vtrip (defined in Fig. 4(a) inset) comparisons among the 8 types of



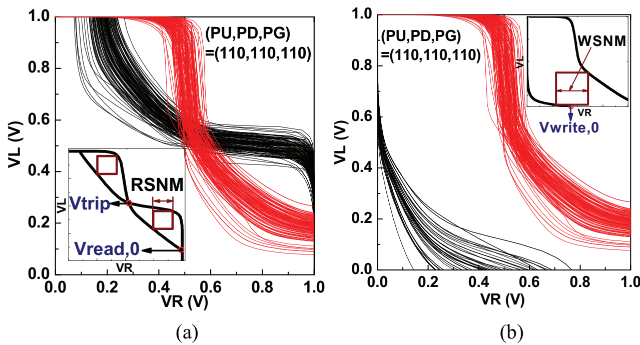
(a) (b)

Fig. 2. (a) RSNM, and (b) Vread,0/Vtrip comparisons among 8 types of 6T FinFET SRAM cells.



(a) (b)

Fig. 3. (a) WSNM, and (b) Vwrite,0/Vtrip comparisons for 8 types of 6T FinFET SRAM cells.



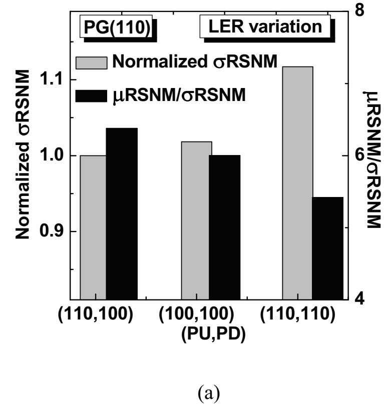
(a) (b)

Fig. 4. (a) RSNM variation, and (b) WSNM variation due to fin LER. (correlation length=20nm, rms amplitude =1.5nm [9]).

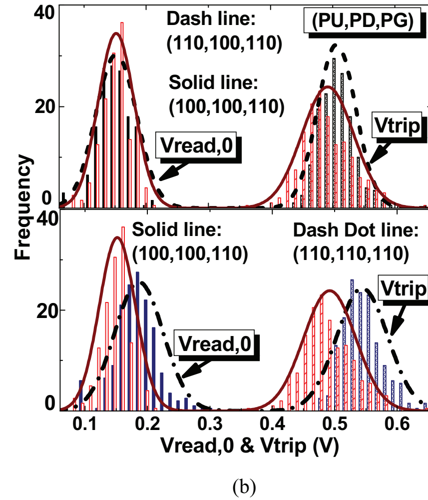
cells. FinFET SRAM cells with (110) PG show lower Vread,0 and higher RSNM. (PU,PD,PG)=(110,100,110) and (100,100,110) show higher RSNM than the standard SRAM cell with all (110) devices. Fig. 3(a) and (b) show the WSNM (Write Static Noise Margin) and Vwrite,0/Vtrip (defined in Fig. 4(b) inset) comparisons. (100) PG with stronger strength shows lower Vwrite,0 and larger WSNM.

A. Short-Term Stability/Variability due to Process Variation

Fig. 4 shows degraded Read/Write stability of 6T FinFET SRAM cell due to LER. Fig. 5(a) shows the normalized



(a)



(b)

Fig. 5. (a) (110,100,110) SRAM cell shows largest μRSNM/σRSNM. μRSNM: mean of RSNM; σRSNM: standard deviation of RSNM. (b) Vread,0 and Vtrip variation comparisons.

σRSNM and μRSNM/σRSNM comparisons among the 3 types of FinFET SRAM cells which have higher RSNM. SRAM cell with orientation (PU,PD,PG) = (100,100,110) shows larger σRSNM than the (110,100,110) one. Because (100) PU devices with stronger quantum confinement exhibit larger threshold voltage variation due to fin LER than the (110) PU devices, the (100,100,110) SRAM cell shows larger Vtrip variation (Fig. 5(b)) and σRSNM than the (110,100,110) cell. The voltage margin between Vread,0 and Vtrip is larger in the (110,100,110) cell than the (100,100,110) one, which indicates the μRSNM is larger in the (110,100,110) SRAM cell. Therefore, the (110,100,110) SRAM cell shows larger μRSNM/σRSNM than the (100,100,110) one. (PU,PD,PG) = (110,110,110) SRAM cell shows higher σRSNM than the (100,100,110) cell because the (110) NFET with stronger quantum confinement shows larger threshold voltage variation due to fin LER than the (100) NFET. (110,110,110) SRAM cell with both (110) PD and PG devices shows larger Vread,0 variation and degrades the RSNM variability (Fig. 5(b), bottom).

Fig. 6(a) compares the normalized σWSNM and μWSNM/σWSNM. (PU,PD,PG) = (100,100,110) SRAM cell

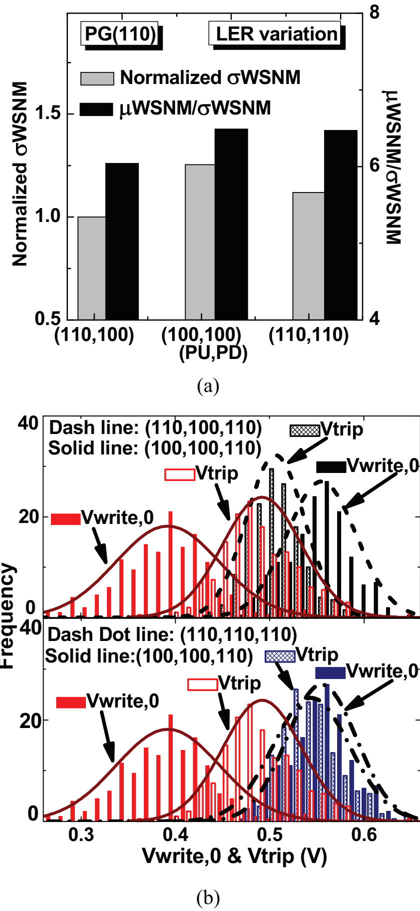


Fig. 6. (a) (100,100,110) SRAM cell shows largest µWSNM/σWSNM. µWSNM: mean of WSNM; σWSNM: standard deviation of WSNM. (b) Vwritet,0 and Vtrip variation comparisons.

shows larger Vwrite,0 variation, Vtrip variation (Fig. 6(b)) and σWSNM due to larger variations of (100) PU and (110) PG devices. However, (100,100,110) SRAM cell still shows higher µWSNM/σWSNM due to its larger µWSNM.

B. Long-Term Stability/Variability due to NBTI/PBTI

Fig. 7 shows the time-dependent threshold voltage increase ($|\Delta V_{th}|$) due to NBTI and PBTI, and the inset demonstrates the good calibration results with published data [7,8]. NBTI induced $|\Delta V_{th}|$ is larger than PBTI by ~1 order of magnitude for the poly-gate FinFETs studied. Degradation in SRAM stability with time under worst-case stress pattern/condition (extreme asymmetry condition, only PR with NBTI and NL with PBTI) is considered (Fig. 8). Fig. 9(a) shows the impact of NBTI/PBTI induced $|\Delta V_{th}|$ on the RSNM. FinFET SRAM cells with (110) PU devices suffer larger NBTI degradation due to higher number of interface traps, resulting in larger degradation in RSNM. RSNM degradation results mainly from the NBTI induced decrease in Vtrip in poly-gate FinFET technology as shown in Fig. 9(b). In contrasted with the significant RSNM degradation due to NBTI/PBTI, Fig. 10 shows that the WSNM only degrades

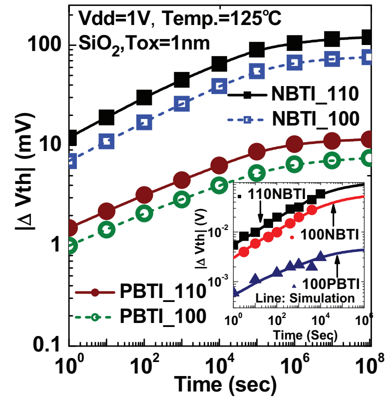


Fig. 7. NBTI/PBTI induced V_{th} shift for (110)/(100) orientation. Inset shows the model-data calibration.

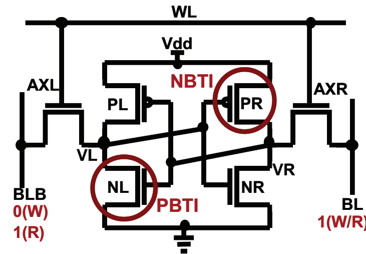
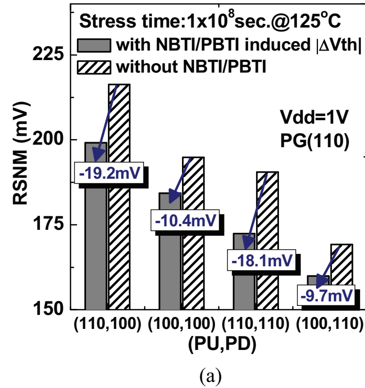


Fig. 8. Worst case stress scenario for Read (R) and Write (W) stability.



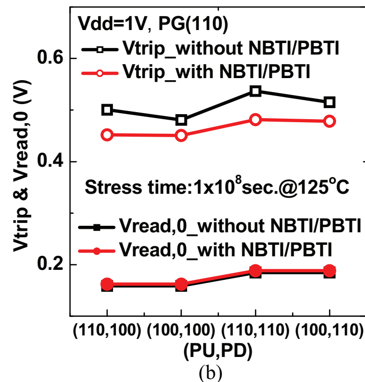


Fig. 9. (a) RSNM degradation due to NBTI/PBTI. (b) Vtrip reduction due to NBTI is larger for (110) PU devices.

slightly. This is because WSNM is mainly determined by the NBTI_Read (NBTI_R) and PBTI_Write (PBTI_W) voltage

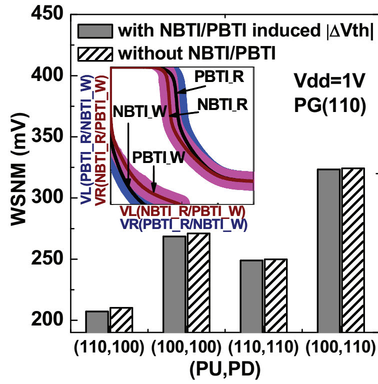
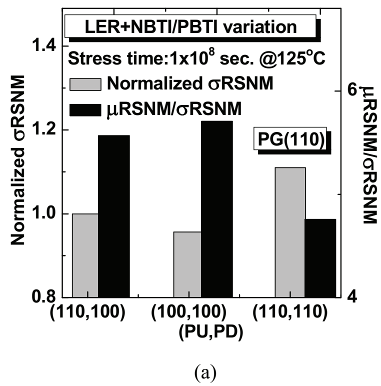
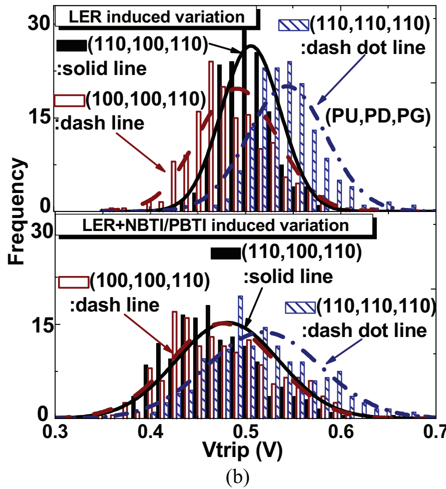


Fig. 10. Slight degradation in WSNM due to NBTI/PBTI under worst case stress condition. NBTI/PBTI stress time is $1\text{x}10^8$ sec. @ 125℃.



(a)



(b)

Fig. 11. (a) Normalized σRSNM and μRSNM/σRSNM comparison considering fin LER and NBTI/PBTI induced variation. (100,100,110) SRAM cell shows largest μRSNM/σRSNM. (b) (110) PU devices show larger time-dependent Vtrip variability degradation. NBTI/PBTI stress time is $1\text{x}10^8$ sec. @ 125℃.

transfer curves (Fig. 10 inset). The long-term WSNM variability degrades slightly as compared with the short-term WSNM variability. Fig. 11 (a) shows the long-term RSNM variability considering LER and NBTI/PBTI induced V_{th} variation. SRAM cells with (110) PU devices show decreased μRSNM and larger Vtrip variation as shown in Fig. 11(b). Therefore, due to NBTI/PBTI, SRAM cells with (110) PU devices show larger decrease in μRSNM/σRSNM than SRAM

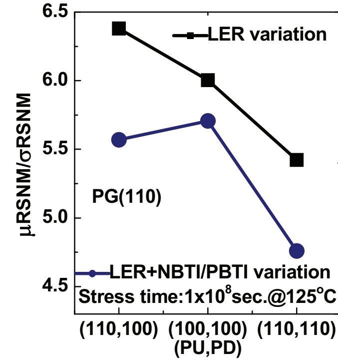


Fig. 12. μRSNM/σRSNM comparison considering short-term (fin LER) and long-term (fin LER + NBTI/PBTI) variations.

cells with (100) PU devices. Fig. 12 demonstrates that NBTI/PBTI induced temporal variability in SRAM will change the optimal choice of FinFET SRAM cells from (110,100,110) to (100,100,110). As compared with the (PU,PD,PG) = (110,110,110) SRAM cell, optimized 6T FinFET SRAM cell (100,100,110) improves the μRSNM/σRSNM by 20% and μWSNM/σWSNM slightly.

In summary, the time-dependent V_{th} drift and variation due to NBTI/PBTI degrades the stability/variability of RSNM (significantly) and WSNM (slightly). Our study indicates that optimum FinFET SRAM design has to consider the combined effects of intrinsic process variability and the temporal variability introduced by NBTI/PBTI.

REFERENCES

[1] K. Shin, C. O. Chui, and T.-J. King, "Dual Stress Capping Layer Enhancement Study for Hybrid Orientation FinFET CMOS Technology," *IEDM Tech. Dig.*, 39-6, 2005.

[2] S. Mitra, "Circuit Failure Prediction for Robust System Design in Scaled CMOS," *in Proc. IRPS*, Phoenix, AZ, pp. 524-531, 2008.

[3] V. Huard, C. Parthasarathy, C. Guerin, T. Valentin, E. Pion, M. Mammasse, N. Planes, and L. Camus, "NBTI degradation: From transistors to SRAM arrays," *in Proc. IRPS*, Phoenix, AZ, pp. 289-300, 2008.

[4] S. E. Rauch Ⅲ, "Review and reexamination of Reliability Effects Related to NBTI-Induced Statistical Variations," *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 4, pp. 524-530, 2007

[5] Sentaurus TCAD, C2009-06 Manual

[6] M.A. Alam, and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Microelectronics Relia.*, vol. 45, pp. 71-81, 2005.

[7] S. Zafar, M. Yang, E. Gusev, A. Callegari, J. Stathis, T. Ning, R. Jammy, and M. Ieong, " A Comparative Study of NBTI as a function of Si Substrate Orientation and Gate Dielectrics (SiON and SiON/HfO_2), *VLSI-TSA*, pp. 128, 2005.

[8] S. Zafar, Y. H. Kim, V. Narayanan, C. Cabral Jr., V. Paruchuri, B. Doris, J. Stathis, A. Callegari, and M. Chudzik, " A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO2/HfO2 Stacks with FUSI, TiN, Re Gates," *Symp. on VLSI Tech.*, 2006.

[9] A. Dixit, K. G. Anil, E. Baravelli, P. Roussel, A. Mercha, C. Gustin, M. Bamal, E. Grossar, R. Rooyackers, E. Augendre, M. Jurczak, S. Biesemans, and K. De Meyer, " Impact of Stochastic Mismatch on Measured SRAM Performance of FinFETs with Resist/Spacer-Defined Fins: Role of Line-Edge-Roughness," *IEDM Tech. Dig.*, 27-8, 2006.

[10] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic Parameter Fluctuations in Decananometer MOSFETs Introduced by Gate Line Edge Roughness," *IEEE Trans, Electron Devices*, vol. 50, no. 5, pp. 1254-1260, 2003.