Multiphysics modeling of PCM devices for scaling investigation

G. Ferrari*, A. Ghetti†, D. Ielmini*, A. Redaelli† and A. Pirovano†
*Politecnico di Milano, Milano, Italy
†Numonyx, R&D - Technology Development, Agrate Brianza, Italy

***Abstract*— A multiphysics model for Phase Change Memory (PCM) is calibrated on a large set of experimental data. Critical material and interface properties such as electrical and thermal resistivities and their dependence on temperature are extracted from data or fitting electrical characteristics with numerical simulations. The model is shown to match with a unique set of parameters experimental data from 90nm and 45nm technology nodes. The calibrated model is then exploited to perform a sensitivity analysis of key cell characteristics to geometry and material properties variations. Furthermore, the model is used to predict performance of a scaled down cell suitable for the 32nm technology node and the results demonstrate the consistent scalability of PCM with respect to the technology node.**

I. Introduction

In recent years, several new non-volatile memory concepts are being extensively investigated as viable alternative to the traditional floating-gate technology as its scaling is becoming increasingly difficult and costly. One of the most promising candidate is Phase Change Memory (PCM) because of its fast read and write operations, bit alterability, high endurance and retention and the potential for high density and better scalability [1]. PCM operation relies on the largely different electrical resistivity of the crystalline and amorphous phases of a particular class of materials, typically chalcogenide alloys like $Ge_2Te_2Sb_5$ (GST). Information storage is attained by switching the active material phase increasing the temperature of the device active region above its melting point by Joule heating, and then rapidly cooling it down. The temperature quenching rate, controlled through a properly designed electrical pulse, determines whether the chalcogenide solidifies in a crystalline low-resistive (SET) or amorphous high-resistive (RESET) state. Therefore accurate PCM modeling requires a detailed description of the interactions between electrical and thermal effects in a complex three-dimensional structure, in presence of different materials and interfaces.

The goal of this work is to extract material thermal and electrical properties from experimental data and by numerical simulations. The resulting calibrated model will then be used in two important applications: an analysis designed to assess the impact of geometrical variations on cell merit parameters and a simulation aimed to estimate performance of future technology nodes.

II. Model calibration and simulation results

We adopt for the chalcogenide material the semiconductor-like model described in detail in [2], in which both crystalline and amorphous phases are described by a band structure with their own energy gap, effective state density and trap states. The model self-consistently solves the standard semiconductor equations for the current density and the heat equation for the temperature profile in conjunction with a phase change algorithm accounting for both crystal growth and nucleation in a Monte Carlo manner [3].

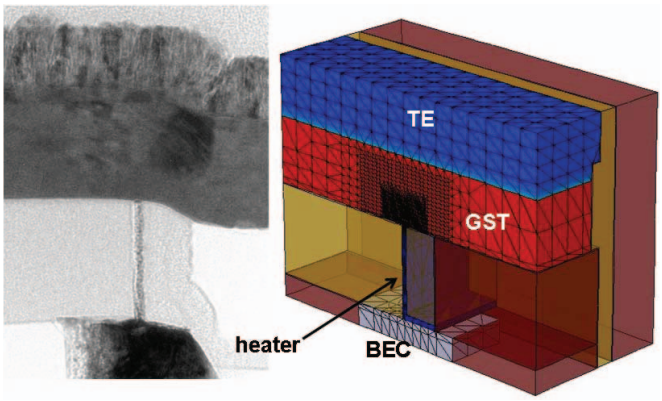

Fig. 1. TEM image of a 45nm "wall" cell (left) and corresponding 3D simulated structure (right). Only half structure is shown. Dielectric materials are shown transparent.

Our primary focus was on the crystalline phase, due to its importance in determining readout and programming characteristics and because it is best described by an energy band model. In particular, low-field resistance (R_{SET}), differential resistance at high currents (R_{ON}) and melting current (I_M) were analyzed, since they provide key information on device performance.

Figure 1 shows the three-dimensional simulated structure representing our proprietary "wall" cell architecture [4], [5], in which the active region lies at the interface between the thin vertical heater and an horizontal line of GST. One of the key original features of the present model is the adoption of an interface thermal resistance of $5{\cdot}10^{-4}$cm^{2}K/W at the interface of any dielectric layer as obtained from measurements. Another important ingredient is an interface electrical resistance at the GST/heater interface.

Following the methodology in [6] we tried to extract as much information as possible from experimental data. To this purpose we collected experimental measures of R_{SET}, R_{ON} and I_M as a function of some geometrical properties. As an

978-1-4244-7700-5/10/$26.00 ©2010 IEEE

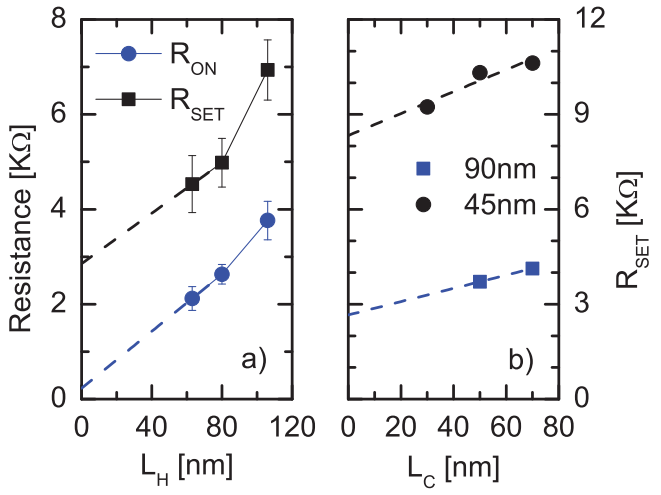

Fig. 2. a) R_{ON} and R_{SET} resistance of 90nm cells for different L_H. b) R_{SET} resistances of 90nm (blue) and 45nm (black) cells for different L_C.

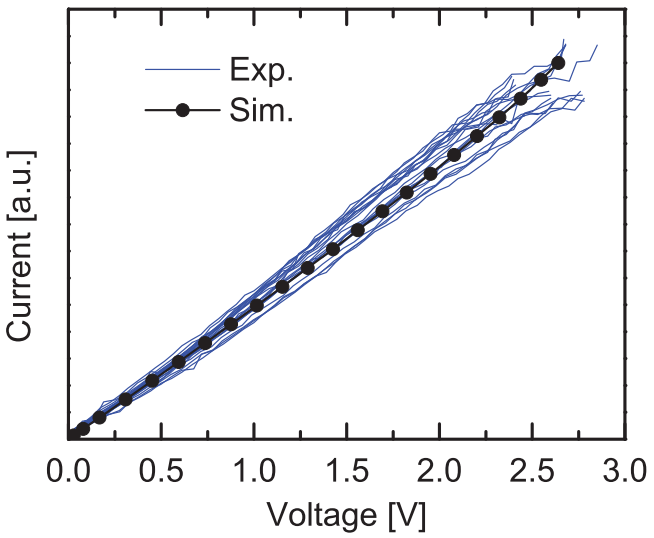

Fig. 3. I-V characteristics for a group of cells without GST. The curves have been fitted by varying the bulk heater power law temperature dependence coefficient. Symbols: simulation.

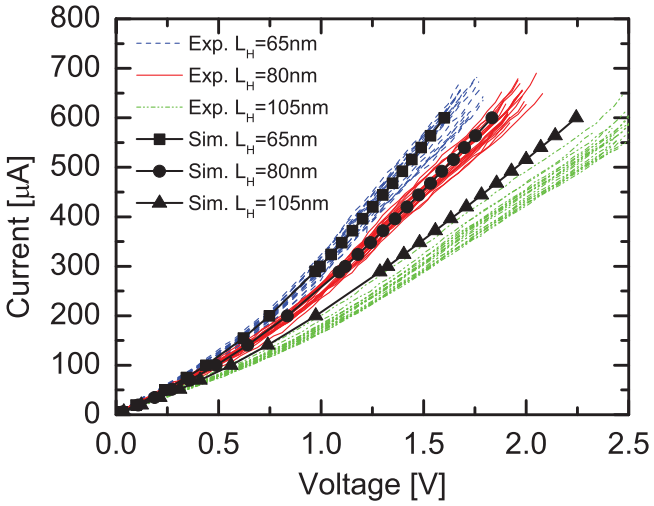

Fig. 4. SET state I-V characteristic of 90nm cells for varying L_H. Blue: 65nm, green: 80nm, red: 105nm. Symbols: simulations.

example, Fig. 2.a shows measures of R_{ON} and R_{SET} for different heater heights (L_H). Each point represents an average of about fifty cells. The cell can be depicted with the series of three temperature (T) dependent resistances, describing the heater (ρ_H), the GST/heater interface resistance (R_{itf}) and the chalcogenide (R_{GST}), in the form

$$R_{cell} = R_{GST}(T) + \rho_H(T) \cdot \frac{L_H}{A_H} + R_{itf}(T) \ . \qquad (1)$$

Due to its temperature dependence, crystalline GST resistivity drops considerably at high current because of self-heating, thus R_{ON} is dominated by the heater resistance. It is then possible to extract heater resistivity and GST/heater interface resistance from the slope and the intercept, respectively, of the R_{ON} vs. L_H curve. Similarly, Fig. 2.b shows R_{SET} of 90nm and 45nm cells for varying GST heights (L_C). Since in this case L_H is constant, R_{SET} depends on L_C only through the variation of the GST layer resistance. This variation is non-linear due to geometry of the cell (current flows from a narrow heater and spreads into a wide GST region), nevertheless the slope of the R_{SET} vs. L_C curve gives an estimate of GST bulk resistivity at low temperature. The resistivity is found to be between 15mΩcm and 35mΩcm, consistent with literature data [7]. A value of 27mΩcm was chosen, as it is able to fit both 90nm and 45nm data.

Heater bulk resistivity and GST/heater electrical resistance are assumed to follow a power-law dependence on temperature [6]. The exponent of such power law for heater bulk resistivity can be inferred considering cells without the GST layer. Since in this case also the GST/heater interface resistance is obviously not present the resulting I-V characteristics are determined entirely by $\rho_H(T)$. The best fit shown in Fig. 3 provided the calibrated value. Notice that: i) Fig. 3 further validates the heater bulk resistivity previously extracted from R_{ON}; ii) in this particular structure with no GST the $\rho_H(T)$ non linearity is less evident than in the real cell because lower temperature are attained since the top electrode, that is also a good heat sink, is closer to the heated region. Finally, the exponent for the GST/heater interface has been calibrated by fitting the overall I-V characteristics for different L_H, as shown in Fig. 4. The extracted parameters provide a good fit for all cell groups.

Next, GST thermal conductivity (K_C) can be inferred from I_M, since K_C determines the temperature reached in the active region by controlling the heat conduction in the chalcogenide, whereas it has little impact on the I-V characteristics, dominated in most of the operative range by the heater properties. I_M is defined as the current pulse amplitude at which cell resistance (R) increases by a factor 1.2. A change in K_C results in a shift of the R-I curve, while its slope remains unaffected, thus we deduced K_C by fitting the measured R-I curves with simulations. The best overall fit, demonstrated

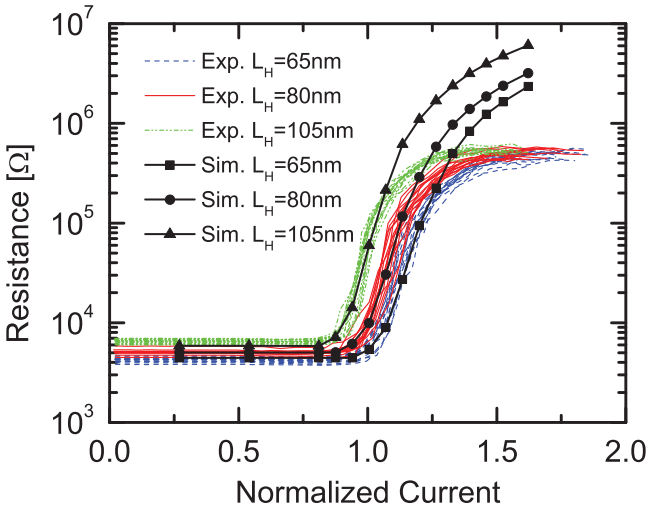

Fig. 5. Pulsed R-I curves of 90nm cells for various L_H. All currents are normalized to the melting current of the L_H=80nm device.

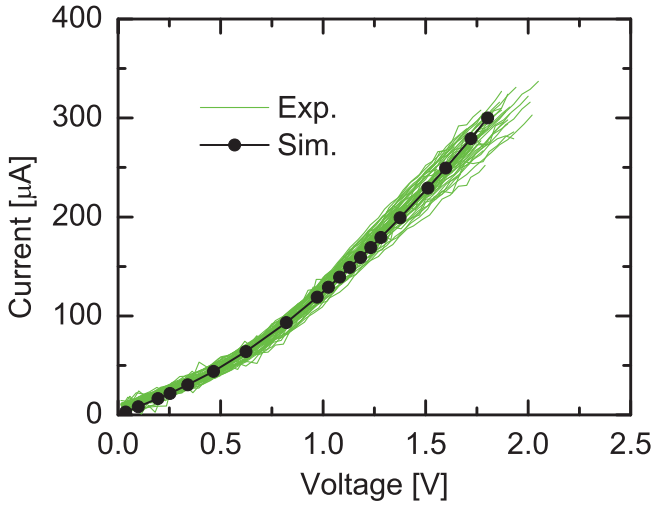

Fig. 7. I-V characteristics for about fifty 45nm cells (solid lines). Symbols: simulation.

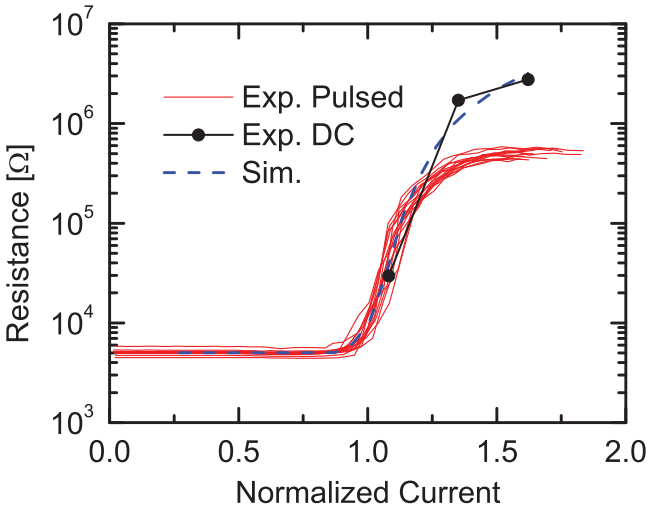

Fig. 6. Comparison of pulsed (solid lines) and DC (symbols) measurements with simulated (dashed line) R-I curves for L_H=80nm.

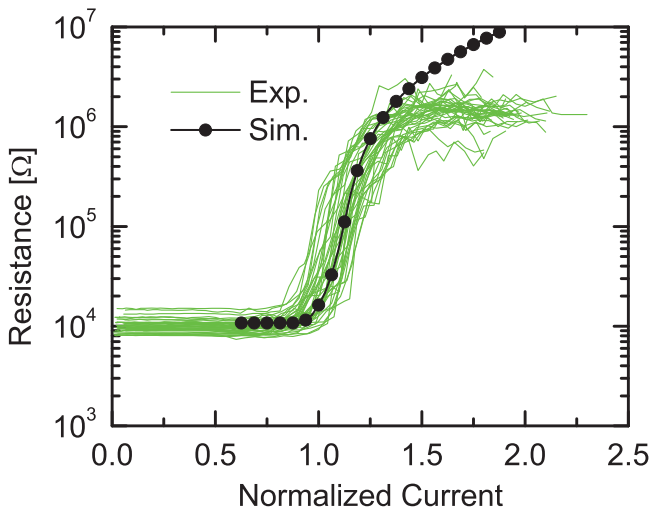

Fig. 8. R-I programming curves for about fifty 45nm cells (solid lines). Symbols: simulation. Current is normalized to average melting current.

in Fig. 5, was achieved with K_C=5.7mW/cmK in agreement with literature data [8]. Notice that the discrepancy between experiments and simulations for R>1MΩ is an artifact due to: i) a limitation of the experimental setup needed to measure pulsed R-I characteristics in sensing low currents when R is large, and ii) to the fact that we model a drifted GST whereas measured R is taken right after the programming pulse. To check this issue we measured a drifted cell resistance with a parameter analyzer in DC (Fig. 6). The two setups provide the same value for low R, while the DC measurement provides a higher R for high programming current that is well reproduced by our calibrated simulations.

Finally, the same set of model parameters has been used to simulate a 45nm technology PCM cell. Figures 7 and 8 show I-V and R-I curves for about fifty cells and the respective simulation results. The model accurately reproduces the curves, thus it can be reliably used to estimate performance of future technology nodes or of more complex geometries. In summary, Table I reports the calibrated parameters.

III. Sensibility Analysis

The so-calibrated model was then used to analyze sensitivity of cell properties to variations of: heater and GST length, cell width, heater and GST resistivity, heater thickness, GST thermal conductivity and melting current. A series of simulations were run by sweeping the variables one at a time from -20% to +20% of their nominal value. The slope was taken as the sensitivity as shown in figure 9 for R_{SET}. Cell width (W) and heater thickness (t_h) are the main contributors to resistance variations. These coefficients can then be used to perform a statistical distribution analysis of a large number of cells and demonstrate that tight R distributions are achievable by optimizing the process flow to reduce geometrical variations.

TABLE I

LIST OF CALIBRATED PARAMETERS.

GST/Heater interface resistivity (R_{itf})	4e-9	Ωcm^2
R_{itf} power law exponent	-0.15	
Heater bulk resistivity power law exponent	-0.03	
GST resistivity @ 300 K (ρ_{GST})	27	mΩcm
Heater thermal conductivity	50	mW/cmK
GST thermal conductivity	5.7	mW/cmK

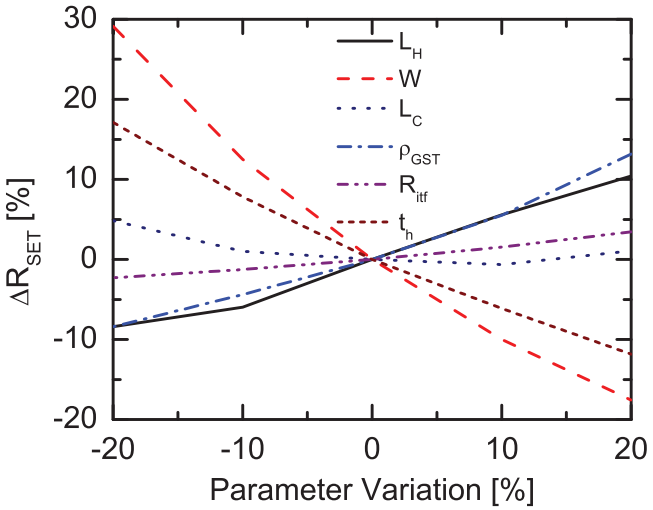

Fig. 9. Relative variations of R_{SET} as a function of relative variations of cell geometry and electrical properties.

IV. PERFORMANCE SCALING ANALYSIS

The calibrated model was also exploited to perform a scaling analysis. The structure reported in Fig. 1 has been anisotropically scaled down to physical dimensions suitable for the 32nm technology node, leaving all extracted parameters and interfaces unaltered. Figure 10 compares the I-V and R-I characteristics of three technology node cells. They do not scale regularly because cells have been scaled strongly anisotropically from one generation to the other due to different technology constraints. From 90nm to 45nm generation the main variation was a reduction of W by a factor of about $3\times$ not balanced by a similar reduction of L_C and L_H, thus resulting in a total increase(decrease) of $R_{SET}(I_M)$ by a factor of $2\times$. On the other hand, from the 45nm to the 32nm generations W was scaled slightly less than L_C and L_H while keeping t_h constant. In this latter case, the numerical model used in this work provides a slightly larger R_{SET} and smaller I_M, thus still showing the advantage of scaling. Notice that, although simpler analytical approaches like the one in [9] would predict similar qualitative trends as shown in Fig. 11, only the calibrated multiphysics numerical model that properly accounts for electrical and thermal resistance scaling and the role of interfaces in a complex structure provides a quantitatively reliable estimates of PCM cell electrical performance.

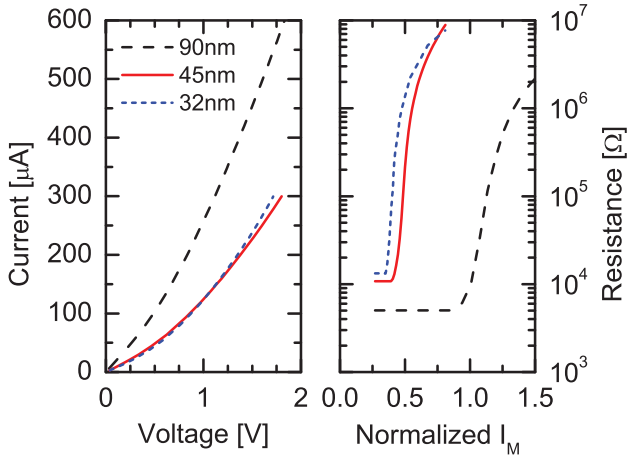

Fig. 10. Simulated I-V (left) and R-I (right) curves for cells from three different technology nodes. In the R-I characteristic, current is normalized to the melting current of the 90nm cell. Simulation for the 90nm and 45nm technology cells are the same shown in Fig. 4 and 7, respectively.

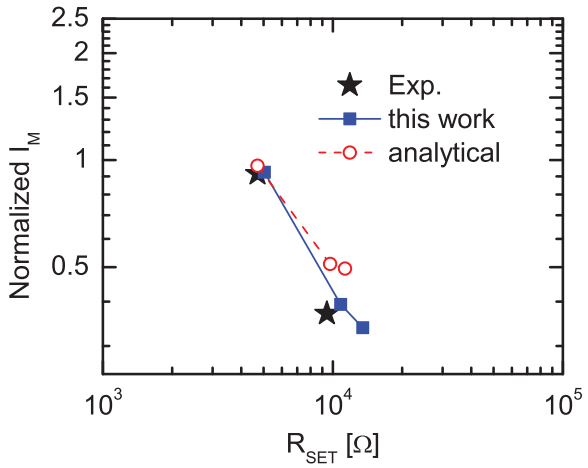

Fig. 11. Bilogarithmic graph representing scaling trends for R_{SET} and I_M.

V. CONCLUSION

A multiphysics numerical model for PCM has been successfully calibrated demonstrating to be able to fit with an unique set of parameters experimental data from 90nm and 45nm technology cells. The model has been exploited to perform a sensitivity analysis showing that cell geometry variations have an important effect on statistical spread of key cell properties. Furthermore, electrical characteristics of a shrunk cell to the 32nm node could have been more reliably predicted pointing out the PCM scaling potential.

REFERENCES

[1] R. Bez, in *IEDM Technical Digest*, p. 89, 2009.
[2] A. Redaelli *et al.*, *Jour. of Appl. Phys.*, vol. 103, no. 11, p. 111101, 2008.
[3] A. Redaelli *et al.*, in *Proc. SISPAD Conference*, p. 279, 2005.
[4] F. Pellizzer *et al.*, in *Proc. VLSI Technology Symposium*, 2006.
[5] G. Servalli, in *IEDM Technical Digest*, p. 113, 2009.
[6] D. Kencke *et al.*, in *IEDM Technical Digest*, p. 323, 2007.
[7] S. Savransky *et al.*, in *Proc. MRS Symp.*, p. 1072, 2008.
[8] H.-K. Lyeo *et al.*, *Appl. Phys. Lett.*, vol. 89, no. 15, p. 151904, 2006.
[9] U. Russo *et al.*, *IEEE Trans. on Elec. Dev.*, vol. 55, no. 2, p. 506, 2008.