# Proposal of a Fitting Accuracy Metric suitable for Compact Model Qualification in all MOSFET Operation Regions

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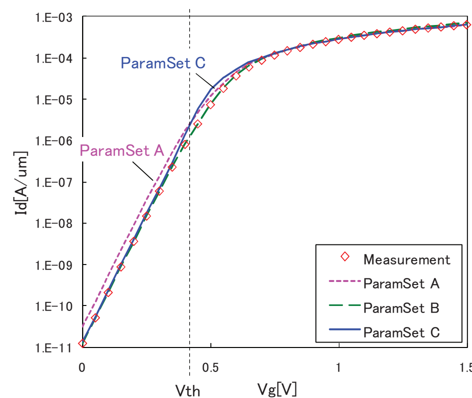
***Abstract*— Proposed is a fitting accuracy metric suitable for compact model qualification in all MOSFET operation regions. Fitting accuracy is quantified with a logarithmic deviation of simulated characteristics (such as current) from their measurement counterparts, normalized with the logarithmic deviation amplitude estimated with process-skewed parameters (corner model). The use of this new metric successfully captures, in all MOSFET operation regions, a "hot spot" where fitting accuracy is compromised. With this knowledge, circuit designers would be able to take a necessary precaution by adding a right amount of margin on top of existing ones.**

## I. INTRODUCTION

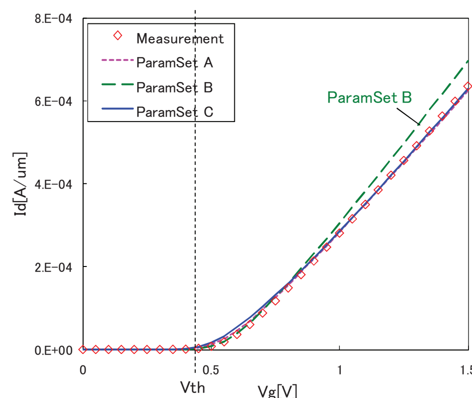
A compact model for SPICE simulation needs to play back device characteristics, such as current, accurately. Its accuracy relies both on a good description embodied by the model equations and a good choice of its model parameter set (model card). For a given compact model, the smaller the fitting error is, the better the parameter set is. Hence, an appropriate evaluation of fitting errors is crucial during model parameter extraction sessions. However, it is a rather difficult task because the drain current ($I_d$) of a MOSFET ranges widely from sub-pA to 1 mA (per channel width of 1 um); it varies exponentially with the gate bias voltage ($V_g$) in the sub-threshold bias region (below the threshold voltage ($V_{th}$)), while it varies rather modestly (i.e. linearly) in the inversion region.

To devise a fitting error indicator suitable for all operation regions needs a thoughtful care because a choice of error indicator may lead to a different judgment on which model card deserves a quality model. Suppose three model parameter sets (ParamSet A, B, and C) exhibit I-V characteristics (Figs. 1(a) and 1(b)). As drawn in Figure 1(a), ParamSet A exhibits the largest deviation from the measurement in the sub-threshold region (below $V_{th}$). As drawn in Figure 1(b), ParamSet B exhibits the largest deviation in the higher $V_g$ region. As evidenced in Figure 1(a), ParamSet C exhibits the largest deviation near the transition region where $V_g$ is near $V_{th}$.

In this setting, fitting errors of each model card are evaluated in several manners. When the absolute linear error ($error = I_{d,sim} - I_{d,meas}$, where $I_{d,sim}$ is $I_d$ simulated with a SPICE model, and $I_{d,meas}$ is the measured value) is used as error indicator, ParamSet A looks to fit best and ParamSet B fits poorest of the three (Fig. 2(a)). However, it may not be true when you look at ParamSet A exhibiting the largest deviation in the sub-threshold region (Fig. 1(a)). On the




(a)




(b)

Figure 1. (a) Logarithmic plot and (b) linear plot of $I_d$-$V_g$ of measured data and ParamSet A, B, and C

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other hand, when the linear percentage error ( $error = I_{d,sim}/I_{d,meas} - 1$ ) is used, you may judge ParamSet B looks best because the error is reasonably suppressed over the entire region, though not necessarily the smallest in the inversion region. ParamSet A still behaves poorly in the sub-threshold region and, however, gains accuracy in the inversion region (Fig. 2(b)). The similar goes for the logarithmic error ( $error = \log(I_{d,sim}) - \log(I_{d,meas})$ ) (Fig. 2(c)). A hybrid of the two error indicators, the logarithmic one for the sub-threshold region and the linear one for the inversion region, would be a contingency plan and would not, however, be a solution. Any of these indicators does not provide circuit designers with clear criteria which model card deserves quality model and whether deviations are large enough to doom circuit designs into failure.

These are why yet another good error indicator must be sought and it will be readily presented hereafter. In another words, the authors propose a fitting accuracy metric suitable for the compact model qualification in all MOSFET operation regions.

## II. Proposed Accuracy Metric

In the proposed accuracy metric, deviations of characteristics are quantified with the unit amplitude of deviation. The unit amplitude of deviation is estimated with a so-called corner model where process-skewed parameters are built in. The use of the unit amplitude arises from an engineering consideration as follows. Deviations of simulated characteristics from measurement may suffer less from design failure when the deviations are well confined within a certain range. As circuit designers usually use corner models to validate their designs, a "natural unit of length" is the difference of characteristics between the typical and corner models. In the sub-threshold region, for example, fitting accuracy would be easily compromised due to the region's exponential nature. However, as the unit amplitude of deviation tends to be larger there as well, fitting accuracy measured by the new metric can stay within a reasonable range. This gives a correct picture of fitting quality.

### *A. Constructing New Accuracy Metric*

Two types of compact model can be involved with the new metric. One compact model (Model I) is for an estimation of the characteristics deviation amplitude according to Equations (1) and (2). This model would be the same one as other model (Model II) used for circuit designs after parameter extraction. Model I needs to be able to predict accurately characteristics variations for process condition changes. For example, HiSIM2 [1] or the compact model proposed by Sakamoto, et al. [2] is qualified for Model I. These compact models have a good predictability of characteristics variations due to process condition change because the models are more physics-oriented than a certain class of compact model (such as a vth-based one) and their major model parameters correspond more directly to device technology such as channel doping profile.

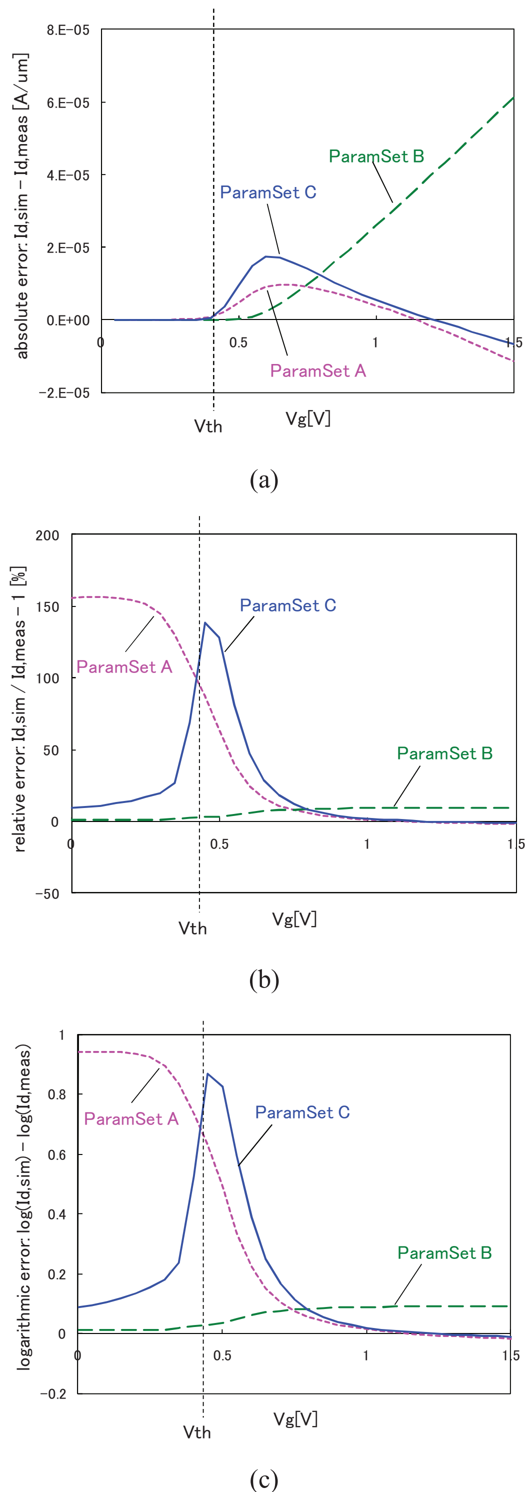



Figure 2. (a) Absolute linear error, (b) relative error, and (c) logarithmic error of ParamSet A, B, and C

$$\Delta logI_d = \sqrt{\Delta logI_{d,\Delta L}^{\;2} + \Delta logI_{d,\Delta W}^{\;2} + \Delta logI_{d,\Delta Tox}^{\;2} + \Delta logI_{d,\Delta Nsub}^{\;2}} \qquad \cdots(1)$$

$$\left.\begin{aligned}
\Delta logI_{d,\Delta L} &= \log\left(I_{d,sim(\mathrm{I})}(L-\Delta L, W, T_{ox}, N_{sub})\right) - \log\left(I_{d,typical}\right)\\
\Delta logI_{d,\Delta W} &= \log\left(I_{d,sim(\mathrm{I})}(L, W+\Delta W, T_{ox}, N_{sub})\right) - \log\left(I_{d,typical}\right)\\
\Delta logI_{d,\Delta Tox} &= \log\left(I_{d,sim(\mathrm{I})}(L, W, T_{ox}-\Delta T_{ox}, N_{sub})\right) - \log\left(I_{d,typical}\right)\\
\Delta logI_{d,\Delta Nsub} &= \log\left(I_{d,sim(\mathrm{I})}(L, W, T_{ox}, N_{sub}-\Delta N_{sub})\right) - \log\left(I_{d,typical}\right)
\end{aligned}\right\} (2)$$

$$I_{d,typical} = I_{d,sim(\mathrm{I})}(L, W, T_{ox}, N_{sub})$$

*1) Calculation of Characteristics Deviation*

First, the parameters of Model I are extracted. Its major parameters only will suffice for reproducing major measured characteristics of MOSFET such as $V_{th}$, $I_{doff}$ ($I_d$ at $V_g = 0$), and $I_{dsat}$ ($I_d$ at $V_g = V_{DD}$). The relevant parameters can be oxide thickness ($T_{ox}$), channel impurity concentration ($N_{sub}$), mobility (μ), and so on.

Next, the characteristics deviation is calculated at each bias point using Model I whose major process parameters --- gate length ($L$), gate width ($W$), $T_{ox}$, and $N_{sub}$ --- are skewed (Eqn. 2). Their amplitudes of skewing would be set from measured data, estimation from previous process generations, or prediction by TCAD simulation or theory, and are taken as the same as the ones used for constructing corner models. For example, the logarithmic $I_d$ deviation ($\Delta logI_{d,\Delta Nsub}$) calculated with skewed $N_{sub}$ using Model I is shown in Figure 3. The total logarithmic $I_d$ deviation ($\Delta logI_d$) is estimated at each bias point by Equation (1) with the logarithmic deviation of $I_d$ contributed by each process-skewed parameter. It is identified with the logarithmic difference of $I_d$ between the typical and a corner model.

*2) Definition of Fitting Error*

The fitting error ($error(i)$) for parameter extraction of Model II is defined at each bias point (denoted as $i$) as a logarithmic deviation of simulated $I_d$ from its measurement, normalized with $\Delta logI_d$ (Eqn. (3)).

$$error(i) = \frac{\log\left(I_{d,sim(\mathrm{II})}(i)\right) - \log\left(I_{d,meas}(i)\right)}{\Delta logI_d(i)} \quad \cdots(3)$$

Figure 4(a) shows $\Delta logI_d$ and the logarithmic error for ParamSet A, B, and C, each of which is a model parameter set of Model II, and Figure 4(b) shows each $error(i)$ for ParamSet A, B, and C, respectively. Figure 4(b) clearly shows where the fitting capability is most compromised by a certain model parameter set.

The total fitting error ($total_error$) for a model parameter set of Model II is defined as RMS (root mean square) of $error(i)$ (Eqn. (4)). A guiding principle is to make $total_error$ minimum as much as possible during the parameter extraction for Model II.

$$total_error = \sqrt{\frac{1}{N}\sum_i error(i)^2} \qquad \cdots(4)$$

$$N = \sum_i 1$$

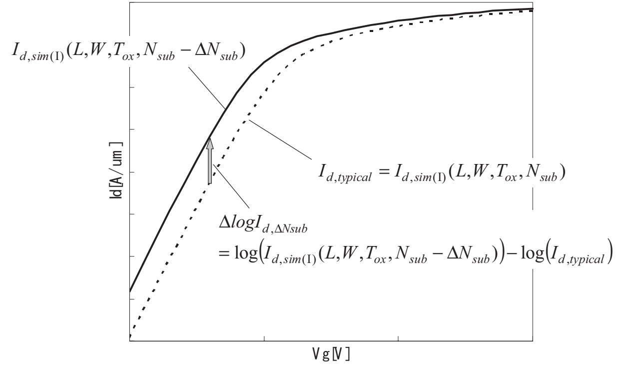
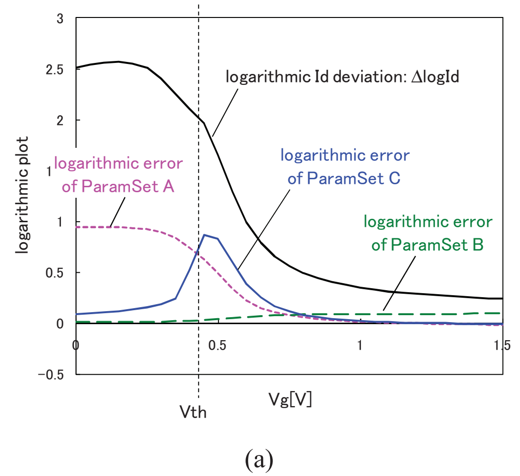
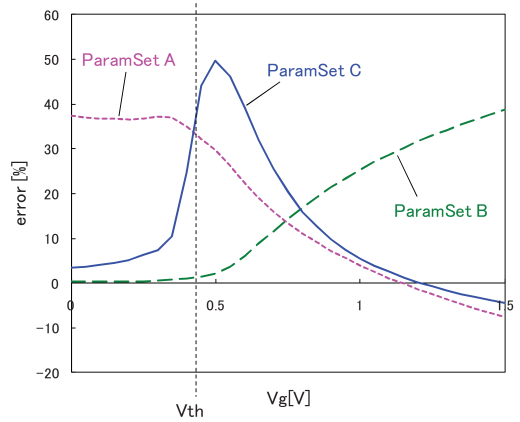



Figure 3. $I_d$ deviation calculated with skewed $N_{sub}$




(a)




(b)

Figure 4. (a) Logarithmic $I_d$ deviation and logarithmic error, and (b) fitting error of the proposed metric of ParamSet A, B, and C

## B. *Example of New Accuracy Metric*

Figures 5(a)-5(d) show how this new metric is applied to $I_d$-$V_d$ of an actual test device. The logarithmic error exhibits a peak near the bias point of $V_g$ = 0.2V and $V_d$ = 0.16V. However, it is too soon for circuit designers to identify the bias point as a hot spot; $\Delta logI_d$ is also large (Fig. 5(c)). Figure 5(d) clearly shows that near the bias point of $V_g$ = 1.2V and $V_d$ = 0.12V is a "hot spot" where fitting accuracy is most compromised, with the maximum error of about 8.5 % against the $I_d$ deviation of the corner model. The RMS error (*total_error*) is actually calculated as 2.4 % from Equation 4.

This knowledge would help circuit designers take a necessary precaution by adding a right amount of margin on top of the existing ones. One way to do this is to displace a corner model (denoted as solid circles in Fig. 6) by a certain offset because actual typical characteristics can be off-centered from the simulated ones due to fitting errors. The offset can be known from the fitting error measured by the new metric as was shown in Fig. 5(d). The offset can be treated as a guard-band that accommodates fitting errors. An additional simulation using such a modified corner model would preclude a possible design failure. A similar procedure can be applied to the prediction of worst-case circuit performances such as propagation delay time.

## III. CONCLUSION

Proposed was a fitting accuracy metric suitable for the compact model qualification in all MOSFET operation regions. Fitting accuracy is quantified with a logarithmic deviation of simulated characteristics normalized with the logarithmic deviation amplitude estimated with process-skewed parameters. The use of this new metric successfully captures, in all MOSFET operation regions, a "hot spot" where fitting accuracy is compromised. This knowledge would help circuit designers take a necessary precaution by adding a right amount of margin on top of existing ones.

## REFERENCES


[1] M. Miura-Mattausch et al., "HiSIM2: Advanced MOSFET Model Valid for RF Circuit Simulation", IEEE Trans. Electron Devices, Vol.53, No.9, pp. 1994-2007, 2006.

[2] H. Sakamoto, et al., "A Discrete Surface Potential Model which Accurately Reflects Channel Doping Profile and its Application to Ultra-Fast Analysis of Random Dopant Fluctuation", SISPAD 2009, pp. 95-98, 2009.

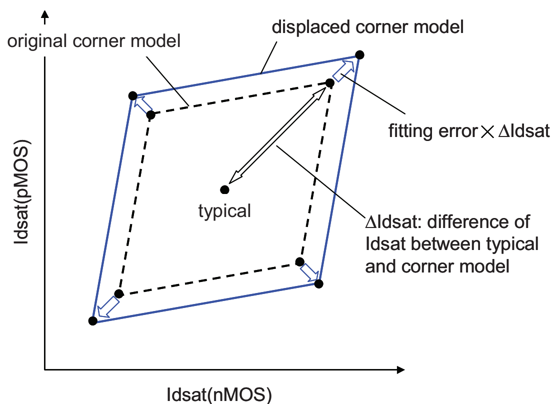




Figure 6. Displacing of a corner model

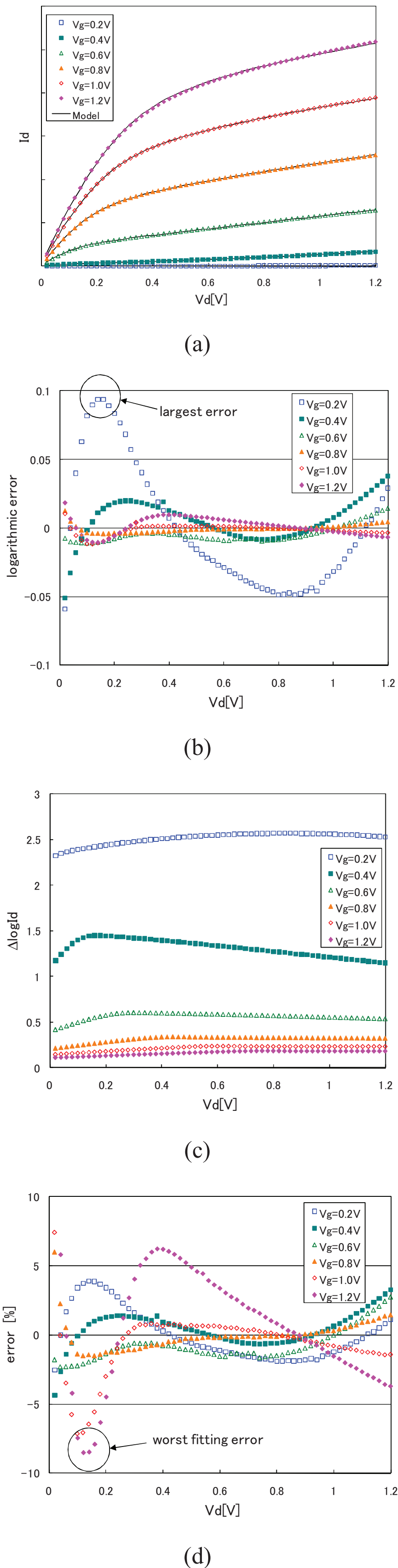



Figure 5. (a) Fitting result, (b) logarithmic error, (c) logarithmic $I_d$ deviation, and (d) fitting error of the proposed metric for $I_d$-$V_d$ of the test device