Compact Modeling of Fe-FET and Implications on Variation-Insensitive Design

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Abstract — Semiconductor devices with self-feedback mechanisms are considered as a promising alternative to traditional CMOS, in order to achieve faster operation and lower switching energy. Examples include IMOS and FBFET that are operated in a non-equilibrium condition to rapidly generate mobile carriers [1-2]. More recently, Fe-FET was proposed to improve the switching by integrating a ferroelectric material as gate insulator in a MOSFET structure [3-5]. Under particular circumstance, ferroelectric capacitance is effectively negative, due to the negative slope of its polarization-electrical field (P-E) curve. This property makes the ferroelectric layer a voltage amplifier to boost surface potential, achieving fast transition. In this paper:

(1) A new threshold voltage model is developed to capture the feedback of negative capacitance and IV characteristics of Fe-FET;

(2) It is further revealed that the impact of random dopant fluctuation (RDF) on leakage variability can be significantly suppressed in Fe-FET, by tuning the thickness of the ferroelectric layer.

Keywords — Fe-FET, Steep Subthreshold Slope, Compact Modeling, Random Dopant Fluctuation (RDF), Variation-Insensitive

I. INTRODUCTION

It is of significant importance to have a steep subthreshold slope because lower the supply voltage and hence the power dissipation can be achieved. However, in a traditional MOSFET, a fundamental limit of surface potential change of $2.3k_BT$ is required to modulate the subthreshold current by 10 times, which is known as Boltzmann tyranny [3]. New device structures such as IMOS and FBFET [1-2] are proposed to circumvent this limit. Moreover, Fe-FET is proposed by integrating ferroelectric material as a voltage amplifier in a traditional MOSFET structure to achieve the fast transition in subthreshold region [3-5].

On the other hand, the aggressive scaling of CMOS technology inevitably leads to a drastic challenge in process variations, such as channel length variation, channel dopant fluctuations, and other layout-dependent proximity effects. Among these variations, random dopant fluctuation (RDF) represents the intrinsic variation source in CMOS structure, posed by fundamental physical and manufacturing limits. RDF has become one of the most major barriers in the progress of large-scale integration scaling.

To enable the early-stage exploration of circuit design and better understand the impact on performance variability, it is necessary to develop an effective model that is able to physically capture the steep subthreshold slope and embed it into standard model parameters for circuit simulation. In this work, a new threshold voltage model of Fe-FET is proposed to capture the steep subthrehsold behavior. This model is derived from the first principle and physically captures the subthreshold behavior of Fe-FET such that model scalability is guaranteed for future technology generations. Moreover, it is found that the model implies Fe-FET is better immune to the RDF effect than the traditional MOSFET.

The paper is organized as following. Section II presents the compact model derivation for the varying threshold voltage with various gate voltages to describe the subthreshold behavior. In section III, the performance variability of Fe-FET is investigated by using the new threshold voltage model and TCAD simulation. Section IV concludes this paper.

II. COMPACT MODELING OF FE-FET

Fe-FET is proposed to speed up the transition by stacking a ferroelectric material on top of silicon dioxide as a voltage amplifier to boost surface potential in a MOSFET structure, as shown in the schematic in Fig. 1(a) [3]. Fig. 1(b) illustrates the equivalent capacitance model for a Fe-FET device, where the ferroelectric capacitance (C_{FE}) is in series with the oxide capacitance (C_{OX}) and the substrate capacitance (C_S). V_{int} denotes the internal voltage between C_{FE} and C_{OX}. The negative capacitance of the ferroelectric dielectric originates

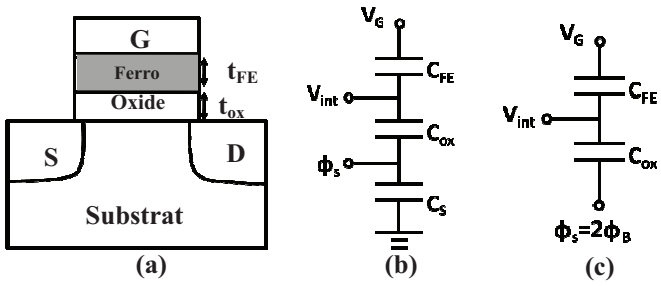

Figure 1. (a) Cross-section of Fe-FET. (b) The equivalent capacitance model in the sub-V_{th} region (c) The capacitance model in the super-V_{th} region.

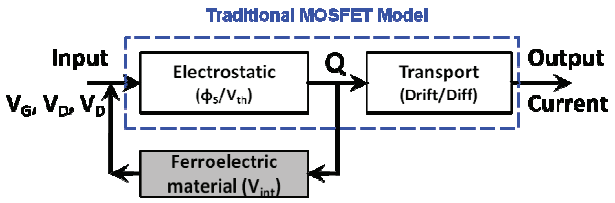

Figure 2. The integration of the ferroelectric material into traditional MOSFET model.

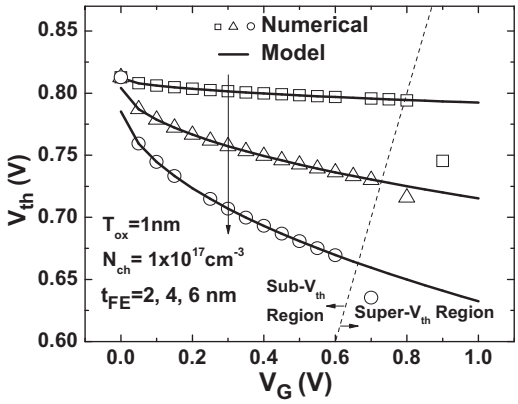

Figure 3. The dependence of V_{th} on gate voltage and t_{FE}.

from the intrinsic feedback mechanism between the induced charge and the voltage drop on the capacitance; it is modeled by inserting an additional feedback path in traditional CMOS model, as shown in Fig. 2. This feedback between charge and voltage drop is modeled by Eq. (1) [4],

$$V_g - V_{\text{int}} \approx \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 + \rho_0 \frac{dQ}{dt} \tag{1}$$

where α_0 and β_0 are negative to account for the negative capacitance. γ_0 is positive to describe the behavior of normal capacitance. ρ_0 is the resistivity for the voltage drop. Those parameters (α_0, β_0, γ_0, and ρ_0) are proportional to the thickness of ferroelectric dielectric (t_{FE}), and are modeled in Eqs. (2)-(5),

$$\alpha_0 = 2\alpha t_{FE} \tag{2}$$

$$\beta_0 = 4\beta t_{FE} \tag{3}$$

$$\gamma_0 = 6\gamma t_{FE} \tag{4}$$

$$\rho_0 = \rho\ t_{FE} \tag{5}$$

where α, β, γ and ρ are material coefficients of the ferroelectric dielectric. The internal voltage (V_{int}), which accounts for the change of voltage drop in C_{FE}, is formulated in Eq. (6).

$$V_{\text{int}} = \phi_s + \frac{\sqrt{2\varepsilon_{si} q N_{ch} \phi_s}}{C_{ox}} \tag{6}$$

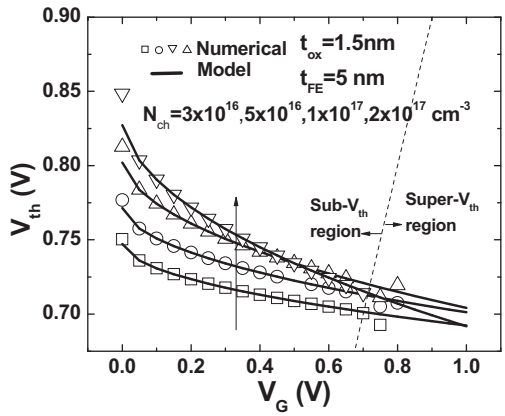

Figure 4. The dependence of V_{th} on gate voltage and N_{ch}.

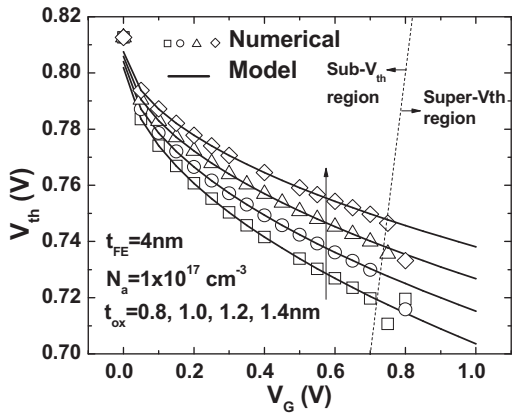

Figure 5. The dependence of V_{th} on gate voltage and t_{ox}.

By combining Eqs. (1)-(6) and ignoring the high order effects, the surface potential (Φ_S) in the subthreshold region is expressed in Eqs. (7) and (8) in a steady state.

$$\phi_s = \left(\frac{-A + \sqrt{A^2 + 4V_g}}{2} \right)^2 \tag{7}$$

$$A = \sqrt{2\varepsilon_{si} q N_{ch}} \cdot \left(\frac{1}{C_{ox}} + \alpha_0 \right) \tag{8}$$

Moreover, to the first order, the threshold voltage (V_{th}) is derived as a function of gate voltage and surface potential, as shown in Eq. (9) [6].

$$V_{th} = V_g + 2m\phi_B - m\phi_s \tag{9}$$

Eqs. (7)-(9) describe the closed-loop behavior of V_{th} in Fe-FET, which is adaptively changed with various gate voltages. To achieve faster transistor switching, V_{th} should vary dynamically toward a smaller value when gate voltage is increasing. Therefore, the sum of ($1/C_{ox} + \alpha_0$) needs to stay below zero, which ensures the negative derivative of V_{th} with respect to V_G (i.e., dV_{th}/dV_G), as shown in Eq. (10).

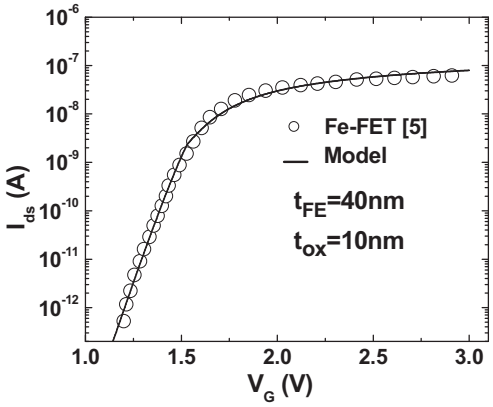

Figure 6. The matching between model prediction and measurement data [5].

$$\frac{\partial V_{th}}{\partial V_G} = 1 - \left(\frac{-A + \sqrt{A^2 + 4V_G}}{\sqrt{A^2 + 4V_G}} \right) \tag{10}$$

The negative value of $(1/C_{ox} + \alpha_0)$ indicates that the series capacitance of C_{FE} and C_{ox} is negative. In this situation, the system could be stable in the subthreshold region as long as the total capacitance in series (Fig. 1(b)) is positive. However, when the channel is formed, i.e., the surface potential is fixed at $2\Phi_B$, the inversion layer shields C_s and thus, the device could become unstable if the series capacitance of C_{FE} and C_{OX} remains negative, as shown in Fig. 1(c).

The values of material coefficient are calibrated with experimental data in [5], where α is estimated roughly at the order of -10^{10}m/F. Fig. 3 shows the threshold voltage decreases at higher gate voltage. A stronger declining rate of V_{th} is observed when a thicker t_{FE} is applied. Note that the V_{th} model is only applicable in the subthreshold region. Fig. 4 shows V_{th} decreases with increasing V_g at various channel doping concentrations (N_{ch}). As N_{ch} increases, V_{th} decreases faster at larger V_G, presenting a more rapid switching behavior in the subthreshold region. Fig. 5 shows the dependence of V_{th} on gate bias when oxide thickness is varying. With thinner t_{ox}, V_{th} goes down more rapidly bias at higher V_G, further

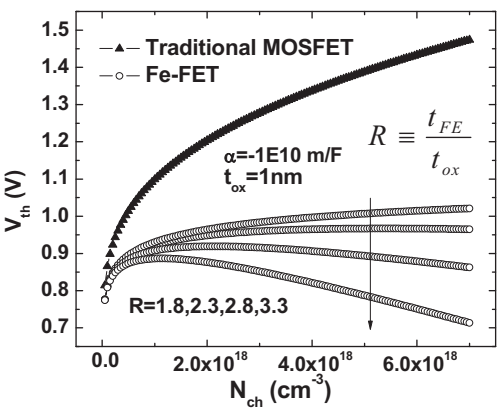

Figure 7. Dependence of V_{th} on N_{ch}. With the intrinsic feedback mechanism, V_{th} can be tuned to be insensitive to channel doping.

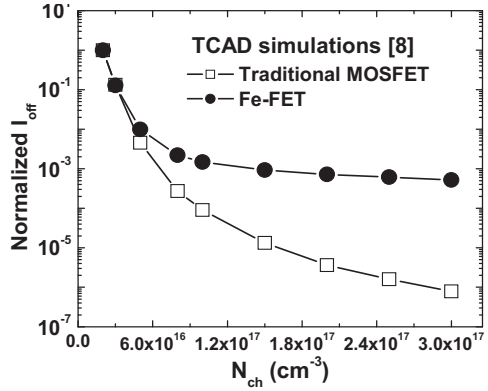

Figure 8. TCAD simulation of normalized off-state current for traditional MOSFET and Fe-FET.

benefiting the faster transition. Finally, Fig. 6 shows the agreement between model-predicted IV and published data [5].

III. Implications on Performance Variability

Different from traditional MOSFET, there is an intrinsic feedback path in Fe-FET (Fig. 2). Exploiting the positive feedback reduces the subthreshold swing [5]. Furthermore, the loop of feedback implies that the sensitivity of device performance to certain parameters could be suppressed, if the

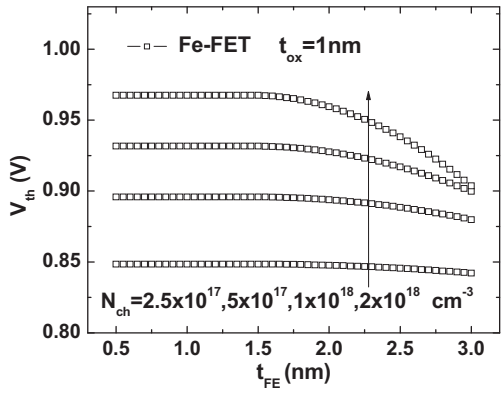

Figure 10. Dependence of V_{th} on t_{FE} and N_{ch}. Higher N_{ch} increases t_{FE}-induced V_{th} variation.

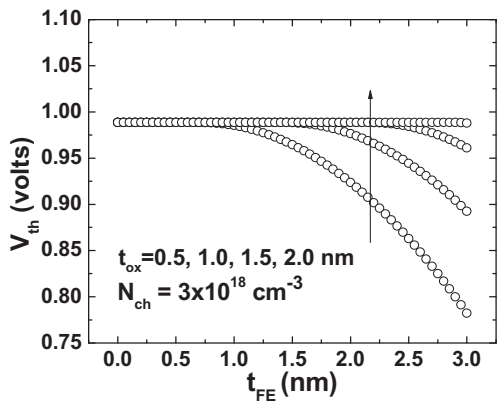

Figure 9. Dependence of V_{th} on t_{FE} and t_{ox} in Fe-FET. Higher t_{ox} suppresses t_{FE}-induced V_{th} variation.

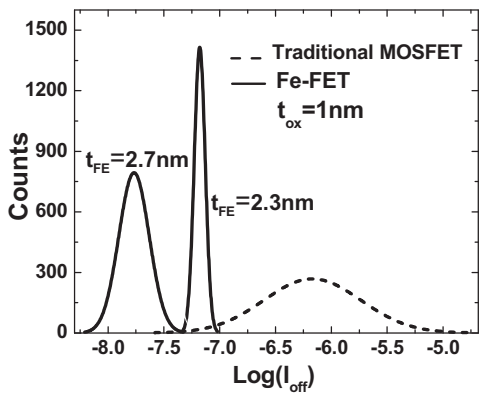

Figure 11. The off-state current distribution under RDF, with the same on-current.

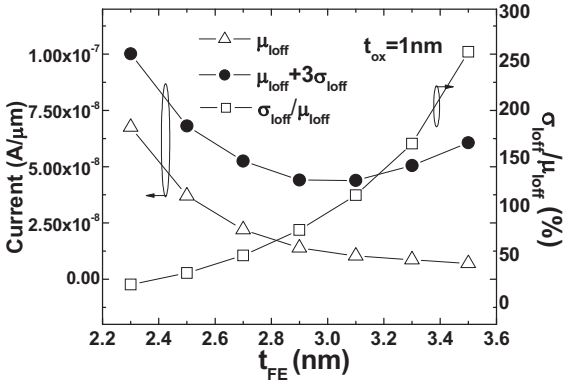

Figure 12. The mean value (μ_{Ioff}), standard derivation (σ_{Ioff}), and the worst case (μ_{Ioff}+ 3σ_{Ioff}) of off-state current, at a fixed on-state current.

feedback strength is appropriately tuned by Eq.(8). The device performance becomes more stable under microscopic variations. Based on TCAD and the new model, this section investigates this phenomenon, particularly on random dopant fluctuations (RDF) [7].

Fig. 7 confirms that V_{th} of Fe-FET is less sensitive to the dopant fluctuation than that in traditional MOSFET. Moreover, the sensitivity of V_{th} to N_{ch} can be modulated by the thickness of ferroelectric layer (t_{FE}). A larger t_{FE} leads to a stronger feedback path that compensates the RDF effect. TCAD simulation is further performed to validate this effect [8]. Using TCAD tools, the dielectric constant of the gate insulator is modified to a negative value to simulate the effect of negative capacitance. In Fig. 8, TCAD simulation results compare the normalized off-state current between traditional MOSFET and Fe-FET, with various conditions of channel doping concentration. It is observed that the dependence on N_{ch} becomes weaker with a negative capacitance applied, implying that Fe-FET helps suppress the RDF effect.

Figs. 9 and 10 further study this behavior under various t_{FE}, t_{ox}, and N_{ch}. V_{th} of Fe-FET changes with t_{FE} and a thicker oxide thickness reduces t_{FE}-induced V_{th} variation as shown in Fig. 9. Fig. 10 illustrates that lower channel doping concentration also reduces the t_{FE}-induced variation. Thus, lower N_{ch} and thicker t_{ox} improve device robustness; meanwhile, with a weaker feedback, the transition is degraded.

The reduction in V_{th} variability directly decreases the distribution of the off-state current (I_{off}) under RDF. Fig. 11 shows this effect for 45nm Fe-FET and traditional MOSFET, at the same on-state current (I_{on}). As t_{FE} decreases to 2.3nm (the least dependence on N_{ch} in Fig. 7), the standard deviation (σ_{Ioff}) is minimized. When t_{FE} further increases, the subthreshold slope becomes steeper and thus, a lower I_{off} is achieved; however, a thicker t_{FE} leads to a larger I_{off} fluctuation (Fig. 11). Fig. 12 illustrates that as t_{FE} increases, the mean value (μ_{Ioff}) decreases due to stronger positive feedback, while σ_{Ioff} increases. A balance between t_{ox} and t_{FE} helps achieve the minimum worst case I_{off} (μ_{Ioff}+3σ_{Ioff}).

IV. Conclusion

A new compact model of Fe-FET is developed, by adding a feedback path for the ferroelectric layer. It is scalable with technology specifications. Based on the model, it is revealed that a thicker ferroelectric material, higher channel doping, and thinner oxide thickness improve the transition in the subthreshold region. On the other hand, a balance between the feedback and feedthrough paths helps stabilize device performance under the RDF effect.

V. Acknowledgement

The authors would like to acknowledge the support of the Interconnect Focus Center (IFC), one of five research centers funded under the Focus Center Research Program, a Semiconductor Research Corporation Program.

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