Modeling of 2D Bias Control in Overlap Region of High-Voltage MOSFETs for Accurate Device/Circuit Performance Prediction

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***Abstract*— High-voltage MOSFETs enable wide bias-range applications realized only by optimizing the device structure. We have developed the compact model HiSIM_HV 2.0.0, based on the potential distribution in the device, which is useful for both device and circuit optimizations. By considering two device-structure dependent potentials, the internal node potential within the high resistive drift region and the potential underneath the gate overlap region, the model can reproduce *I-V* characteristics for a wide range of structure variations without additional fitting parameters.**

I. INTRODUCTION

For realizing ecology-friendly low-loss energy control, power devices play an important role. Among them high-voltage (HV) MOSFETs are most widely used in the range from a few volts up to several hundred volts and are realized by adding only an optimized resistive drift region to the basic MOSFET structure (Fig. 1, asymmetric LDMOS structure) [1-3]. The most important task for a HV-MOSFET model is to correctly capture the resistance effect of the highly resistive drift region. For this purpose a linear potential drop within the drift region was approximated previously [4,5]. However, many fitting parameters are needed in this previous approach to reproduce the *I-V* characteristics for a wide range of applied bias variations. Here our task is to develop a predictable HV-MOSFET model for device/circuit optimization. It is demonstrated that the overlap region, where 2D bias control occurs, determines the current flow within the drift region. The observed 2D current flow can be modeled with 2 structure-internal potential values (ϕ_{s_over}, V_{dps}), obtained by solving the Poisson equation and the continuity equation separately.

II. METHOD AND RESULTS

Potential distributions within the HV-MOSFET are shown in the lower part of Fig. 1 together with the schematic HV-MOSFET structure. Most of the potential difference, applied between source and drain contacts, is consumed within the drift region. For including the drift-region effect, we develop a diffused resistor model which considers the potential at the internal node V_{dps} and the terminal drain voltage V_{ds} as shown in Fig. 2a. Fig. 2b shows 2D-device simulation results of the *I-V* characteristic as a function of the potential difference V_{ddp} (=V_{ds}-V_{dps}) with different assumptions for the saturation velocity v_{sat}. It can be seen that reduced v_{sat} results in substantial deviation from a linear Ohmic dependence, resulting in similar *I-V* characteristics as observed for MOSFETs. Calculation results of the developed model are also depicted in Fig. 2b by lines. Model equations used for the calculation are

$$I_{ddp} = W_{eff\_LD} \cdot x_{ov} \cdot q \cdot n \cdot \mu_{drift} \cdot \frac{V_{ddp}}{L_{drift} - RDRDL1}, \quad (1)$$

$$\mu_{drift} = \frac{RDRMUE}{\mu V} \;;\; \mu V = \left(1 + \frac{RDRMUE}{RDRVMAX} \cdot \frac{V_{ddp}}{L_{drift}}\right) \quad (2)$$

q: elementary charge

where the carrier concentration n is approximated to be N_{drift}, and x_{ov} in Eq. (1) is approximated to be equal to x_{res}. It is seen that the model-calculation results deviate slightly from the 2D-device simulation results, namely the simulated *I-V* characteristics never reach the saturation condition, which is different from conventional MOSFETs. Fig. 3 illustrates the reason for the growing current even under already high V_{ddp} condition. The velocity saturation (see Fig. 3b) occurs beyond much smaller V_{ddp} values than the quasi-saturation of the current I_{ddp} (see Fig. 3a). Thus the main cause for continuously growing I_{ddp} can be attributed to the increase of the carrier concentration with increased V_{ddp} as depicted in Fig. 3b. The reason for the carrier increase is the carrier accumulation at the surface. This growth of the carrier concentration is modeled as

$$n = N_{drift}\left\{1 + RDRCAR \cdot \frac{V_{ddp}}{L_{drift} - RDRDL2}\left(1 - \frac{1}{\mu V}\right)\right\}. \quad (3)$$

Introduced model parameters are summarized in Table I with their physical meanings. By taking into account the growth of the carrier concentration according to Eq. (3), the simulated I_{ddp}-V_{ddp} result is well reproduced as shown in Fig.4.

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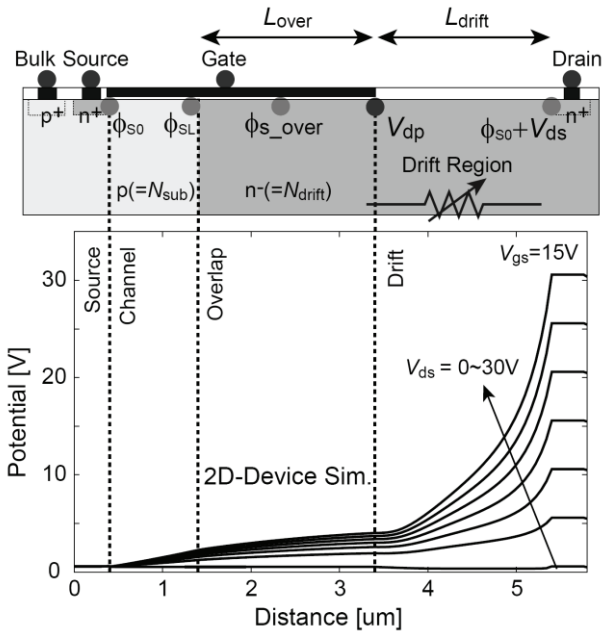

Fig. 1. Studied HV-MOSFET structure and the internal potential distribution along the device in horizontal direction.

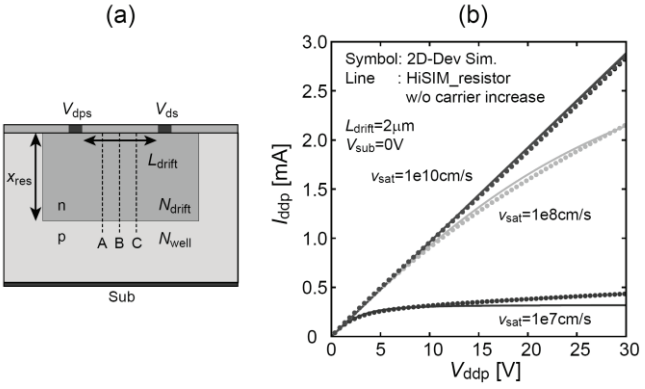

Fig. 2. 2D-device simulation results. (a) Studied resistor structure and (b) *I-V* characteristics as a function of the potential difference V_{ddp} for various saturation velocity v_{sat} values.

TABLE I. MODEL PARAMETERS USED IN THE DEVELOPED MODEL

RDRMUE	mobility in drift region
RDRVMAX	max velocity in drift region
RDRCAR	high field injection
RDRCX	current exudation coefficient
RDRDL1	modification of L_{drift} length
RDRDL2	length of pinch-off region

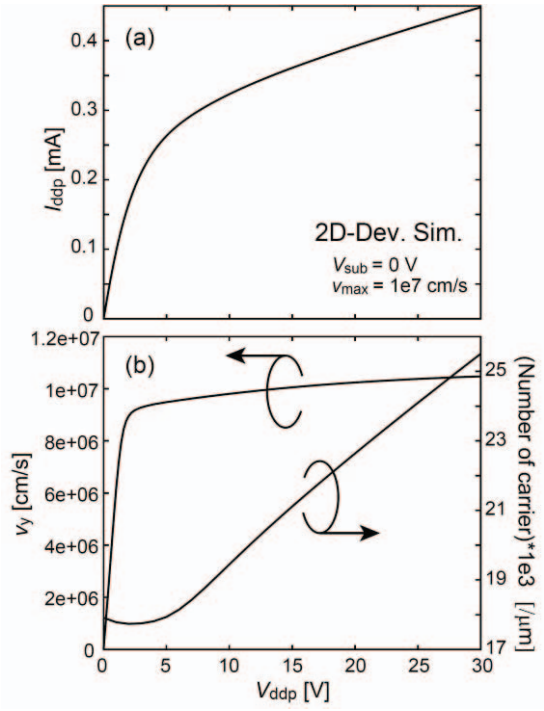

Fig. 3. 2D-device simulation results of the studied resistor for the v_{sat}=1×10^7 cm/s case in Fig. 2b. (a) I_{ddp}-V_{ddp} characteristic, (b) velocity v_y and carrier concentration.

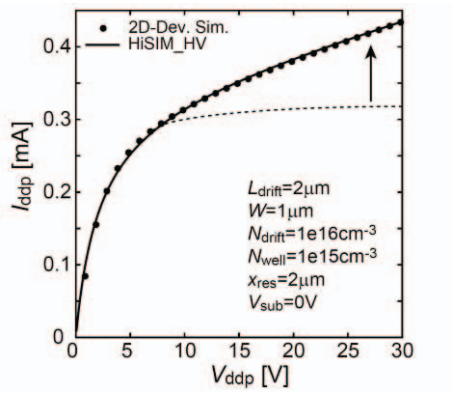

Fig. 4. The same comparison as shown in Fig. 3a for v_{sat}=1e7cm/s with inclusion of the carrier concentration increase according to Eq. (3).

In addition to the diffused resistor case, the HV-MOSFET provides a third electrode, namely the gate electrode, which controls the injected carrier concentration into the V_{dps} terminal of the resistor. We focus here on the task of how to incorporate the gate control into the resistor model. Fig. 5 compares 2D-device simulation results of the current flow for different V_{gs} values. The current-flow path stays at the surface for large V_{gs}. This modification of the current flow due to changes of V_{gs} is governed by two depletion widths formed in the overlap region as shown in Fig. 6. To model this current-flow modification, 2 bias dependent depletion widths, W_{junc} induced at the channel/drift junction and W_{dep} induced underneath the gate oxide, must be considered. W_{junc} is calculated with the

potential difference between V_{bs} and V_{dps} (see Fig. 1) and W_{dep} is calculated from the surface potential in the overlap region ϕ_{s_over}. The accumulation charge, induced underneath the overlap region, enhances the diminishing process of W_{dep}. The final current width x_{ov} for the drift-region-resistance model, the current-flow-path created between W_{junc} and W_{dep}, is modeled as shown in Fig. 6. Developed compact-model equations are

$$x_{ov} = W_0 - RDRCX\left(\frac{W_0}{D_{junc}}W_{dep} + \frac{W_0}{L_{over}}W_{junc}\right), \quad (4)$$

$$W_0 = \sqrt{{L_{over}}^2 + {D_{junc}}^2}, \quad (5)$$

$$W_{dep} = \sqrt{\frac{2\varepsilon_{si}\left(V_{dps} - \phi_{s\_over}\right)}{q \cdot N_{drift}}}, \quad (6)$$

$$W_{junc} = \sqrt{\frac{2\varepsilon_{si}\left(\phi_{bi} + V_{dps} - V_{bs}\right)}{q} \cdot \frac{N_{sub}}{N_{drift}(N_{sub} + N_{drift})}}. \quad (7)$$

D_{junc} : junction depth at the channel/drift region
ε_{si} : semiconductor permittivity
ϕ_{bi} : built-in potential

Fig. 7 compares calculated W_{dep} and W_{junc} with 2D-device simulation results verifying fairly good agreement.

The potential calculation within the channel is done by solving the Poisson equation iteratively. The further potential increase within the drift region is calculated by using the continuity requirement for the currents within the channel I_{ds} and the drift region I_{ddp}. Compact-model results for the *I-V* characteristics are compared with 2D-device simulation results in Fig. 8. Fig. 9 verifies the prediction capability of the HiSIM_HV simulation result, shown in Fig. 8b, for an extended bias range.

An advantage of the LDMOS structure is that the breakdown voltage can be controlled simply by adjusting the L_{drift} length. Fig. 10 shows 2D-device simulation results of the *I-V* characteristics and the extracted breakdown voltage V_{break} for different V_{gs} and L_{drift} values (D1, D2, D3, D4). Fig. 11 compares the *I-V* characteristics of the studied 4 L_{drift} length. Good agreement confirms the availability of scaling properties to different L_{drift} lengths. In addition to high accuracy, very stable circuit simulation without sacrificing simulation speed is achieved.

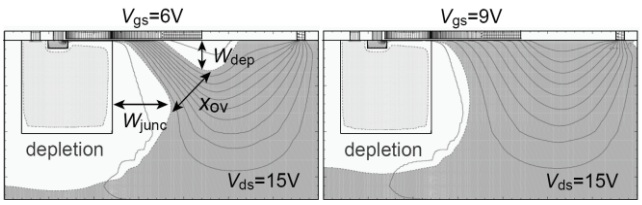

Fig. 5. 2D-device simulation results of the current flow for two V_{gs} values as V_{ds}=15V. Contour lines show the current density distribution.

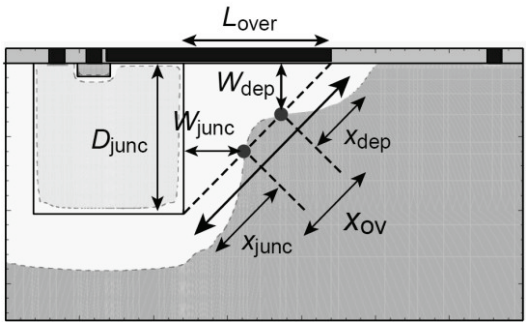

Fig. 6. Modelling of the 2D bias control in the overlap region. Two depletions widths W_{junc} and W_{dep}, shown in white colour, are induced by V_{gs}, V_{dps}, V_{bs} as well as the surface potential ϕ_{s_over} as in the overlap region.

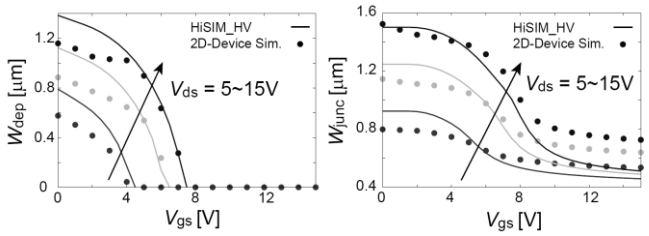

Fig. 7. Comparison of W_{dep} and W_{junc} caluculated with the developed compact-model and 2D-device simulation results.

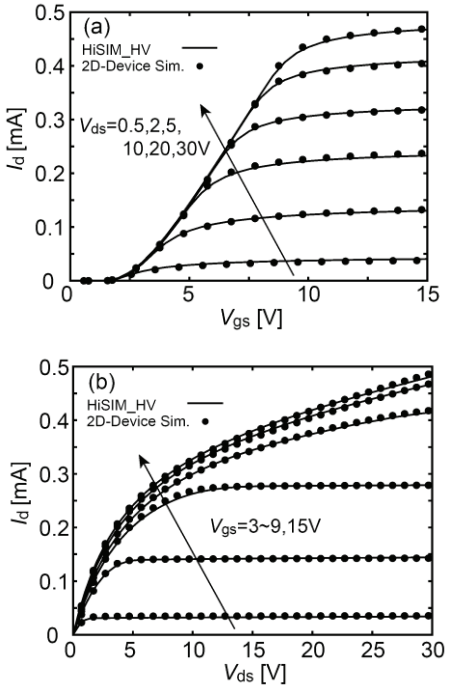

Fig. 8. Comparison of *I-V* characteristic obtained with 2D-device simulation results and the developed compact model. (a) as a function of the gate voltage V_{gs} and (b) as a function of the drain voltage V_{ds}.

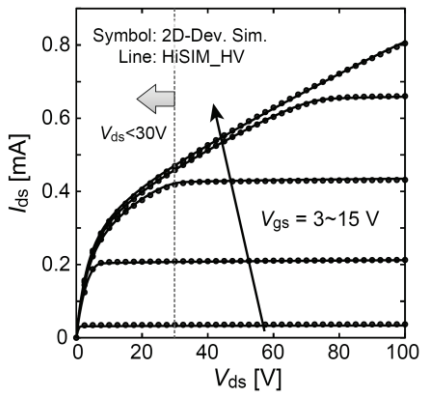

Fig. 9. Verification of the HiSIM_HV prediction capability beyond the fitted bias condition-region of V_{ds}<30V.

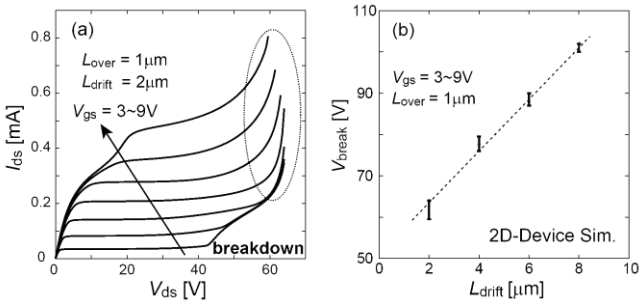

Fig. 10. 2D-device simulation results. (a) I_{ds}-V_{ds} characteristics for different V_{gs} values and (b) extracted breakdown voltage V_{break}. Vertical bars in (b) denote the variation of V_{break} for different V_{gs} values.

III . CONCLUTION

The complicated structure dependent *I-V* characteristics of the HV-MOSFETs are well reproduced by a physical compact-modelling concept with only six parameters for drift-region-resistance modelling. Prediction capabilities of the compact model beyond the region of fitted bias conditions could be confirmed. Compact-model scalability with the drift-region-length parameter was also verified. Furthermore, the circuit-simulation need of high simulation speed is not sacrificed.

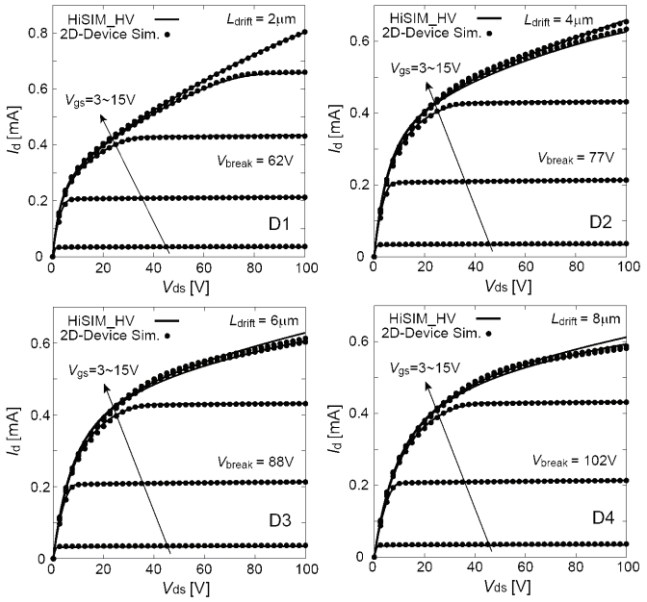

Fig. 11. Comparison of *I-V* characteristics obtained with 2D-device simulation and with the developed compact model without any additional fitting parameters. For the comparison no impact ionization is included, and there the breakdown is not modeled.

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