Investigation of Charge Loss Mechanisms in Planar and Raised STI Charge Trapping Flash Memories

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***Abstract*—A comprehensive simulation to investigate the charge loss mechanisms in planar and raised STI NAND-type charge trapping flash (CTF) memories with careful calibrations is present. The tunneling and silicon nitride trap transport with Poole-Frenkel (PF) effect are solved self-consistently and validated based on the experimental data including gate stacks leakage, program speed, and high temperature retention. Based on the programmed state, the high temperature retention is simulated and compared with the measurement data. In planar CTF, the vertical charge loss through tunneling layers and blocking layers are analyzed. The results show that the former is the dominant one. Finally, the charge loss in raised STI CTF is compared with that in planar CTF. The results show that the enhanced charge loss in raised STI CTF is induced by the lateral spreading and the non-uniform charge storage nearby the STI edge, especially in the narrow width (100nm) raised STI CTF.**

I. INTRODUCTION

CTF memories have attracted tremendous attention, both theoretically and experimentally, as one of the promising candidate to overcome the disadvantage of conventional floating gate NAND flash memories, which have several scaling challenges beyond the 45-nm technology node [1, 2]. The cell to cell coupling is drastically reduced by using silicon nitride storage layer instead of polysilicon floating gate. The effect of stress induced leakage current (SILC) is neglectable since the charge is stored on the localized trap site. The effect of back tunneling from gate is eliminated by using optimized blocking layers and gate materials [3]. The enhanced hole tunneling for erase operation by tunneling layer engineering makes it possible to have a trade-off between improving the erase speed and still keeping a good retention [4].

However, charge redistribution causes critical reliability issues in CTF memories [5]. The electron and hole are mostly stored locally after they tunnel into the silicon nitride. Thus, the uniformity of tunneling is critical for the threshold voltage controlling. In a NAND array, due to the existence of the STI edge, the tunneling and trapping tend to be non-uniform. This gradient distribution of trapped charge generates a lateral electric field, which makes the lateral redistribution worse. Additionally, the electron and hole mobilities in silicon nitride are different. A lateral dipole with trapped electron and hole after program/erase cycles will enhance the lateral charge redistribution [1]. Moreover, worse degradation is happened in tunneling layers by using the enhanced hole tunneling for erase operation, as hole capturing by bond reduces the bond energy for bond breakdown [6]. These all make the charge retention, especially high temperature retention a big challenge for CTF memories.

In this work, we perform a comprehensive simulation to reveal the charge loss mechanisms in planar and raised STI CTF. The simulation is based on the validation of gate stacks leakage, program speed and high temperature retention. In planar CTF devices, we compare the vertical charge loss through tunneling layers and blocking layers. The electron de-trapping from the trap sites and the following drift to the silicon nitride/tunneling layers or blocking layers interface are included at the same time. In raised STI CTF, STI edge effect on the threshold voltage controlling with non-uniform tunneling is discussed. Based on the programmed state, the vertical charge loss and lateral spreading are compared.

II. PHYSICAL MODEL AND STRUCTURE

For high temperature retention of CTF memories with program/erase cycles, the trapped charges not only on the silicon nitride traps but also on the generated traps in tunneling layers by program/erase cycles will be involved in the charge loss mechanisms. In order to remove these disturbances, we just consider the high temperature retention without program/erase cycles.

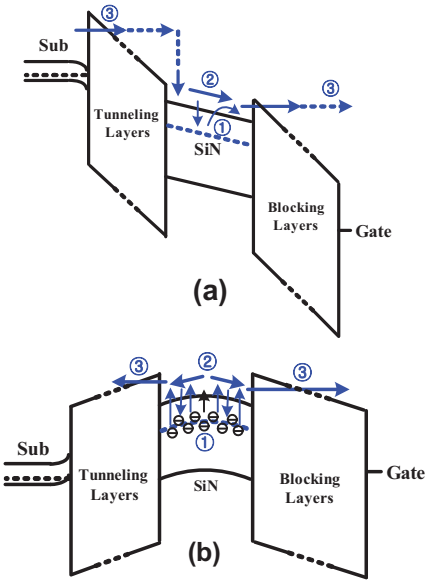

Fig. 1. Band diagram during (a) gate stacks leakage or program operation, (b) retention. The models include: ① trapping and de-trapping with PF enhanced emission ② drift transport ③ barrier tunneling.

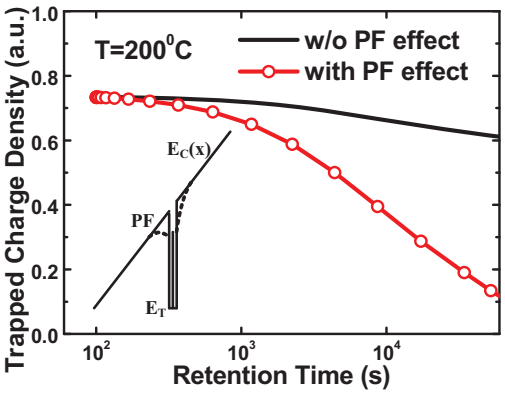

Fig. 2. PF enhanced emission effect on the trapped charge density during high temperature retention.

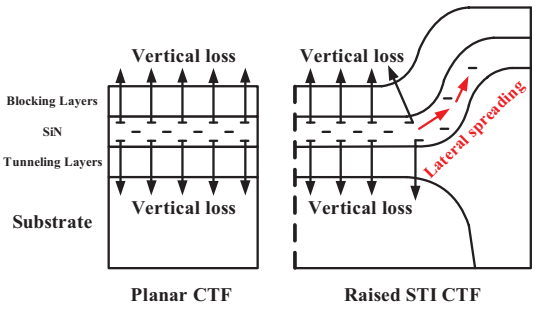

Fig. 3. Planar and raised STI CTF structures. The lateral spreading is another important charge loss mechanism for raised STI CTF.

The main physical models are shown in Fig. 1 [7-10]. Tunneling and nitride transport are solved self-consistently. The barrier tunneling covers FN and DT components, which are dependent on the band barrier and bending [11]. Tunneling through tunneling layers and blocking layers is taken into account. For high temperature retention, de-trapping from the trap sites is the main mechanism [7]. The trap-assisted tunneling through the trap sites in tunneling layers or blocking layers is not taken into account since it only contributes a little charge loss, especially for no cycle high temperature retention. Trap-to-band tunneling is also not considered, which is important for room temperature retention. The charge transport in nitride includes drift in the conduction band and charge trapping/de-trapping based on the thermal emission from the trap site. The PF model is used for the de-trapping enhancement. As shown in Fig. 2, PF effect reduces the barrier which the trapped charge need emit by the local electric field. Thus, the de-trapping rate will increase. Planar and raised STI CTF devices with tunneling layers/silicon nitride/blocking layers are shown in the Fig. 3. Planar CTF is used for the gate stacks leakage and program speed simulation. The high temperature retention simulation is performed for the both structures.

As shown in the Fig. 1, electron tunneling from the substrate to silicon nitride through tunneling layers is the source flux of the gate stacks leakage. During drifting to the blocking layers, some of the tunneled electron will be captured by the traps, and the others will arrive at the silicon nitride/blocking layers interface, then tunnel out to the gate. The gate stacks leakage will depend on not only the tunneling in/out fluxes but also the trapping/de-trapping and drift in silicon nitride. Fig. 4 (a) shows a good agreement between the simulation and measurement data by carefully tuning the tunneling and trap parameters.

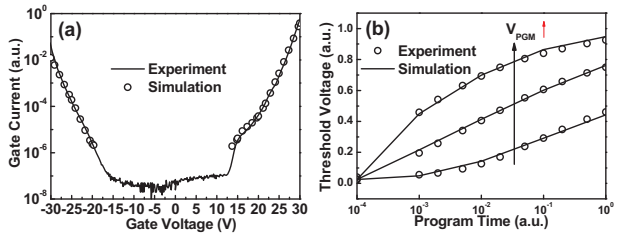

Fig. 4. Measured and simulated (a) gate stacks leakage and (b) program speed of planar CTF.

The physics during program operation is similar to that of gate stacks leakage except for the different operation time. The program voltage pulse has an increasing, flat and decreasing region with time $0.1t_{write}$, $0.9t_{write}$ and $0.1t_{write}$, respectively. The validation of program speed is shown in Fig. 4 (b). The simulation matches the measurement data well for three program voltages.

III. RESULT AND DISCUSSION

The electron emitted from the trap site transports to the interface between silicon nitride/tunneling layers or silicon nitride/blocking layers and then tunnels out. The two vertical charge loss components in planar CTF are plotted in Fig. 5. The vertical loss through tunneling layers is found to be the dominant one in the simulated planar structure. The electric field distribution after different retention time is plotted in the Fig. 6 (a). The longer retention time means more charge loss. Then the electric field is reduced within the whole gate stacks. And electric field in tunneling layers is larger than that in blocking layers. As a result, the tunneling rate through tunneling layers is much larger than that through blocking layers as shown in the Fig. 6 (b).

The simulated retention of planar CTF is shown in the Fig. 7 and matches the measurement data well with two programmed threshold voltages.

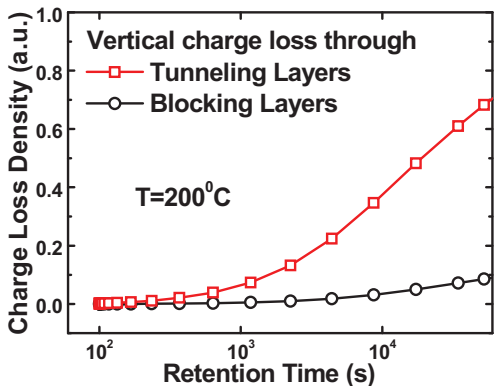

Fig. 5. Vertical loss through tunneling layers and blocking layers. The charge loss through tunneling layers is dominant.

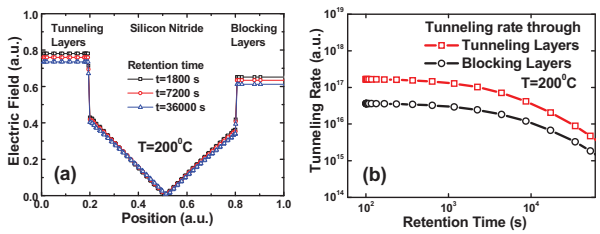

Fig. 6. (a) Electric field distribution after different retention time. (b) Tunneling rate through tunneling and blocking layers during high temperature retention.

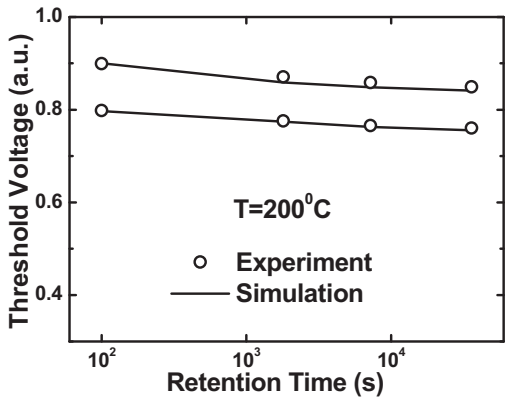

Fig. 7. Measured and simulated charge retention of planar CTF with two programmed threshold voltages.

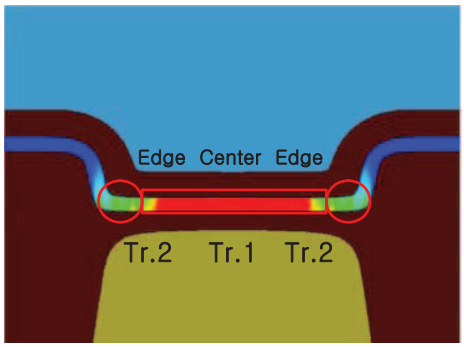

Fig. 8. Non-uniform trapped charge for programmed state in raised STI CTF, which induces an internal lateral electric field. Tr.2 nearby the edge reduces the whole device's threshold voltage.

For raised STI CTF, the programmed state is also used as the initial condition for high temperature retention. The device is separated to be one center (Tr.1) region and two STI edge (Tr.2) regions. As shown in Fig. 8, due to the non-uniform tunneling efficiency nearby the STI edge and local trapping, there is a gradient distribution of the trapped charge. This gradient will induce an internal lateral electric field and also the Tr.2 has a lower threshold voltage. The whole device's threshold voltage will be reduced. The reduction for smaller width device is significant. IdVg curves of 10um and 100nm width devices after different program times are plotted in Fig. 9. A humping shape is shown for the 10um width device, which reveals the channel conductivity controlled by Tr.1 or Tr.2. Note that the constant current which decides the threshold voltage are dependent on the device width. The threshold voltages are controlled by Tr.1 and Tr.2 for 10um and 100nm width, respectively. It is also found that the program speed of 100nm width device is slower than that of 10um width device. Thus, for the programmed state with comparable threshold voltage, the trapped charge density of 100nm width device is larger than that of 10um width device, which will enhance the lateral spreading nearby the STI edge.

Based on the programmed state, 200^{0}C charge retention of 10um and 100nm width devices is simulated. Fig. 10 plots the simulated and measured threshold voltage change after different retention time at 200^{0}C. Good agreement has been achieved between the simulations and measurements. Though the programmed threshold voltage is smaller for 100nm width device, the threshold voltage reduction is larger than that of 10um width device which is similar to planar CTF. It means that the threshold voltage change caused by the charge loss of Tr.2 is large than that of Tr.1. In order to understand the charge loss of 100nm width device, we need separate the vertical loss and the lateral spreading. By turning off the tunneling through tunneling layers and blocking layers, we get the threshold voltage change caused by the lateral spreading. After subtracting it from the total threshold voltage change, we extract the threshold voltage change caused by the vertical loss. The result is plotted in the Fig. 11. Due to the existence of the internal lateral electric field by the gradient distribution of the trapped charge nearby the STI edge, the lateral spreading is dominant within all the simulated retention time. For typical two hours charge retention at 200^{0}C, the lateral spreading is about two times to the vertical loss.

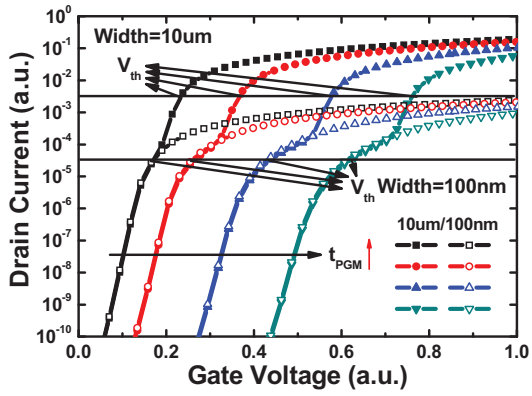

Fig. 9. Device width dependent IdVg curves after different program times. The humping effect by Tr.2 nearby the STI edge is shown for the 10um width device.

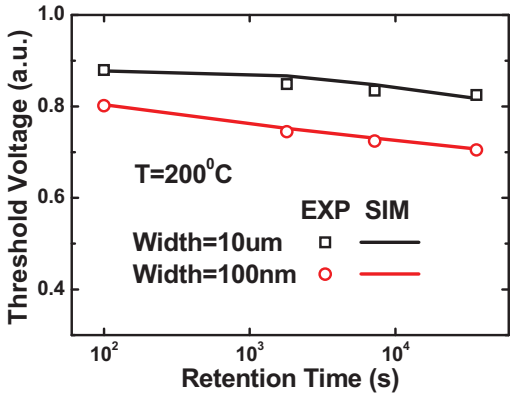

Fig. 10. Measured and simulated device width dependent threshold voltage for raised STI CTF during high temperature retention.

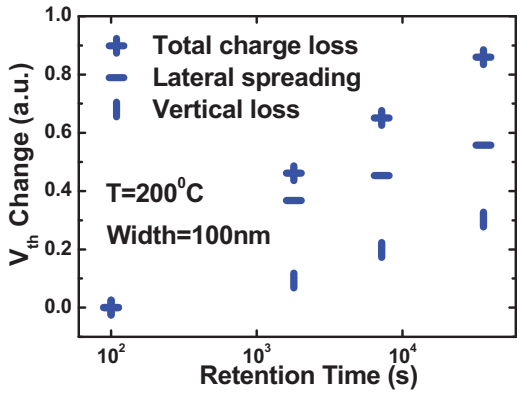

Fig. 11. Comparison between vertical loss and lateral spreading for raised STI CTF. The lateral spreading is the dominant charge loss mechanism for raised STI CTF.

IV. CONCLUSION

We have demonstrated the charge loss mechanisms in planar and raised STI NAND-type CTF memories by carefully calibrated simulations. The results show that the vertical loss through tunneling layers is dominant in planar CTF. Raised STI CTF shows an enhanced charge loss. The lateral spreading is critical in raised STI CTF with narrow width due to the internal lateral electric field by the gradient distribution of the trapped charge nearby the STI edge. Moreover, STI edge effect on threshold voltage controlling and non-uniform tunneling with local charge trapping nearby the STI edge are also responsible to the worse date retention. This work will help to understand the physical origin of CTF retention.

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