A Novel Algorithm for the Solution of Charge Transport Equations in MANOS Devices Including Charge Trapping in Alumina and Temperature Effects

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***Abstract*—We present a new algorithm for the exact solution of the system of equations describing charge trapping and transport across the dielectric stack of nitride-based charge trapping memories. The algorithm is implemented in a physical MANOS model accounting for temperature effects and charge trapping into the Al_2O_3 blocking layer. The model reproduces threshold voltage shifts measured at different temperatures on different MANOS stacks.**

I. Introduction

Nitride-based charge trapping devices like MANOS [1] are considered a promising alternative to conventional Floating Gate technology for scaled NAND Flash, since they provide a better immunity to capacitive coupling between adjacent cells and allows reducing the vertical charge loss through the tunnel oxide. The optimization of MANOS memory performance and reliability demands for a deep understanding of the physical mechanisms governing device operations. This requires accurate simulation models to interpret experimental results and to derive the trapped charge distribution, as well as to understand the effects of temperature (T) and charge trapping into the alumina. These two fundamental aspects are usually not accounted for by the physics-based MANOS models presented in the literature [2]-[5]. In addition, the existing models adopt computationally expensive iterative methods to solve the equation system describing charge trapping and transport across the MANOS stack.

In this scenario, we present a physical MANOS model accounting for temperature effects and charge trapping into Al_2O_3 blocking oxide layer. A new algorithm is developed to find the exact solution of the system of equations describing charge trapping and transport across the stack. The model is used to reproduce threshold voltage V_T shifts measured at different T on different MANOS stacks.

II. Physics-Based Model

The flow chart of the model we developed to simulate MANOS operations is shown in Fig. 1(a). The core of the model is represented by the system of differential equations in space and time given by Poisson's Equation (PE), which is solved to calculate the electric fields and the potential profile across the multilayer stack, and drift-diffusion (DD) and charge balance (CBE) equations, which are solved self consistently to derive the density of free, n_F, and trapped, n_T, electrons/holes in nitride and alumina layers. The equation system is solved self consistently by discretizing space and time into a matrix of bins (indexes i and j, respectively).

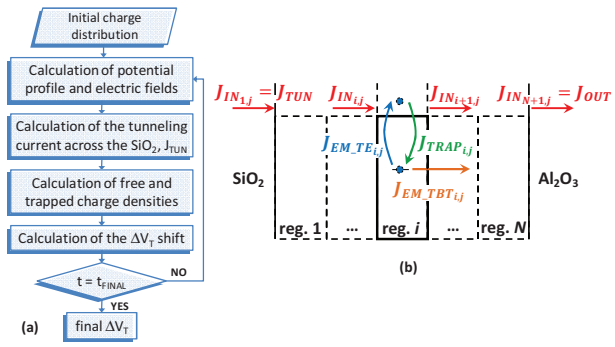

Figure 1. (a) Flow chart of the model developed to simulate TANOS operations. (b) current fluxes considered in each region.

$$J_{IN_{i,j}} = q\mu\left(n_{F_{i,j}}F_{i,j-1} + \frac{k_BT}{q}\frac{n_{F_{i,j}}-n_{F_{i+1,j}}}{L_R}\right) \quad (1)$$

$$\frac{qL_R\left(n_{F_{i,j}}-n_{F_{i,j-1}}\right)}{t_j-t_{j-1}} = J_{IN_{i,j}} - J_{IN_{i+1,j}} - J_{TRAP_{i,j}} + J_{EM_{i,j}} \quad (2)$$

$$\frac{qL_R\left(n_{T_{i,j}}-n_{T_{i,j-1}}\right)}{t_j-t_{j-1}} = J_{TRAP_{i,j}} - J_{EM_{i,j}} \quad (3)$$

$\Delta t = t_j - t_{j-1}$ is the simulation time step, q is the electron charge, μ is the constant electron mobility, $F_{i,j-1}$ is the electric field in the ith region, k_B is the Boltzmann's constant, L_R is the length of each region. $J_{IN_{i,j}}$ is the current density entering the ith region, whereas $J_{TRAP_{i,j}}$ and $J_{EM_{i,j}}$

are the current densities due to charge trapping and emission into/from the *i*th region, respectively. $J_{TRAP_{i,j}}$ is computed using Shockley-Read-Hall theory [6], whereas $J_{EM_{i,j}}$ accounts for thermal emission (TE), J_{EM_TE}, [7], and trap-to-band tunnel (TBT), J_{EM_TBT}, mechanisms [8]

$$J_{TRAP_{i,j}} = qn_{F_{i,j}} L_R R_{C_{i,j}} \tag{4}$$

$$J_{EM_{i,j}} = qL_R R_{E_{i,j}} n_{T_{i,j-1}} \tag{5}$$

$R_{C_{i,j}}$ and $R_{E_{i,j}}$ are the capture and emission rates, respectively. The *exact solution of the equation system (1)-(3), is derived using a new algorithm*, described here without lack of generality for the case of the electron (e^-) transport in nitride. Equations (1) and (2) can be rewritten to express $n_{F_{i+1,j}}$ and $J_{IN_{i+1,j}}$ as a function of $n_{F_{i,j}}$ and $J_{IN_{i,j}}$

$$n_{F_{i+1,j}} = n_{F_{i,j}} A_{i,j} - BJ_{IN_{i,j}} \tag{6}$$

$$J_{IN_{i+1,j}} = J_{IN_{i,j}} - n_{F_{i,j}} C_{i,j} + Y_{i,j} \tag{7}$$

$B = L_R/qD_N$ is a constant and $D_N = \mu k_B T/q$ is the diffusion coefficient. $A_{i,j} = \left(\mu F_{i,j-1} L_R/D_N + 1\right)$, $C_{i,j} = \left(qL_R R_{C_{i,j}} + qD_N/L_R\right)$ and $Y_{i,j} = J_{EM_{i,j}} + qL_R n_{F_{i,j-1}}/\Delta t$ are determined at the beginning of each simulation time step by calculating $F_{i,j-1}$, $R_{C_{i,j}}$ and $J_{EM_{i,j}}$, which depend only on the profile of the trapped charge calculated at the previous time t_{j-1}. Writing (6) and (7) for the *N* spatial regions leads to a system of *2N-1* equations with *2N+1* unknowns given by the currents $\left(J_{IN_{1,j}} \quad \cdots \quad J_{IN_{N+1,j}}\right)$ and by the free electron densities $\left(n_{F_{1,j}} \quad \cdots \quad n_{F_{N,j}}\right)$. The system can be solved by imposing the proper boundary conditions for the DD equation at the layer interfaces

$$J_{IN_{1,j}} = J_{TUN} \tag{8}$$

$$J_{IN_{N+1,j}} = J_{OUT} = qn_{F_{N,j}} L_R \mu F_{N,j-1} P_{OUT} \tag{9}$$

J_{TUN} and J_{OUT} are the electron current densities entering the conduction band (CB) of the first region ($i = 1$) and leaving the CB of the last region ($i = N$), see Fig. 1(b). P_{OUT}, the tunneling probability of the free electrons at the Si_3N_4/Al_2O_3 interface, and J_{TUN} are calculated using the model reported in [9], which considers a multi-phonon Trap-Assisted Tunneling (TAT) conduction mechanism, including random defect generation and charge quantization effects at the Si/SiO_2 interface. Substituting (9) in (7) written for the last region ($i = N$) allows calculating $n_{F_{N,j}}$ as a function of $J_{IN_{N,j}}$

$$n_{F_{N,j}}\left(qL_R \mu F_{N,j-1} P_{OUT} + C_{N,j}\right) = J_{IN_{N,j}} + Y_{N,j} \tag{10}$$

Equation (10) can be rewritten as

$$n_{F_{N,j}} = \frac{\beta_{N,j} J_{IN_{N,j}} + \gamma_{N,j}}{\alpha_{N,j}} \tag{11}$$

where $\alpha_{N,j} = qL_R \mu F_{N,j-1} P_{OUT} + C_{N,j}$, $\beta_{N,j} = 1$ and $\gamma_{N,j} = Y_{N,j}$. Equation (11) can be generalized by observing

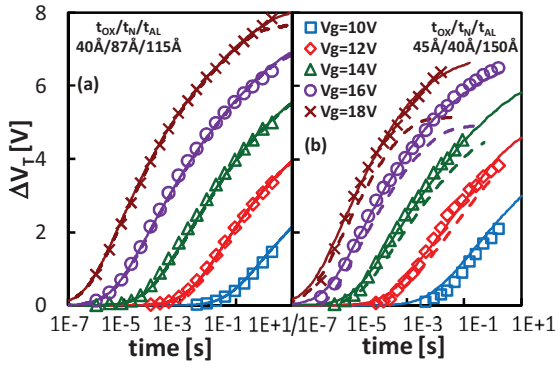

Figure 2. Program ΔV_T shifts measured (symbols) and simulated (lines) on TANOS devices with different $t_{OX}/t_N/t_{AL}$ stacks. Simulations are performed taking into account (solid lines) and neglecting (dashed lines) charge trapping into the alumina layer.

that the substitution in (10) of (6) and (7) written for the (*N-1*)th region allows calculating $n_{F_{N-1,j}}$ as a function of $J_{IN_{N-1,j}}$. Since the same procedure can be adopted for the remaining regions, we can write

$$n_{F_{i,j}} = \frac{\beta_{i,j} J_{IN_{i,j}} + \gamma_{i,j}}{\alpha_{i,j}} \tag{12}$$

where

$$\alpha_{i,j} = \begin{cases} \alpha_{i+1,j} A_{i,j} + \beta_{i+1,j} C_{i,j}, & i < N \\ qL_R \mu F_{i,j-1} P_{OUT} + C_{i,j}, & i = N \end{cases} \tag{13}$$

$$\beta_{i,j} = \begin{cases} \beta_{i+1,j} + \alpha_{i+1,j} B, & i < N \\ 1, & i = N \end{cases} \tag{14}$$

$$\gamma_{i,j} = \begin{cases} \gamma_{i+1,j} + \beta_{i+1,j} Y_{i,j} + \beta_{i+1,j} J_{TUN}, & i = 1 \\ \gamma_{i+1,j} + \beta_{i+1,j} Y_{i,j}, & 1 < i < N \\ Y_{i,j}, & i = N \end{cases} \tag{15}$$

The coefficients $\alpha_{i,j}$, $\beta_{i,j}$ and $\gamma_{i,j}$ are calculated at the beginning of the simulation time step, since they depend on quantities that depend only on the profile of the trapped charge calculated at the previous time t_{j-1}.

Once $\alpha_{i,j}$, $\beta_{i,j}$ and $\gamma_{i,j}$ have been calculated for every region, equations (12) and (7) can be used to derive the profile of the free electron density n_F, starting from the first region where $J_{IN_{1,j}} = J_{TUN}$ (J_{TUN} is calculated). The n_T profile is finally determined from the n_F profile by using (4). The same procedure is adopted to derive n_F and n_T profiles in the alumina layer, provided that the correct boundary conditions are used for the DD equation.

Equations (6), (7), (12)-(15) represent a fast alternative method (compared to the iterative methods proposed and adopted in the literature [5], [10]) to achieve a closed-form accurate solution of the equation system (1)-(3). Note that the minimum time step adopted in simulations should not exceed ~10ms in order to guarantee a high accuracy and the self-consistency of the derived solution.

III. Model Results

Model simulations allow reproducing threshold voltage shifts measured during P/E operations and retention in TANOS devices manufactured by different technologies

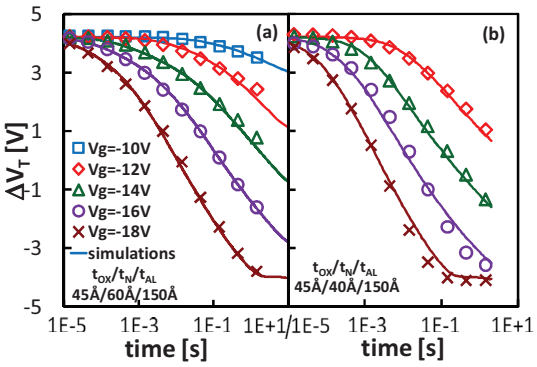

Figure 3. Erase ΔV_T shifts measured (symbols) and simulated (lines) on TANOS devices with different stacks.

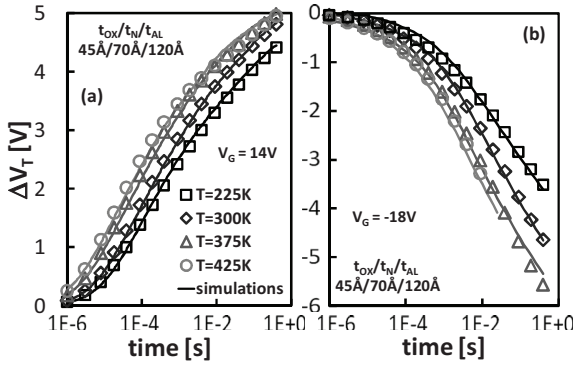

Figure 4. (a) program and (b) erase ΔV_T shifts measured (symbols) and simulated (lines) at different T.

[6], [8], [11]. In this paper we will focus on simulation results reproducing the effects of charge trapping in alumina and temperature on TANOS devices operation and reliability. Devices considered in this work are MANOS capacitors with different $SiO_2/Si_3N_4/Al_2O_3$ layer thicknesses. The SiO_2 tunnel oxide was thermally grown on the (100) Si substrate, followed by the silicon nitride layer deposition. Al_2O_3 blocking layer was grown using the atomic layer deposition technique. A post-deposition annealing at 1100°C is used to obtain the Al_2O_3 γ crystalline phase. PVD TaN was then deposited to complete the gate stack.

The model described in the previous section allows both reproducing V_T shifts and estimating the contribution of alumina trapping to the total P/E V_T shift and its dependence on stack composition (i.e. on the ratio between nitride and alumina thicknesses, t_N/t_{AL}). Fig. 2 shows the programming transients measured on samples having (a) high and (b) low t_N/t_{AL} ratio. Simulations reproduce very well the experimental data in the whole voltage and time range using a single set of electron trap parameters for nitride (N_T=4.5·10^{19} cm^{-3}; σ_T=8.5·10^{-15} cm^2; E_T=1.6÷2.6 ± 0.2eV below CB) and alumina (N_T=2·10^{19} cm^{-3}; σ_T=8·10^{-15} cm^2; E_T=1.9÷2.7 ± 0.2eV below CB). In devices having a high t_N/t_{AL} ratio, the charge trapping into the Al_2O_3 layer is negligible, as confirmed by simulations performed considering and neglecting the alumina contribution, which are superimposed, see Fig. 2(a). In fact, most of the electron charge injected through the SiO_2 layer during program is trapped in the thick nitride layer. As a consequence, only a limited fraction of electrons can reach the alumina CB and, therefore, is available for trapping in the alumina defects.

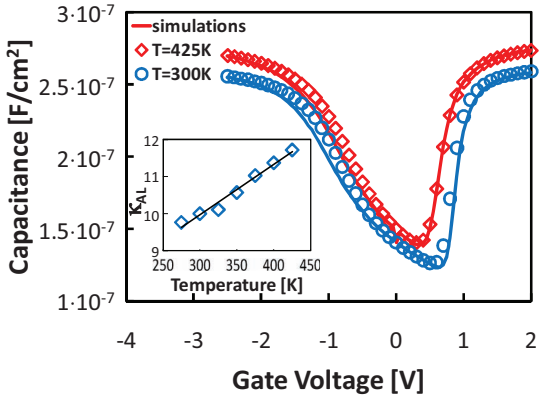

Figure 5. C-V characteristics measured (symbols) and simulated (lines) on a TANOS capacitor at different temperatures. The inset shows the extracted variation of the alumina dielectric constant (κ_{AL}) with temperature.

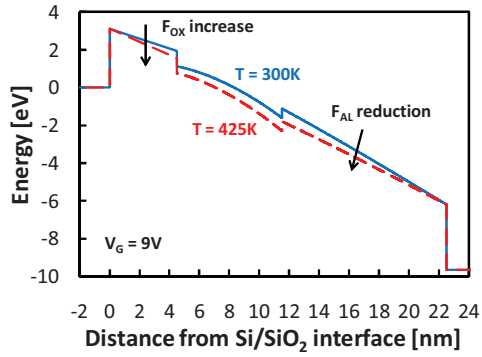

Figure 6. Schematic representation of the band diagram of a TANOS device under program at different temperatures.

Conversely, data measured on the stack with a low t_N/t_{AL} ratio cannot be reproduced if electron trapping into Al_2O_3 defects is neglected, and corresponding simulations exhibit an early saturation, see dashed lines in Fig. 2(b). The contribution of electrons trapped into alumina to the total V_T shift ranges from 15% to 25%, depending on the program voltage and on the nitride/alumina thickness ratio.

Threshold voltage shift measured during erase in TANOS devices are shown in Fig. 3 for two different stack compositions. Again, the experimental data are accurately reproduced by simulations performed considering the simulated electron distribution after program and a single set of hole (h^+) trap parameters for nitride (N_T=6·10^{19} cm^{-3}; σ_T=2·10^{-14} cm^2; E_T=1.9÷2.7 ±0.2eV below the valence band, VB) and alumina (N_T=2·10^{19} cm^{-3}; σ_T=1·10^{-14} cm^2; E_T=1.6÷2.4 ± 0.3eV below VB). Interestingly, simulations show that hole trapping in alumina is negligible regardless of both the erase V_G and the t_N/t_{AL} ratio. This because the high offset between nitride and alumina valence bands (~3eV) prevents h^+ from reaching the Al_2O_3 layer.

The proposed model takes into account also the strong T dependence observed in P and E operations, see Fig. 4. As can be seen, threshold voltage curves observed during P/E transients increase with the temperature [8]. This effect is due to a linear increase of the Al_2O_3 dielectric constant κ_{AL} with temperature [8], [12] that we estimated in 20%-25% over 125K by reproducing the CV curves measured on TANOS capacitors, see Fig. 5. A similar variation of κ_{AL} has been measured on nMOS capacitors with a 150Å thick

alumina layer as gate dielectric [8], proving that the effect is related only to the alumina. By including the linear variation shown in Fig. 5 in the MANOS model, simulations reproduce very accurately the experimental V_T shifts in the whole T range considered, see Fig. 4. In fact, an increase of κ_{AL} leads to a reduction of the electric field and thus of the voltage drop across the Al_2O_3 layer that, in turn, results in higher voltage drops across SiO_2 and Si_3N_4 (since the voltage applied to the stack is constant), as schematically depicted in Fig. 6. The final effect is an increase of the SiO_2 electric field, which raises the electron current injected into nitride CB leading to higher P/E speed, as described by the model in Fig. 4.

IV. Conclusions

We presented here a novel algorithm for the fast solution of the equation system describing charge trapping and transport in MANOS memory devices. The model is shown to reproduce accurately the effects of both temperature and charge trapping into alumina on MANOS P/E operations and reliability.

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