Variability in Nano-scale Intrinsic Silicon-on-Thin-Box MOSFETs (SOTB MOSFETs)

Yunxiang Yang, Gang Du, Ruqi Han, Xiaoyan Liu*
Institute of Microelectronics, Peking University, Beijing, China
* xyliu@ime.pku.edu.cn

Abstract- **Lightly doped or even intrinsic channel can be used in SOTB MOSFETs and therefore very Low RDF (random dopant flunctuation) can be expected in such devices. In this work, we systematically investigated the influences of the intrinsic parameter fluctuations, including LER (line-edge-roughness), STV (silicon thickness variation) and WFV (metal-gate work-function variation), on 20nm-gate intrinsic SOTB MOSFETs with GP (ground plane). Conditions of SOTB without GP and with PGP (partial ground plane) are also simulated for comparison. Our results show that LER dominates fluctuations in n-SOTB while LER and WFV dominate that in p-SOTB. Introduction of GP can effectively reduce LER- and STV-induced variations of V_{tsat}, DIBL and I_{on} with a slightly sacrifice of σLog(I_{off}) while it has little effect on WFV-induced variations. A detailed design of PGP is desired from the perspective of variability-aware optimization.**

Keywords- Intrinsic channel, SOTB, variability, intrinsic parameter fluctuations, ground plane, variability aware design, TCAD

I. INTRODUCTION

Variability is one of the most important considerations as the critical dimension (CD) stepped into nano-scale region. Conventional bulk MOSFETs have been dramatically challenged by the intrinsic parameter fluctuations, especially random dopant fluctuation (RDF) since highly doped channel has to be used in such devices to adjust the threshold voltage (V_{th}) as well as suppress the short channel effects (SCEs). Silicon-on-thin-box (SOTB) MOSFET is an attractive device because of its excellent immunity to SCEs as well as its good controllability of threshold voltage and power consumption [1]. Since lightly doped or even intrinsic channel can be used in SOTB MOSFETs, very small RDF can be obtained. In fact, it is reported [2] that SOTB MOSFETs have the smallest V_{th} variability due to its suppressed RDF.

However, in nano-scale technology, the correlation length of line-edge-roughness (LER) [3] is comparable to the transistor dimension and the grain size of metal gate is comparable to the total gate area [4], both of which will cause a strong variability. Therefore, it is imperative to study the variability performance of SOTB MOSFETs. Beyond LER and WFV (Work-Function Variation due to various grain orientations), silicon film thickness variation (STV) is another important variability source for SOTB because ultra-thin silicon body has to be used in SOTB to gain immunity to SCEs [5]. In this study, we systematically investigated the influences of LER, WFV and STV on 20-nm-gate SOTB MOSFETs. Different SOTB MOSFETs that with and without ground plane (GP) and with partial ground plane (PGP) were compared. Results are important on optimizing the performance of SOTB MOSFETs.

II. SIMULATION METHOD

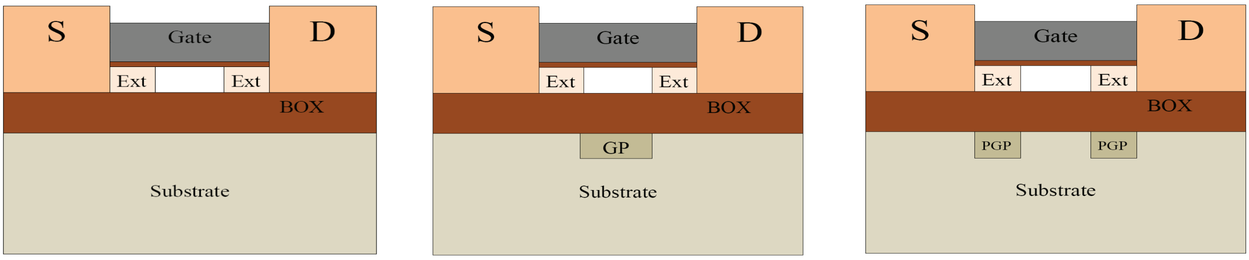
Fig.1 (a)-(c) shows the simulated SOTB without GP, with GP and with PGP, respectively. Geometrical, doping and electrical parameters are listed in Table I. Fig.1 (d) illustrates the influence of LER on device's channel length and extension doping profile. Fig.1 (e) sketches a square part of the metal-gate consisting of several grains. A Fourier analysis of the power spectrum of Gaussian autocorrelation function is employed to simulate LER. Typical value of LER parameters (Δ=1.5nm and Λ=20nm) are used according to [6, 7]. The silicon layer thickness tolerance is taken as 10% [7]. The effective gate work-function is modeled as a probabilistic distribution [8, 9], as illustrated in Fig.1 (f), considering that the gate of a nano-scale device is composed of a small number of the grains which may have different orientations and thus various work-functions. The ISE TCAD tools [10] have been used to carry out our simulations. In order to achieve a good stability of the statistics, all the simulations have a sample size of 100. Quantum effect is taken into account by the density-gradient approximation.

TABLE I
PARAMETERS USED IN SIMULATION.

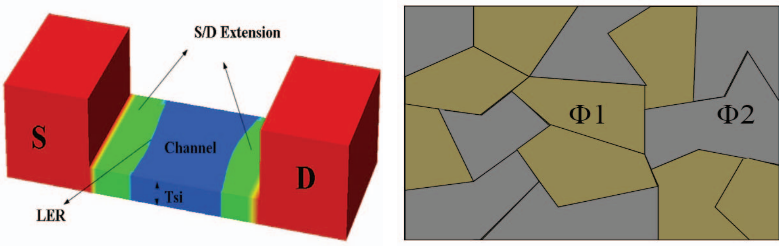
PARAMETERS	VALUES
Gate Length (Lg)	20 nm
Channel Width (W)	30nm
Silicon Body Thickness (T_{si})	5.5nm
Box Thickness (T_{Box})	10nm
EOT	1.0 nm
S/D Doping Conc.	10^{20} cm^{-3}
Extension Doping Conc.	$5x10^{19}$ cm^{-3}
GP/PGP Doping Conc.	$1x10^{19}cm^{-3}$
Channel Doping	Intrinsic
Supply Voltage	+/- 0.9V
Back Gate Bias ($V_{back-gate}$)	-0.9, 0,0.9 V
Work-function (WF)	4.60eV

III. RESULTS

The threshold voltage (V_{th}) is extracted by the constant current ($1.5x10^7$ A for n-SOTB and $0.5x10^{-7}$A for p-SOTB) method. We define V_{tlin} as V_{th} at drain bias of



(a) (b) (c)



(d) (e)

Material	Orientation.	Probability	WF	Grain Size
TiN n-SOTB	<200>	60%	4.6 eV	Process depended. Here we assume 4nm both for TiN and MoN. [4]
	<111>	40%	4.4 eV	
MoN p-SOTB	<110>	60%	5.0 eV	
	<112>	40%	4.4 eV	

(f)

Fig.1 Simulated structures: (a) without GP; (b) with GP; (c) with PGP. (d): LER causes a variation of the effective channel length and influences the extension doping profile. (e): Different orientations have different WFs, and the effective WF is calculated as : $\Phi_{eff}=\Sigma\Phi_iP_i$. Φ_i donates the WF, and P_i is the probability corresponding to Φ_i, as shown in (f).

+/-0.05V, and V_{tsat} as V_{th} at drain bias of +/-0.9V. The drain induced barrier lowering (DIBL) effect is evaluated by $|V_{tlin}-V_{tsat}|/0.85$. The body factor (γ) is simply defined as $|\Delta V_{tsat}/\Delta V_{back\text{-}gate}|$ or C_{BS}/C_{gate}, where C_{BS} stands for body/substrate coupling capacitance and C_{gate} donates gate capacitance [11]. Then we focus on their fluctuations under different back gate biases (see TABLE I). Results are shown in Fig.2-7.

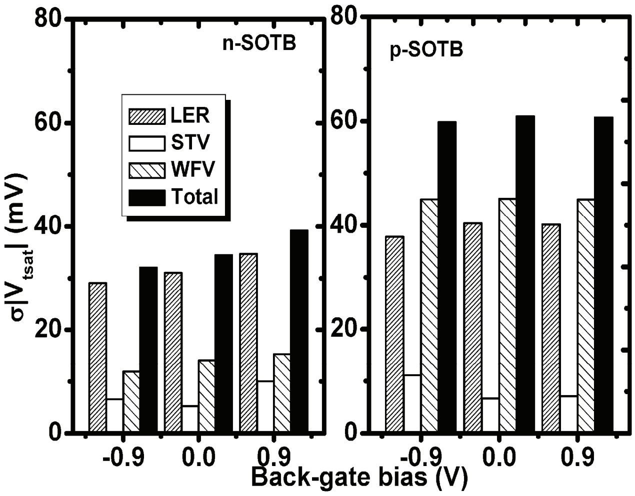


Fig.2 $|V_{tsat}|$ fluctuation for n- and p-SOTB with GP under different back-gate biases.

Fig.2 shows the V_{tsat} fluctuations of n- and p-SOTB with GP. It can be seen that for n-SOTB LER dominates σV_{tsat}, followed by WFV and STV; however, for p-SOTB WFV and LER together dominate σV_{tsat}, and STV causes the smallest σV_{tsat}. Considering that WFV is process sensitive and that the grain size of 4nm we have used in the WFV modeling is of the state-of-art, the actual WFV-induced V_{th} fluctuation might be even larger than what we have predicted in Fig.2. Fig.3 plots the DIBL variation of n- and p-SOTB with GP. Different from the result of σV_{tsat}, WFV has little effect on σDIBL. Moreover, LER causes a large variation of DIBL, and this is one important reason for the large LER-induced fluctuation of V_{tsat} as shown in Fig.2. STV brings about a fluctuation of DIBL around the scale of 5mV/V. Variation of SS (subthreshold slope) , as shown in Fig.4, presents similar trend as that of DIBL because both of them have a strong correlation with the body/substrate coupling capacitance [12]. Variation of body factor is dominated by STV and is strong influenced by the back gate bias as shown in Fig.5. This is easy to understand since both STV and back gate bias directly modulate the magnitude of C_{BS}. Fig.6 plots fluctuations of drive current (I_{on}) and Fig.7 show that of leakage current (I_{off}) in the log-scale. LER causes the largest fluctuations of I_{on} and I_{off} both for n- and p-SOTB, which is different from the intuitional prediction based on the result of σV_{tsat}. In fact, the aforementioned LER-induced large fluctuation of SS will also bring about a large spread of I_{on} and I_{off}. Therefore, LER becomes the dominating factor of σI_{on} and $\sigma Log(I_{off})$. However, WFV still challenges p-SOTB in terms of σI_{on} and $\sigma Log(I_{off})$, especially considering that WFV is process sensitive.

Considering that the introduction of GP may bring large parasitic capacitance and thus increases the circuit delay, the condition of SOTB without GP and that of with PGP are simulated here as well. Results are listed in Table II, showing that, compared with the case of without GP and that of with PGP, GP effectively reduces LER- and STV-induced variations of V_{tsat}, DIBL and I_{on}, slightly increases LER-induced $\sigma Log(I_{off})$, and has little effect on other parameters. Under different back-gate biases, PGP presents a complicated influence (compared to case of without GP) on LER- and STV-induced variability, which may indicate that in the case of with PGP parameter fluctuations are very sensitive to details of PGP structure (e.g., doping concentration, dimension, position [13]) in the scale of around 20nm. Both of GP and PGP have little effect on WFV-induced variations.

		n-SOTB/|p-SOTB| w/o GP						n-SOTB/|p-SOTB| w/ PGP					
		σV_{tsat}	σ_{DIBL}	$\sigma\gamma$	σSS	σI_{on}	$\sigma log I_{off}$	σV_{tsat}	σ_{DIBL}	$\sigma\gamma$	σSS	σI_{on}	$\sigma log I_{off}$
-0.9	LER	31/41	16/25	5/4	3.7/5.6	48/40	1.15/1.13	31/37	16/22	1/4	3.4/5.5	45/36	1.22/1.08
	STV	8/14	4/9	5/2	1.0/2.0	15/7	0.39/0.47	6/12	4/7	3/7	*/2.0	11/6	0.25/0.44
	WFV	14/44	*/*	2/3	*/*	11/28	0.38/0.99	13/45	*/*	2/*	*/*	10/27	0.39/1.02
0	LER	35/38	22/20	--	5.2/4.7	56/37	1.08/1.18	31/39	16/16	--	3.4/3.9	49/28	1.14/1.23
	STV	11/12	8/8	--	1.8/1.8	15/8	0.42/0.47	6/7	3/4	--	*/1.5	12/5	0.31/0.36
	WFV	15/45	*/*	--	*/*	12/27	0.36/1.05	15/45	*/*	--	*/*	11/26	0.38/1.11
0.9	LER	38/41	25/18	4/5	5.8/5.0	59/26	1.02/1.27	34/43	22/20	4/6	5.5/5.2	54/23	0.99/1.31
	STV	14/11	9/6	2/2	2.1/1.7	14/7	0.43/0.44	11/8	7/7	8/4	2.0/0.9	13/4	0.39/0.29
	WFV	15/45	*/*	*/*	*/*	12/25	0.34/1.11	15/45	*/*	*/*	*/*	12/25	0.35/1.15
Unit		mV	mV	mV/V	mV/dec	μA/um	Log(A/μm)	mV	mV	mV/V	mV/dec	μA/um	Log(A/μm)

TABLE II: Intrinsic parameter fluctuations of n- and p-SOTB w/o GP and w/ PGP. (*: Variations that below 1% (σ/μ), and thus ignored.)

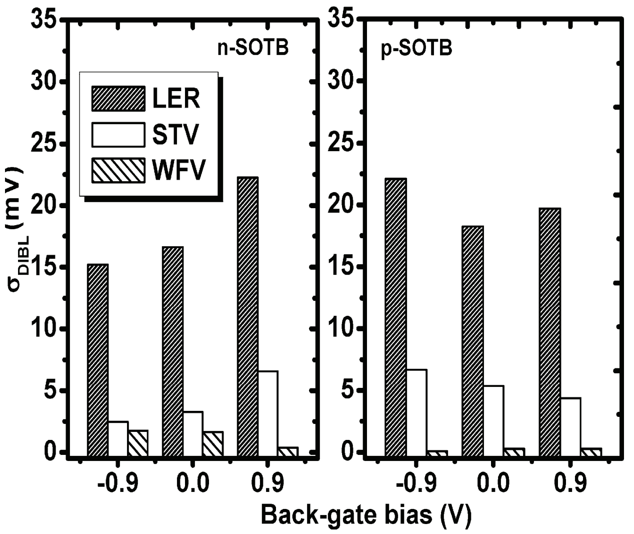


Fig.3 DIBL fluctuation for n- and p-SOTB with GP under different back-gate biases.

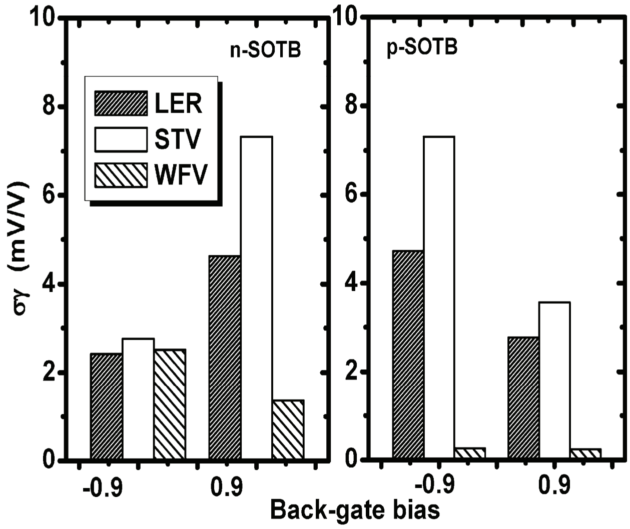


Fig.5 γ (body factor, defined as $|\Delta V_{tsat}/ \Delta V_{back\text{-}gate}|$) fluctuation for n- and p-SOTB with GP under different back-gate biases.

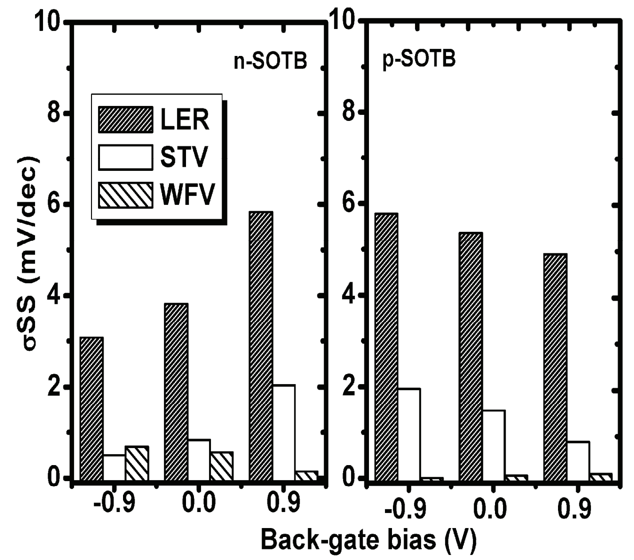


Fig.4 SS (sub-threshold slope) fluctuation for n- and p-SOTB with GP under different back-gate biases.

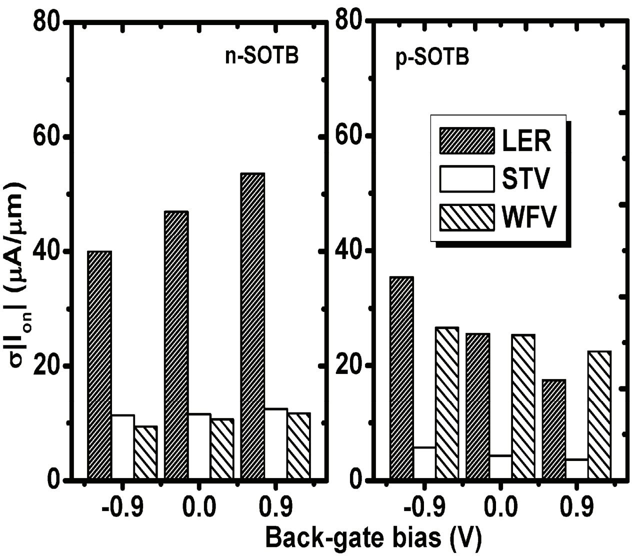


Fig.6 $|I_{on}|$ fluctuation for n- and p-SOTB with GP under different back-gate biases.

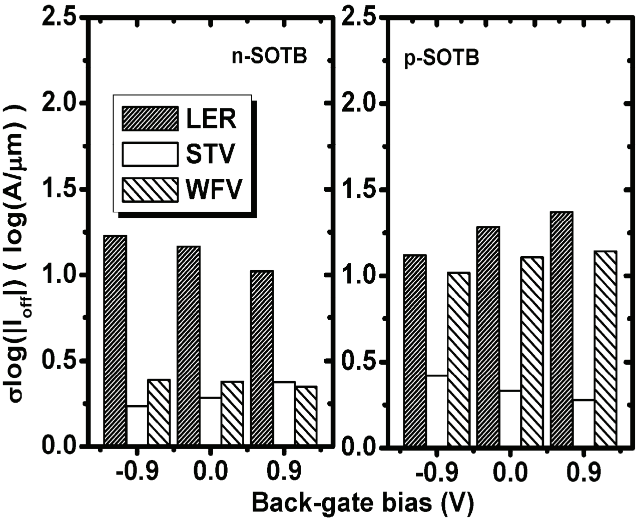


Fig.7 $|I_{off}|$ fluctuation for n- and p-SOTB with GP under different back-gate biases.

IV. CONCLUSION

In this study, we have investigated the influences of intrinsic parameter fluctuations in 20-nm-gate SOTB MOSFETS. Our results show that LER dominates fluctuations in n-SOTB, and LER and WFV dominate that in p-SOTB. Introduction of GP can effectively reduce LER- and STV-caused variations of V_{tsat}, DIBL and I_{on} with a slightly sacrifice of $\sigma Log(I_{off})$ while has little effect on WFV-caused variations. A detailed design of PGP is desired from the perspective of variability-aware optimization.

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