Statistical Simulation of Metal-Gate Work-function Fluctuation in High-κ/Metal-Gate Devices

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Abstract—**In this work, we statistically examine the emerging high-κ / metal gate work-function fluctuation (WKF) induced threshold voltage (V_{th}) fluctuations in 16-nm-gate MOSFET devices. Our Monte-Carlo model extensively evaluates the impact of WKF for different technology node, metal grain size, and gate material. This model provides us to identify suitable materials and fabrication processes that can significantly reduce the impact of V_{th} fluctuation owing to WKF. First, four kinds of gate material are examined and TiN possesses the smallest V_{th} fluctuation. For fabrication process, a fast deposition of metal at lower temperature prevents the metal grain not to grow to large size result in a smaller variation. In addition, an idea of modeling multilayer metal gate WKF is also presented and discussed, in which the first layer plays the most important role, compared with other layers, for the fluctuation suppression.**

Keywords - Work-function fluctuation, emerging device, 16-nm-gate MOSFET, high-κ/metal gate, modeling and simulation, Monte Carlo

I. INTRODUCTION

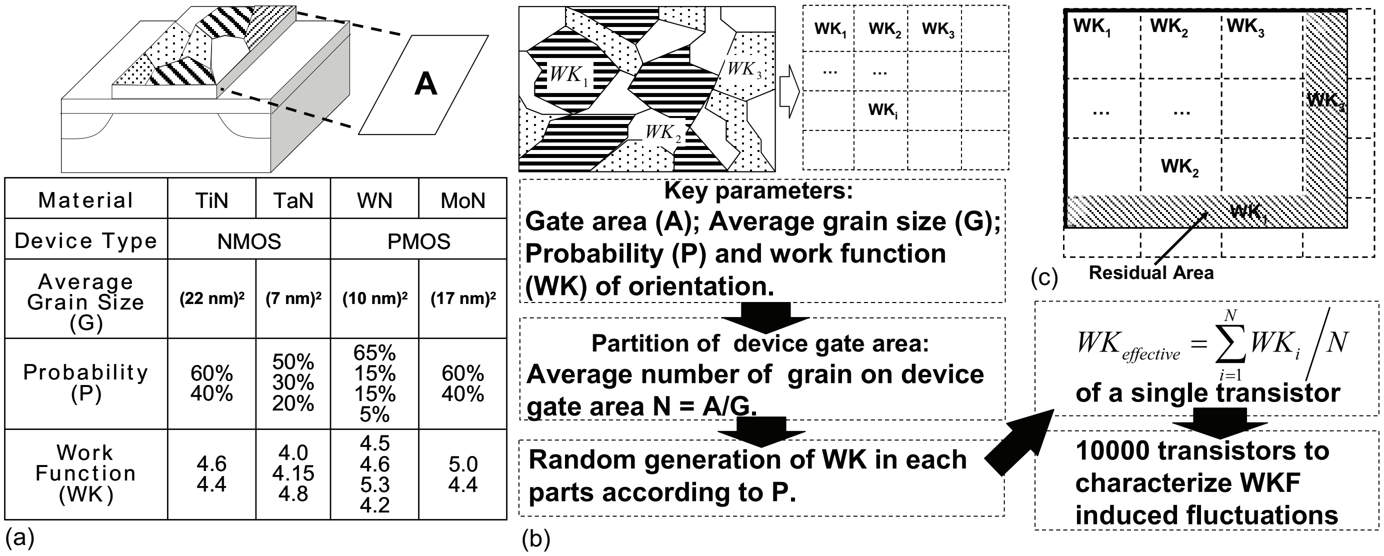
The size of complementary metal-oxide-semiconductor (CMOS) field effect transistors (FETs) have been rapidly scaled down and the variability are great of interest and become a major challenge to device technologies. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, fluctuations in process parameters, and other factors, are known as indispensable components of the robust circuit design procedure. For state-of-art nanoscale CMOS circuits and systems, the intrinsic device parameter fluctuations that result from line edge roughness [1], the granularity of the polysilicon gate [2,3], random discrete dopants [4-11] and other causes, have substantially affected signal system timing in digital circuit [10], high frequency characteristics in analog circuit [9], and operating failure in memory circuits. Diverse simulation and suppression approaches have recently been presented to investigate intrinsic parameter fluctuations in semiconductor devices [1-8] and circuits [9-10]. Among these approaches, the metal-gate and high-κ dielectrics are key technologies for the reduction of intrinsic parameter fluctuations.

High-κ/metal-gate technology has been recognized as the key to sub-45-nm transistor fabrication due to the small gate leakage current with an increased gate capacitance. The sheet resistance is also reduced with the use of metal as gate material. Comparing to the poly-gate technology, the metal-gate material will not react with high-κ material; and therefore there existing less threshold voltage (V_{th}) pinning effect. The gate depletion in poly-gate material is no longer existed. Moreover, the phonon scattering effect is significantly reduced due to the less quantum resonance effect. However, the grain orientation of metal is uncontrollable during growth period [12,13]. It is known that metal grains usually grow up to few nanometers in size under temperatures normally used in integral circuit fabrication. Since gate dimensions are in the range of few tens of nanometers, it is expected that the gate area will contain only a small number of grains. Therefore, the use of metal as gate material introduces a new source of random variation, work-function fluctuation (WKF) due to the dependency of work-function on metal grain orientations [14,15]. It is essential to find a way which can effectively investigate the impacts of the WKF on CMOS device and circuit characteristic fluctuations.

In this work, the work-function fluctuation issue has been highlighted and a statistical model is presented, which can be used in evaluating the impact of WKF on emerging high-κ/metal gate CMOS devices. In addition, the proposed model can be employed to identify appropriate materials and process conditions that can reduce the impact of random grain orientations and to analyze the impact of such variations on the device characteristic fluctuations and circuit-level performance and reliability. Moreover, multilayer metal material is a novel technique to achieve a desired work-function of device to further reduce the V_{th} fluctuation, where the fluctuation of such technique is also predicted and discussed with our model.

This paper is organized as follows. Section II introduces the modeling technique for studying the effect of work-function fluctuation on device's characteristics. Section III studies the WKF- induced device characteristic fluctuations with different technology node, metal grain size, and gate material. Section IV presents the idea of multilayer metal-gate WKF-induced V_{th} fluctuation. Finally, conclusions are drawn and the future work is suggested.

978-1-4244-7700-5/10/$26.00



Material	TiN	TaN	WN	MoN
Device Type	NMOS		PMOS	
Average Grain Size (G)	(22 nm)^2	(7 nm)^2	(10 nm)^2	(17 nm)^2
Probability (P)	60% 40%	50% 30% 20%	65% 15% 15% 5%	60% 40%
Work Function (WK)	4.6 4.4	4.0 4.15 4.8	4.5 4.6 5.3 4.2	5.0 4.4

Figure 1. (a) The device gate area is A which composes many metal grains, and the average grain size (G), probability (P) and workfunction (WK) of grain orientation for different metal materials used in this work are listed. (b) Simulation flow chart to study the work-function-induced characteristic fluctuations, the grain shape is assumed to be square for simplication. (c) In our model, we consider the effect of residual area to provide the best accuracy.

II. MODEL OF METAL WORK FUNCTION FLUCTUATION

The devices we explored are the planar bulk metal oxide semiconductor field effect transistors (MOSFETs) with amorphous-based HfSiON gate stacks and different metal materials, TiN and TaN are used for n-type MOSFET (NMOS) and WN and MoN for p-type MOSFET (PMOS) [10,13]. The device performances are according to ITRS roadmap for low operating power application and calibrated to the experimentally measured data to ensure the best accuracy [11]. Figure 1(a) illustrates the work function fluctuation on metal-gate devices, the gate area is A and contains many metal grains for a given material, and the average grain size (G), probability (P) and work-function (WK) of grain orientation for different metal materials used in our simulation are also defined [13]. Since each grain orientation has different work-function, the gate work-function should be modeled as a probabilistic distribution rather than a deterministic value. Therefore, a statistically-sound Monte-Carlo approach is advanced here for modeling such a probabilistic distribution. Figure 1(b) shows the statistical simulation flow chart of our model. To effectively characterize the work-function fluctuation, we assume the metal grain is square. Then the gate area of 16-nm-gate transistor is partitioned into several parts according to the average grain size and the number of grain is device area over grain size. The work-function of each grain is generated according to it probability, and the effective work-function of a single transistor is equal to an average of all grains. We randomly simulated 10^4 transistors to estimate the WKF-induced V_{th} fluctuation (σV_{th}). Moreover, it is also important to consider residual areas due to the gate will not always fortuitously include the integer value of grains, as shown in Fig. 1(c). In our simulation approach, we also randomly generate the work-function for each residual grain, and consider their weight related to their area when calculating effective work-function.

III. RESULTS AND DISCUSSION

Figure 2 shows WKF-induced σV_{th} for the properties of metal according to Fig. 1(a), in which the TiN gate material exhibits the smallest σV_{th} and MoN gate material shows the largest. To find the key parameter of work-function fluctuation, we further compare the σV_{th} for the differential metal material in different gate area with the same grain size (4 nm)^2, as shown in Fig. 3. The TiN induces the smallest σV_{th} due to fewer kinds of grain orientations and smaller work-function deviation of each orientation. Figure 4 compares the WKF-induced σV_{th} as the function of grain size but fixed gate area (16 nm)^2 with TiN, TaN, WN, and MoN gate material, the results indicate that σV_{th} increases as the grain size increases.

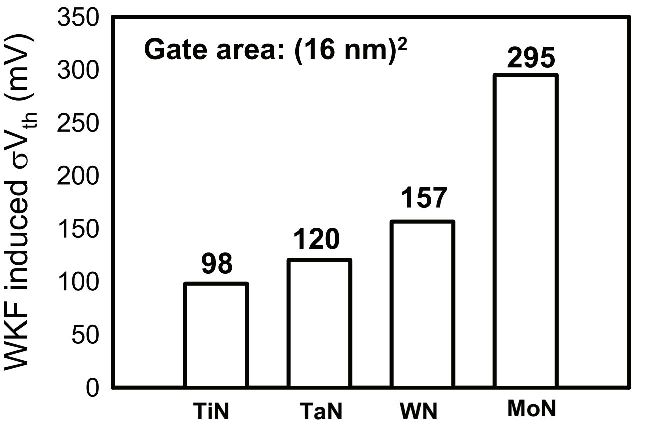


Figure 2. The work-function-induced threshold voltage fluctuation (σV_{th}) of different material, whose properties are shown in Fig. 1(a).

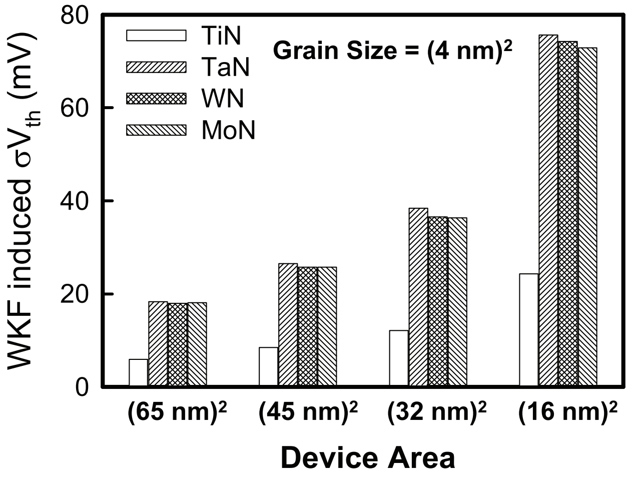


Figure 3. Comparison of the σV_{th} among various metal materials with respect to different technology node for a $(4\ \text{nm})^2$ grain size.

The reason of this result is because when the grain size is large, the gate area may contains only one grain, the effective work-functions of single transistor are 4.4 eV or 4.6 eV, and induce two different V_{th} values as shown in Fig. 5(a); consequently, it results in a large standard deviation of the threshold voltage in the simulated 10^4 devices. On the other hand, when the grain size is small, the gate area contains many metal grains and the effective work-functions among all devices become a Gaussian distribution, as shown in Fig. 5(b). Therefore, a fast deposition of metal at lower temperature prevents the metal grain not to grow to large size should be used in fabrication process when we consider WKF induced σV_{th}. Additionally, when the metal grain size is larger than device's gate area, the σV_{th} saturated due to the number of grain in a device gate area unchanged (contain only one grain).

We could conclude that the WKF-induced threshold voltage fluctuation is affected by the gate area, the grain size, and the gate material, according to the aforementioned results. Therefore, to evaluate the impact of work-function fluctuation in threshold voltage fluctuation more effectively, we herein consider an analytic formula to describe them:

$$\sigma V_{th} = A_{VT}\sqrt{\frac{G}{A}}, \tag{1}$$

where G and A are the grain size and the device gate area , and A_{VT} is a fitting coefficient depending upon the metal materials, the unit of A_{VT} is (mV). The $A_{VT,TiN}$, $A_{VT,TaN}$, $A_{VT,WN}$, $A_{VT,MoN}$, which represent the fitting coefficient of TiN, TaN, WN, and MoN are 90, 283, 272, 271, respectively. Note that the equation (1) is validated for the grain size smaller than the gate area; for the grain size larger than the gate area, the WKF-induced σV_{th} will be saturated, as mentioned in the last paragraph.

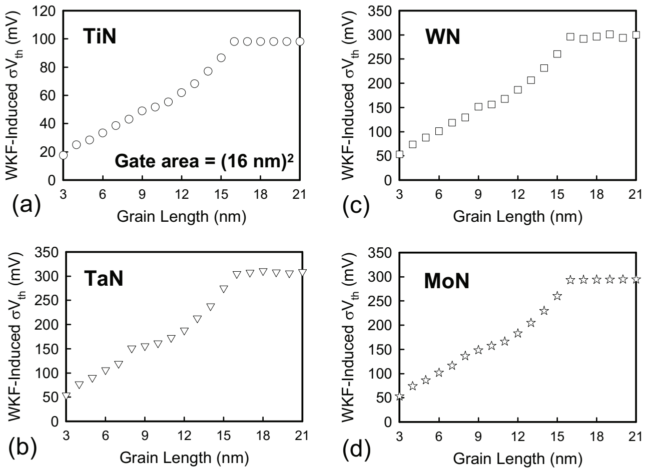


Figure 4. WKF-induced σV_{th} as a function of grain size for (a) TiN, (b) TaN, (c) WN, and (d) MoN, where the grain length is square root of grain size.

IV. MODEL OF MULTILAYER METAL GATE STRUCTURE

Multilayer structure is a technique in order to further reduce σV_{th} for enhancement of current drivability and low operating power applications at a reduced supply voltage, or to realize multiple V_{th}'s for design flexibility of CMOS circuits [15,16]. Our model can also predict the σV_{th} of this fabrication technique. Figures 6(a) and 6(b) show the illustration of multilayer structure and its band diagram, and Fig. 6(c) introduces a way to characterize the multilayer metal gate induced-WKF. We first independently generate the work-function of each grain in each layer, the details of the flow follows Fig. 1(b), in which each layer has its own work-function distribution. To calculate the effective work-function of multilayer gate device, we find the highest common factor (H.C.F.) of grain sizes among these layers, and the work-function at each point in the gate area is their combination with a given weight, as shown in Fig. 6(c). The weight of each layer is estimated by the device simulation. Table I shows the comparison of the computed σV_{th} for different material as the first layer at the given material TiN and MoN with grain size $(22\ \text{nm})^2$ and $(17\ \text{nm})^2$, respectively. The device area is set to $(90\ \text{nm})^2$. The results show that first layer is the most important for device design if we consider WKF-induced device characteristic fluctuations because the first layer causes large and direct controllability to the device channel region.

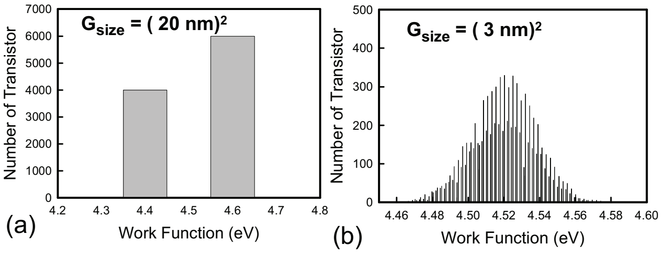


Figure 5. The work function distributions for the gate size of (a) 21 nm x 21 nm and (b) 3 nm x 3 nm.

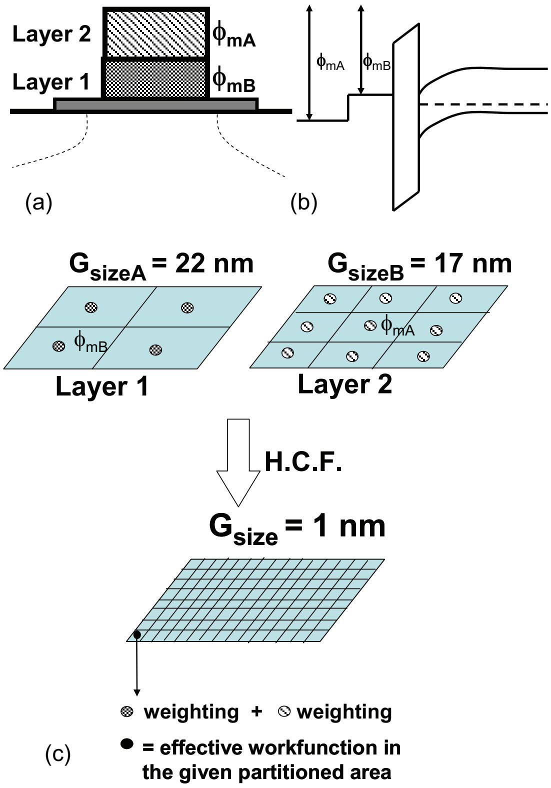


Figure 6. Illustrations of the novel multilayer (a) structure and (b) band diagram. (c) The idea for calculating the multilayer metal gate WKF-induced characteristic fluctuation.

V. CONCLUSIONS

In this study, a new source of random variation caused by the dependency of metal work-function on grain orientation has been modeled. We have presented a statistical Monte Carlo simulation approach to estimating the effect of WKF on device's characteristics. Our results show that the large metal grain size and small device area will induce large V_{th} fluctuation. However, the fluctuation could be saturated if the grain size is larger than the device area. For this reason, a fast deposition of metal at lower temperature preventing the metal grain not to grow to large size should be used in fabrication process. Additionally, TiN material shows the robustness to against WKF due to fewer kinds of grain orientations and smaller work-function deviation of each orientation. Moreover, the method of multilayer metal gate work function fluctuation has also presented; the first layer plays the most important role if considering work-function fluctuation.

TABLE I. THE VTH FLUCTUATION COMPARISON FOR DIFFERENT MATERIAL AS THE FIRST LAYER

Material	Grain Size	Device Area	σV_{th} (mV)
TiN (layer1) MoN (layer2)	$(22\ \text{nm})^2$ $(17\ \text{nm})^2$	$(90\ \text{nm})^2$	17.7
MoN (layer1) TiN (layer2)	$(17\ \text{nm})^2$ $(22\ \text{nm})^2$	$(90\ \text{nm})^2$	63

ACKNOWLEDGMENT

This work was supported in part by Taiwan National Science Council under Contact NSC-97-2221-E-009-154-MY2 and by TSMC, Taiwan, under a 2009-2010 grant.

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