Lithography Induced Layout Variations in 6-T SRAM Cells

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Abstract— **A simulation study of lithography induced layout variations in 6-T SRAM cells is presented. Lithography simulations of a complete 6-T SRAM cell layout, including active n+/p+ regions layer and poly-gate layer were performed. The smallest feature size was assumed to be 45 nm. 76 positions of the projector focus were simulated for each layer in total. TCAD simulations of 32 nm single gate FD SOI MOSFETs were performed to calculate the electrical behavior. SPICE parameters were extracted from reference results obtained by TCAD simulations. More than 5000 variations of the the static and dynamic SRAM cell performance in dependence on lithography induced variations of the physical transistor width and the physical gate length were simulated.**

I. Introduction

A statistical analysis of the performance of integrated circuits gains more and more importance when the critical device sizes reach the nanometer range. In fact, there are several process variations that make each transistor in a circuit different from others. The most frequently studied effect is the impact of the random positioning of the doping atoms in the channel regions of CMOS devices [1]. Further effects studied are the impact of grain boundaries in polysilicon and in metal gates [2] and the impact of geometrical fluctuations (line edge roughness) [3]. It should be noted that a very important source of geometrical variations in CMOS technology is the process of optical lithography [4]. The gate length of the state-of-the-art CMOS transistors is currently significantly smaller than the light wavelengths used in conventional optical lithography. Therefore, the diffraction effects are significant and they negatively impact the accuracy of the lithography. In this paper we consider the effects of the distortion of the critical geometrical device dimensions (gate length and channel width) for CMOS technology with a mean gate length of 32 nm due to typical uncertainties in the process of optical lithography. An SRAM integrated circuit was chosen as an example for this study.

II. Lithography Simulations

Photolithographic structuring of active silicon areas and of polysilicon gates was simulated. The Fraunhofer IISB simulation tool Dr.LiTHO [5] was used for the lithography simulation part. All simulations are aerial image based. Therefore, each lithography simulation is divided into three steps: The computation of the mask diffraction spectrum, the aerial image computation and the evaluation of the aerial images. Undercutting of photoresist was taken into account by a fixed etch bias of 13 nm, to achieve the final physical gate lengths of 32 nm for the inner flip-flop transistors and 42 nm for the access transistors. Due to the small lithography target feature sizes down to 45 nm for the presented SRAM example, the mask diffraction spectrum has to be computed rigorously by using a so called rigorous electromagnetic field solver. The areal image simulation, taking the mask diffraction spectrum as input data, is based on an extended Abbe approach. Instead of a full resist simulation a simplified aerial image based threshold model was used for the CD computation of the different SRAM features. For all simulations the following lithography system was assumed: 193 nm water immersion with a numerical aperture of 1.35 and a 4x reduction, a strong off-axis Quasar illumination with 20 degree pole opening angle, a sigma inner/outer of 0.8/0.98 and unpolarized light. In the first step, an attenuated phase shift mask with feature sizes corresponding to the target feature sizes was used. Then a simple OPC was performed: In an optimization loop the mask feature dimensions were modified in order to obtain the target sizes at a focus position of 0 nm on the wafer side. The described system and mask optimization procedure was used for the two simulated lithography steps for the SRAM poly layer and the active n+/p+ layer. In Fig. 1 both layers are shown in one picture (horizontal lines correspond to the poly layer, vertical lines correspond to the active n+/p+ layer). For each layer, shown in Fig. 1, an individual mask and lithography step is required. Figures 2 and 3 show exemplarily the aerial

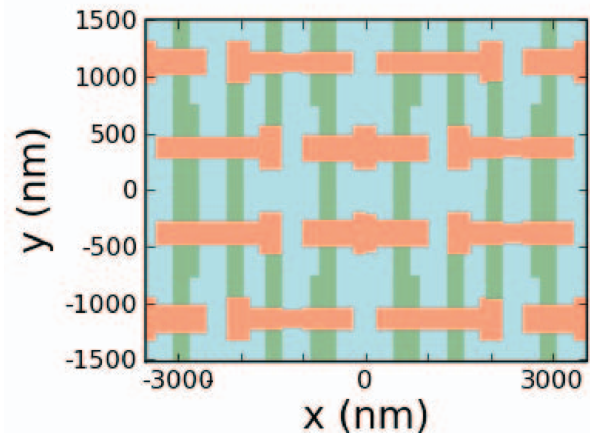

Fig. 1. Mask layout of the poly layer (horizontal lines) and the active n+/p+ layer (vertical lines) without OPC

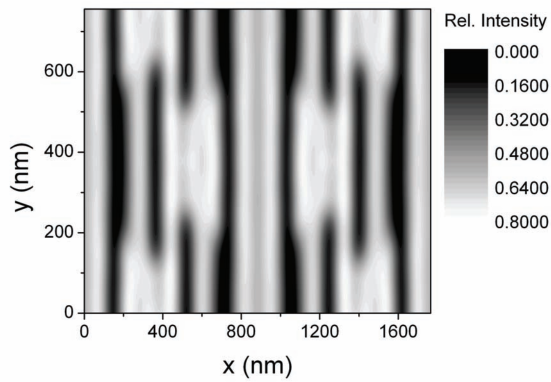

Fig. 2. Aerial image of the active n+/p+ layer exemplarily at a focus position of 0 nm

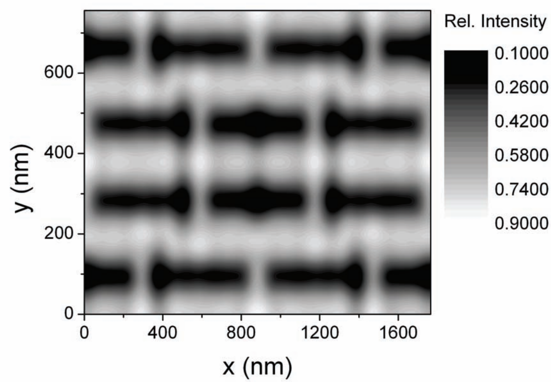

Fig. 3. Areal image of the poly layer exemplarily at a focus position of 0 nm

images of the poly layer and active n+/p+ layer, respectively, at a focus position of 0 nm.

III. Defocus Variation Results

Based on this setup, focus fluctuations were simulated as an example for process variations. A maximum acceptable CD variation of 15 % was assumed in order to guarantee the functionality of the SRAM cell. Due to the described lithography setup this results in a maximum focus variation from -30 nm to +45 nm. The distribution of the focus positions was assumed to be uniform and was varied in 1 nm steps between the limits. In this range the corresponding aerial images of both layers were computed at the resulting 76 different focus positions and all CDs were evaluated at the following feature positions: The poly line CDs in the center of the active n+/p+ regions and the transistor width CDs in the center of the poly lines. Due to the periodic boundary conditions of the used lithography simulation models four neighboring SRAM cells instead of only one cell have to be taken into account in order to obtain a x- and y-periodic mask layout for all computations. This can be seen in the Figs. 1, 2 and 3. The evaluation of the feature CDs was only performed in the upper left cell. Figure 4 shows exemplarily the behavior of the gate length CD versus the defocus. The corresponding distribution functions of the gate length CD and device width CD are plotted in Figs. 5 and 6, respectively. As can be seen, a strongly asymmetric PDF was found for both.

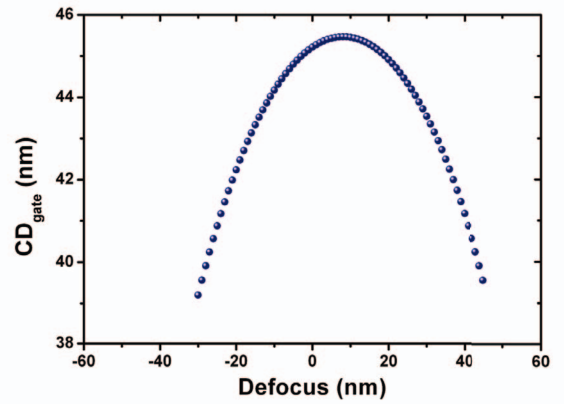

Fig. 4. Bossung plot of the poly line CD without etch bias

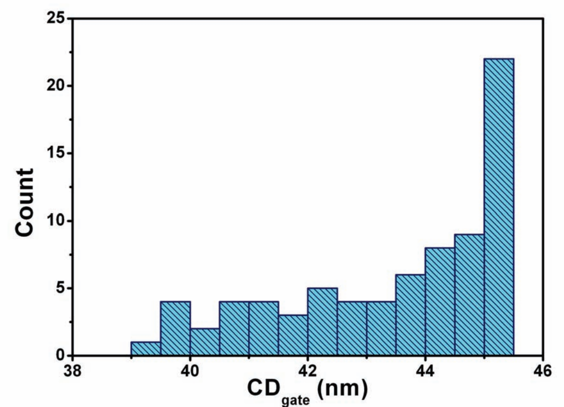

Fig. 5. PDF of the gate length CD without etch bias

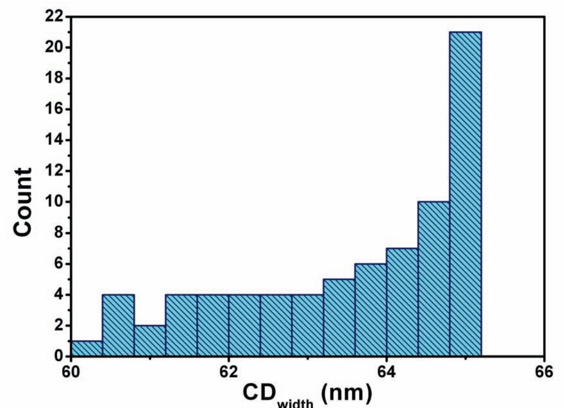

Fig. 6. PDF of the device channel width CD without etch bias

IV. TCAD AND SPICE SIMULATIONS

In this paper, 32 nm single gate FD SOI MOSFETs were chosen for variability investigations. Sentaurus Process and Sentaurus Device [6] were used for the TCAD simulation part. SPICE simulations were done using HSPICE [7]. The oxide thickness of the devices amounts to 1.2 nm, the buried oxide thickness to 20 nm and the silicon body thickness to 10 nm. A heavy ground plane doping was used for short channel effect suppression. Figure 7 shows the geometrical shape and the doping distribution of the NMOS device. Device simulations were undertaken at supply voltages of 1.1 V, to calculate the required single device behaviour. The on-current I_{on} amounts to 1.3 mA/μm and 0.5 mA/μm for the NMOS and PMOS, respectively. The off-currents of both devices, NMOS and PMOS, was calculated to be 1.0 nA/μm at 320 mV threshold voltage. The sub-threshold current drops with a slope of 87 mV/dec. The drain induced barrier lowering (DIBL) was finally calculated to be 77 mV/V.

Based on the TCAD simulation results, SPICE parameters were extracted using the EKV compact model. The extraction method is based on two steps. First of all, several parameters, e.g. low-field mobility, mobility reduction coefficient, long channel threshold voltage, transconductance, and critical electric field are calculated and included in a EKV modelcard. Secondly, additional SPICE parameters are fitted using our in-house SPICE parameter extraction software HARVESTER. After the extraction of the SPICE parameters, additional adjustments of the EKV model were done, to ensure the correlation of the SPICE models and the TCAD models under the influence of process variations. This procedure is presented elsewhere [8].

After the SPICE parameter extraction of the devices was finished, simulations of the initial SRAM cell behavior without variability were performed. The READ static noise margin (SNM) was calculated to be 260 mV at $V_{DD} = 1.1$ V. The READ propagation delay $t_{prop,READ}$ amounts to 169.3 ps by assuming a load capacitance C_{load} of 6 fF connected to each bit-line. The READ process was assumed to be finished if $V_{DD}/2$ was reached. The WRITE delay $t_{prop,WRITE}$ of the SRAM cell was calculated to be 7.2 ps. The WRITE process was assumed to be finished after a one was stored in the cell by assuming that a one is stored if 90 % of the supply voltage was reached.

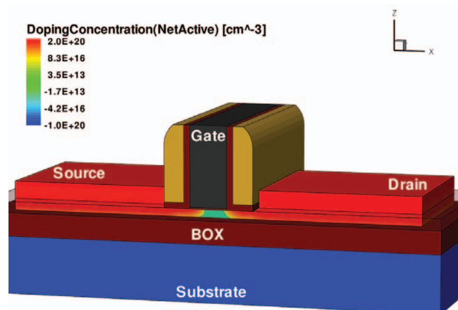

Fig. 7. Shape and doping distribution of the SG FDSOI NMOS

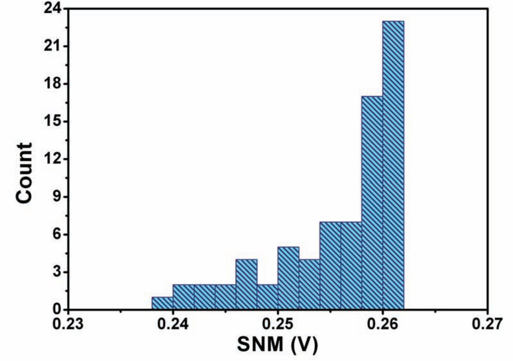

Fig. 8. PDF of the SNM by considering gate length CD variations

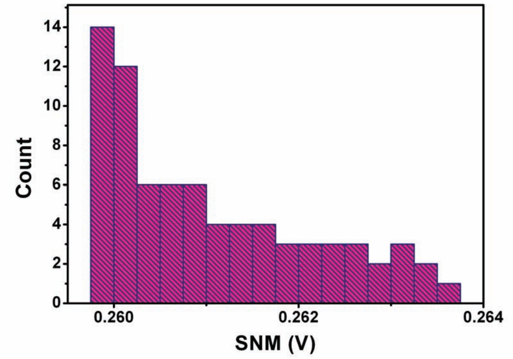

Fig. 9. PDF of the SNM by considering width CD variations

V. CIRCUIT VARIABILITY SIMULATION RESULTS

The calculated CD values of the respective devices of the SRAM cell, resulted from lithography simulations, were used in the SPICE simulations to investigate the SNM in presence of CD fluctuations. Figure 8 shows the probability distribution function (PDF) of the SNM resulted from the variations of the gate length CD. As can be seen, a strongly asymmetric PDF was found for the SNM, comparable to the PDF of the CD (Fig. 5). This result corresponds with earlier work already presented [9]. In contrast, if only the impact of the device channel width variations on the SNM is considered (Fig. 9), the skewness of the resulting SNM distribution changes its sign: most probable SNM is in this case at smaller values. This is because the most probable large values of device widths (Fig. 6) result in smaller values of the SNM (Fig. 9). In general, the SNM of the SRAM cells is determined by a so called β ratio which is equal to the relation of the currents of the pull-down transistors and access transistors. The relative 3σ variation of the SNM caused by ΔW_{gate} amounts to only 1.2 %, while L_{gate} variations cause a relative 3σ of 6.96 %. Figure 10 shows the butterfly characteristic spread calculated from applying both, gate length CD variations and device width CD variations on the SRAM cell. As can be seen, only a moderate impact of layout variations resulted from lithography parameter fluctuations on the static SRAM cell behavior is observed with a relative 3σ of 7 %.

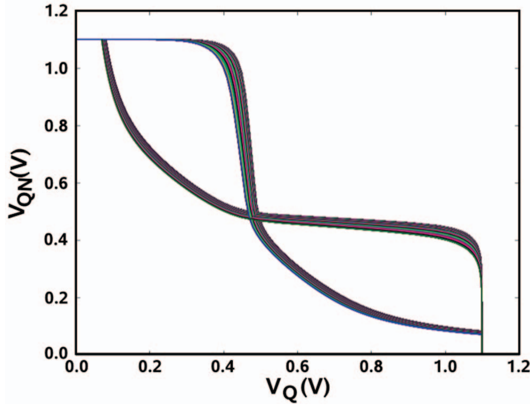

Fig. 10. Butterfly characteristics by considering gate length CD and device width variations

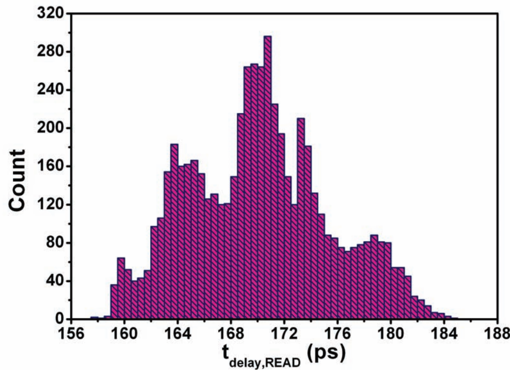

Fig. 11. PDF of the READ delay by considering gate length CD and width CD variations

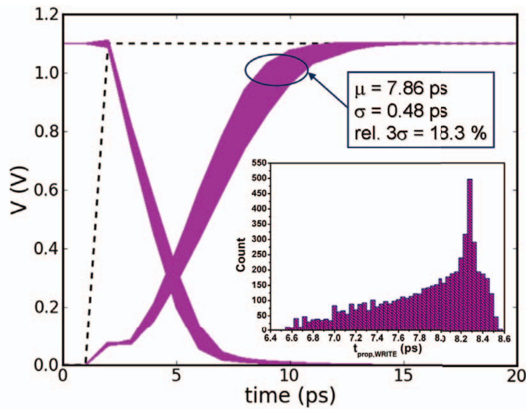

Fig. 12. Write characteristic by considering gate length CD and device width variations

Next, the influence of lithography resulted layout variations on the dynamic READ and WRITE performance was studied. Figure 11 shows the PDF of the READ delay considering both layout variations, ΔL_{gate} and ΔW_{gate}. Compared to the PDFs of the READ SNM in dependence on ΔL_{gate} and ΔW_{gate}, the asymmetry of the READ delay $t_{\text{prop,READ}}$ was found to be less strong. This results from the different algebraic sign of the skewness caused by gate length variations and n+/p+ regions width variations, respectively. Due to the superposition of both effects, the PDF of the dynamic READ performance tends to a more Gaussian like behavior. The relative 3σ of the READ delay was calculated to be $9.36\,\%$.

Figure 12 finally shows the spreading of the dynamic WRITE delay of the SRAM cell by considering both kind of lithography resulted layout variations. Here, we observed the strongest influence of lithography variations on the electrical performance. Due to the fact that the bit-lines do not change their voltage value in this mode, the impact in the case of the dynamic WRITE mode is determined by transistor performance. The relative 3σ of $t_{\text{prop,WRITE}}$ was calculated to be $18.3\,\%$.

VI. Conclusion

A coupling of lithography simulations, TCAD simulations, and SPICE simulations was realized. Lithography simulations of a two layer SRAM cell layout were performed, including the influence of defocus variations. The resulted CD values were used in SPICE simulations to study the impact of defocus variations on the static and dynamic behavior of 6-T SRAM cells. A strongly asymmetric probability density function of the static noise margin was observed, if either gate length variations or gate width variations are considered, but with a different algebraic sign of the skewness. The superposition of the different sources of variability lead to a more symmetrical PDF of the dynamic READ delay. The strongest influence of lithography induced layout variations was observed for the dynamic WRITE delay with a relative 3σ of $18.3\,\%$.

Acknowledgment

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