

Compact Process and Layout Aware Model for Variability Optimization of Circuit in Nanoscale CMOS

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Abstract—A predictive MOSFET model is very critical for early circuit design in nanoscale CMOS technologies. In this work, we developed a new compact MOSFET model which can dramatically improve the predictability of BSIM4 for the major 3 process and 2 layout variations by applying the simple physics-based equations to model these parameters. The accuracy of the model is verified using numerical TCAD simulation results and measurements under full range of temperature and bias conditions. The compact model for the circuit simulation can be efficiently used to predict the effects of process and layout variations on the circuit characteristics.

I. INTRODUCTION

The process and layout variability has increasingly a significant impact on the device and circuit characteristics for nanoscale CMOS technologies. To handle the impact of these variations, a corner-based model has been traditionally used in circuit simulation. However, due to the lack of the physical scalability of BSIM4 and PSP which are the industry standard, the simulation can not reflect accurately the variations. In recent years, several efforts to overcome this problem have been proposed [1-2]. But, the model of Nagumo et al. [1] focused on the connections between threshold voltage related parameters and channel doping profile. Therefore, it was not enough to predict the circuit performances despite its physics-based approach. On the other hand, Tirumala et al. [2] proposed the modeling method for circuit simulation by using numerical TCAD. However, the model was fully generated by empirical equations.

This paper presents a compact process and layout aware model (PLAM) for circuit simulation. Our model is developed by incorporating the simple physics-based equations which link the process and layout factors with the model parameters of BSIM4. In addition, the equations are generated for both dc and ac characteristics, and provides the predictive method for accurate circuit simulation with various bias voltage and temperature conditions. In this work, the key variation factors are selected by sensitivity analysis and modeled by SPICE sub-circuit statements.

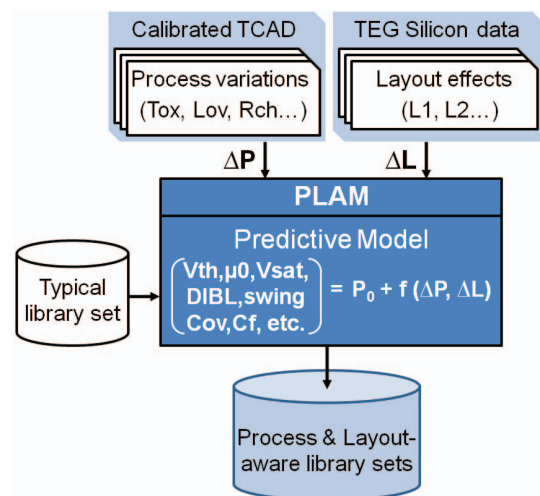


Figure 1. Methodology of development for the process layout aware modeling. The predictive model includes some simple physics-based equations to model process variations and layout effects.

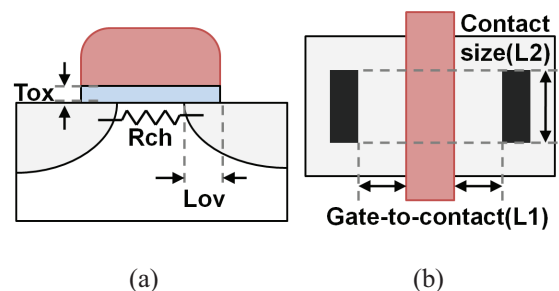


Figure 2. The major variable parameters of (a) process and (b) layout in this work.

Because the model equations are based on the physical correlation with each process parameter, it allows to optimize for targeting process with minimum effort. These predictive models connect manufacturing to circuit design, so that measurable process variations or layout factors can be fed into circuit design.

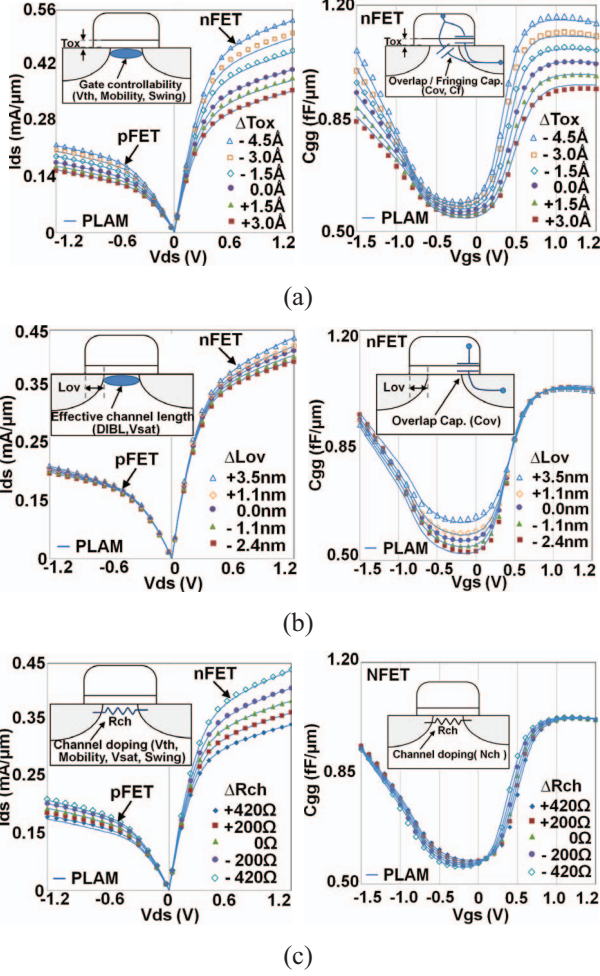


Figure 3. Id-Vd curve and gate capacitance with varying (a) Tox, (b) Lov, and (c) Rch. Our model (lines) and numerical TCAD simulation (symbols) are in good agreements for both nFET and pFET.

II. MODELING

A. Methodology and Major Variations

Fig. 1 shows the methodology of development for the PLAM. The methodology is based on the TCAD simulation because it allows to analyze the effects of each process variation on device and has cost effectiveness compared to experimental wafers. In this work, gate oxide thickness (Tox), gate to drain/source overlap length (Lov), and channel doping concentration (Nch) are modeled by using the TCAD simulation as shown in Fig. 2 (a). Although the TCAD is the ideal method for analysis the impact of various parameters on device, some parasitic or 3-dimensional layout effects can be measured accurately in the test element groups (TEG) of silicon wafers. Distance between gate and contact (L1), and contact size (L2) are modeled by using the TEG data as shown in Fig. 2 (b). Firstly, the electrical characteristics for the process and layout variations have been obtained from simulations and TEG measurements. Based on the data, new physics-based equations are generated as the function of each variable, and added on the selected BSIM4 model parameters. Finally, the new model library set is reconstructed for predictive circuit simulation.

Above all, one of the most important things is to find the certain model parameters which have physical meaning related with each variation factor. In next section, the

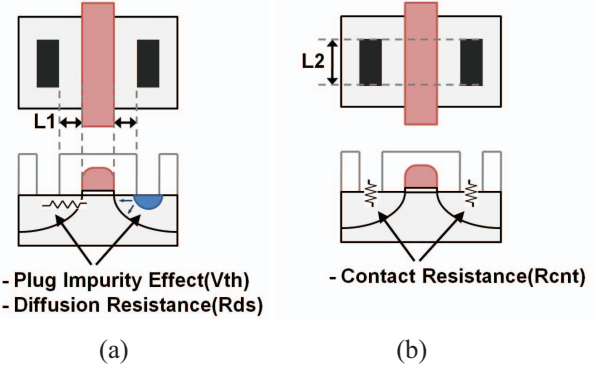


Figure 4. Layout effects of (a) distance between gate and contact, and (b) contact size.

specific modeling method and the physical causes will be explained.

B. Process Layout Aware Modelings

Table. I summarizes the equations and the BISM4 model parameters for PLAM.

Gate oxide thickness variation (ΔTox) causes the shift of oxide capacitance (Cox) and vertical electric field as well as channel controllability. This means threshold voltage, mobility and leakage current are changed. Changing Cox also causes threshold voltage shift and channel controllability variation [3]. Threshold voltage and subthreshold slope can be derived from these physical correlations in (6) and (9). Due to the universal relationships with the bulk and inversion charge density [4], the low field mobility has been modified as a function of gate drive voltage in terms of the oxide thickness as shown in (7). Because gate to drain/source overlap and inner fringing capacitances are closely related with Cox , ac parameters are modeled in (14) and (15). Fig. 3 (a) shows the predictive ability of these model equations for drain current and gate capacitance.

Gate to drain/source overlap length offset (ΔLov) is one of the main factors that can lead to performance variation of nanoscale CMOS. Effective channel length is directly affected by Lov as shown in (2). Because of its important role in short channel transistors [5], the parameters related to drain-induced barrier lowering and velocity overshoot have to be modified as a function of Lov in (8) and (11). Overlap capacitance is also changed with Lov. Therefore, (14) describes the Cov dependent on Lov variation. Fig. 3 (b) demonstrates the model is in good agreement with the results of numerical TCAD simulation.

The fluctuation of channel doping concentration (ΔNch) is another major process factor. There is growing concern about the random dopant fluctuation of nanoscale transistors. Not only parameters related to the on-current characteristics, such as Vth , body factor, and mobility, but also the off-current parameters have to be considered. In the PLAM, ΔNch is expressed as a function of the channel resistance in (3). Equations (6), (7) and (10) are derived from physical relationship between Nch and depletion charge density. Equation (11) represents the effect of impurity scattering on carrier velocity. Leakage current model due to the channel controllability deviation is also included in terms of ΔNch as

TABLE I. EQUATIONS FOR COMPACT PROCESS LAYOUT AWARE MODEL (1)–(15)

PLAM Eqs.(1)-(6)	BSIM4	PLAM Eqs.(7)-(10)	BSIM4	PLAM Eqs.(11)-(15)	BSIM4
$Tox = tox_0 + \Delta tox$	(1) TOX	$\mu = \mu_0 + \frac{p2 \cdot \exp(-\sqrt{N_{ch}}(\Phi_F - V_{BS}))}{V_{GS} - V_{th0}} \cdot \frac{\Delta tox}{Leff}$		$V_{sat} = v_{sat0} + p6 \cdot \left(\exp\left(-\frac{\Delta lox}{Leff}\right) - 1 \right)$	
$Leff = leff_0 - \Delta lox$	(2) LINT DLC	$+ \frac{p3 \cdot \exp(-\sqrt{N_{ch}}(\Phi_F - V_{BS}))}{V_{GS} - V_{th0}} \cdot \frac{tox}{Leff}$ (7)	U0	$+ p7 \cdot \left(\exp\left(-\frac{\Delta nch}{Leff}\right) - 1 \right)$ (11)	VSAT
$Nch = nch_0 + \Delta nch^{*1}$	(3) NDEP	$DIBL = DIBL_0 \cdot p4 \cdot \log\left(1 + V_{dd} \cdot \frac{\Delta lox}{Leff}\right)$ (8)	ETA0	$Rds = rds_0 + p8 \cdot \Delta L1$ (12)	RDW RSW
$\Delta X1 = X1 - X1_{D/R}$	(4) .	$Swing = Swing_0 + 2.3 \frac{kT}{q} \cdot \frac{(3 \cdot \Delta tox)}{W_{dm}}$		$Rcnt = rcnt_0 + p9 \cdot (\exp(-\Delta L2) - 1)$ (13)	RDC RSC
$\Delta X2 = X2 - X2_{D/R}$	(5) .	$+ 2.3 \frac{kT}{q} \cdot \frac{3 \cdot tox}{\sqrt{2\epsilon_s V_{bi}}} \cdot \left(\sqrt{q \cdot \Delta nch} \right)$ (9)	NFACTOR	$Cov = cov_0 + p10 \cdot \epsilon_{ox} \cdot \Delta tox$	
$V_{th} = v_{th0} + \frac{\sqrt{2\epsilon_s q N_a \phi_s}}{\epsilon_{ox}} \cdot \Delta tox$				$+ (\epsilon_{ox}/Tox) \cdot \Delta lox$ (14)	CGDO CGSO
$+ \Delta V_{FB}^{*2} + \Delta 2\Phi_F^{*3} + \frac{\Delta Q_d^{*4}}{C_{ox}}$				$Cf = cf_0 - \frac{2 \cdot \epsilon_{ox}}{\pi} \log(1 + p11 \cdot \Delta tox)$ (15)	CF
$+ p1 \cdot \left(\exp\left(-\frac{\Delta L1}{Leff}\right) - 1 \right)$	(6) VTH0	$\gamma = \gamma_0 + p5 \cdot \frac{\sqrt{2\epsilon_s q \cdot \Delta nch}}{C_{ox}}$ (10)	K1		
$^{*1} \Delta nch = p0 \cdot (rch - rch_0)$ $^{*2} \Delta V_{FB} = \Phi_F(nch) - \Phi_F(\Delta nch)$ $^{*3} \Delta 2\Phi_F = 2 \frac{kT}{q} \left\{ \ln \frac{(nch + \Delta nch)}{n_i} - \ln \frac{(nch)}{n_i} \right\}$ $^{*4} \frac{\Delta Q_d}{C_{ox}} = \frac{T_{ox} \cdot \sqrt{2\epsilon_{ox} \phi_s}}{\epsilon_{ox}} \left\{ \sqrt{(nch + \Delta nch) \cdot (2\Phi_F(\Delta nch))} - \sqrt{(nch) \cdot (2\Phi_F(nch))} \right\}$ $\times p0 \sim p11$: Sensitivity coefficients depending on MOSFET type					

shown in (9). Results of Nch model compared to numerical simulation data are illustrated in Fig. 3 (c).

Gate to contact distance (L1) is a layout parameter which causes stress effect or doping fluctuation in the channel region. Because the contact plug impurities affect

the doping profile in channel region as shown in Fig. 4 (a), Vth can be modulated. As the contact is moved, diffusion resistance between gate and contact is also changed. Therefore, (6) and (12) is included to reflect these layout effects.

The effect of contact size (L2) is examined as shown in Fig. 4 (b). The drain current can be affected by contact size because the total size is closely related with contact resistance. Therefore, equation (13) is included to express the contact resistance dependent on its size.

III. RESULTS

Our model has been implemented by sub-circuit statements and simulated in SPICE. The simulation results of Vth, Ion and Idoff are compared to the numerical TCAD results and measurement data as shown in Fig. 5 (a)-(c) and Fig. 6 (a)-(b). These results demonstrate excellent matching of the PLAM for the wide range of variation. Especially, our model predicts the on-current characteristics as well as the off-current characteristics under various bias voltages and temperature conditions. With some sensitivity coefficients fitted to various device data, the PLAM accurately predicts trends in circuit performance for process variations. Fig. 7 compares the PLAM and numerical simulation results for the transfer curve of an inverter. In this simulation, Tox, Lov and Rch variations are assumed to be worst case, +1.6Å, -2nm, and +150ohm respectively. It shows the PLAM make

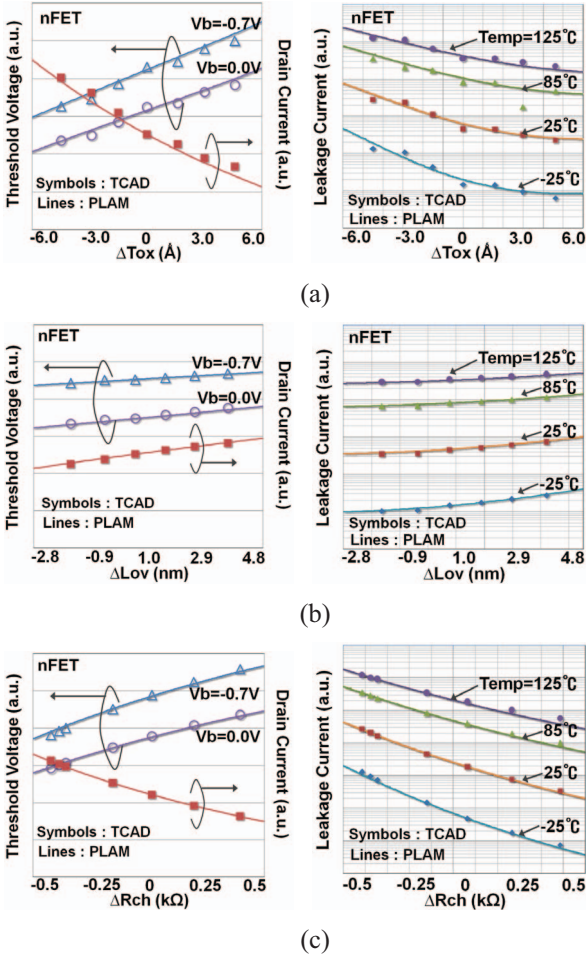


Figure 5. Vth, Ion and Idoff versus process variations (a) Tox, (b) Lov, (c) Rch. Our model (lines) and numerical TCAD simulation (symbols) are in good agreements among various bias and temperature conditions.

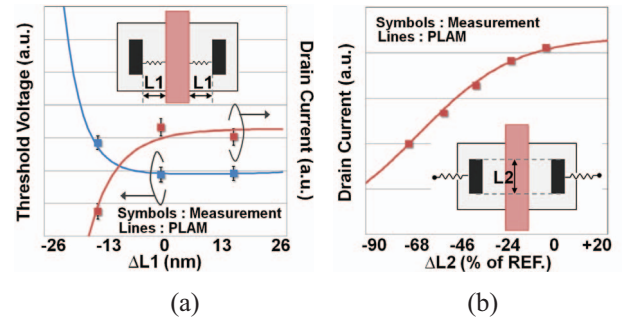


Figure 6. Layout effects of (a) distance between gate and contact, and (b) contact size.

an accurate estimate of switching point in transfer characteristics of an inverter. In Fig. 8, the propagation delay of ring oscillator can be also predicted with 95% accuracy under various supply voltage conditions, while BSIM4 has a poor accuracy. These results show the proposed model can be used to reflect the effects of process variations on circuit performance.

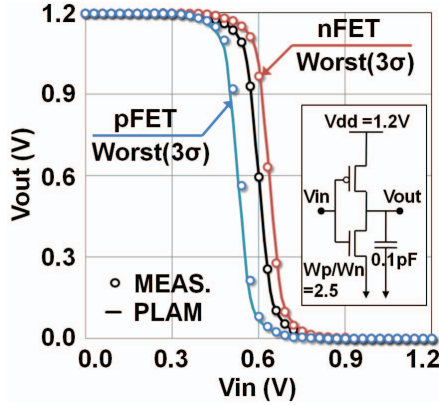


Figure 7. Transfer curves of measurement (symbols) and model prediction (lines) at 3σ corner.

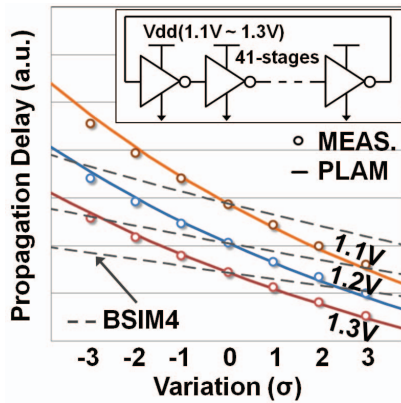


Figure 8. Propagation delay variation of 41-stages ring oscillator. Our model adequately predicts the circuit performance in overall supply voltage conditions, whereas the BSIM4 does not follow measured data.

IV. CONCLUSION

A compact process and layout aware model was presented for the variability optimization of the circuit performance. For the key variation factors, our model predicts the device and circuit characteristics with an excellent accuracy. The proposed model allows direct access to process variations in circuit design level and provides an insight into the relationship between fabrication and circuit design.

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