A comparative 3D simulation approach with extensive experimental Vt/Avt data and analysis of LER/RDF/reliability of CMOS SRAMs at 40-nm node and beyond

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***Abstract*— With the advent of CMOS SRAMs manufactured at 40-nm node and beyond, variability of threshold voltage (Vt) and technology-dependent factor in Pelgrom plot (Avt) has become a serious issue in the practical design and fabrication phases. This paper presents (i) a comparative 3D simulation approach using extensive measured data to clarify the magnitudes of LER and RDF effects in generic processes, (ii) estimation of magnitudes of LER, RDF and FER (metallurgical junction front edge roughness) effects, (iii) simulation of LER, RDF and FER in a FinFET device to evaluate practical feasibility and (iv) analysis of size-dependent NBTI-induced Vt fluctuation as a possible application of this method.**

I. INTRODUCTION

The continuous miniaturization of CMOS SRAMs down to 40-nm node has led to significant changes in process and device design, and has made variability and reliability issues crucial[1]-[3]. The importance of Vt roll-off and Avt control has increased greatly in the actual design and fabrication phases. We have proposed a comparative 3D simulation approach using extensive measured data, and have clarified the magnitudes of LER and RDF effects in generic processes. We used this approach in actual practice to evaluate LER/RDF effects and to provide practical feedback. In order to do this, we paid special attention to (1) net number and spatial distribution for the impurities and trap site, (2) regridding around the metallurgical junctions to preserve the fluctuation, and (3) intensive optimization of process models.

II. FLOW OF COMPARATIVE 3D SIMULATION APPROACH

The flow of the comparative 3D simulation approach is presented in Fig. 1. With regard to impurity and trap site distributions in scaled devices, in addition to the random location it is necessary to pay attention to net-number fluctuation. It is noticed that the net-number of impurities is definitely fluctuated in individual area, particularly in the halo region as can be seen in the figure. Basic frame of simulation tool which we used is 3D Sentaurus process/device produced by Synopsys.[4] Before using the process simulator in actual practice, we intensively examined experimental data for B, As, P, In, and Ge from more than 60 sources in the literatures[5] and we optimized models for scaled device design phase. We implemented LER model based on Kaya's method[6]. We also confirmed that the results produced by our random-number-based variability simulator were consistent with the results of our experimental data acquisition procedure (eqs. 1 and 2) as shown in Fig. 2, where P means an observable and herein the value is a threshold voltage Vt of transistor. The value of ΔP is a difference of Vts in an adjacent neighbor pair of transistors. L, W and D are channel length, channel width and distance in neighbor pair

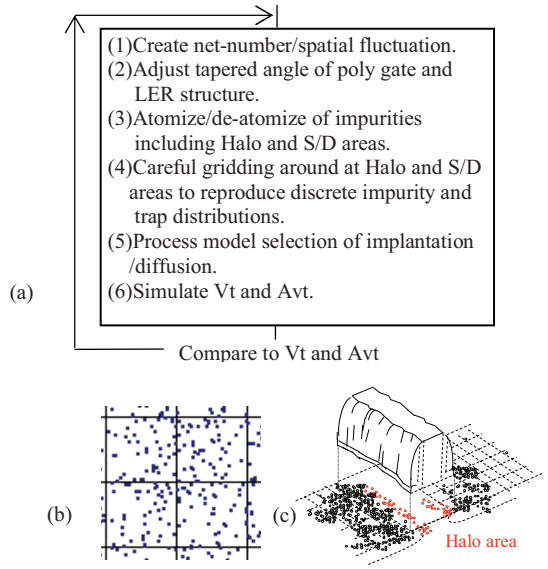

Fig.1 Schematic illustration of comparative 3D simulation approach. (a)Successive simulations are done with tuning of items (1) to (6) until obtaining well-reproduced results. (b) net-number/spatial fluctuation for impurity and hole trap, and (c) typical image of discrete atoms around at Halo and S/D edge areas.

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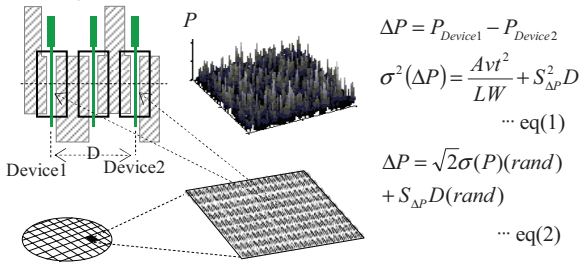

Fig.2 Procedures of variability measurements on paired transistors over whole wafers. Simulation results using random number have been checked to be consistent to experimental procedures.

transistors, respectively. Moreover, Avt which we focus is a linear coefficient of Pelgrom plotting.

III. SHIMULATED AVT, METALLUGIVCAL JUNCTION FRONT EDGE ROUGHNESS AND FEASIBILITY STUDY OF FIN DEVICES

We would like to herein report our simulated characteristics of Avt, junction edge roughness, feasibility study of Fin devices and preliminary work of size dependent NBTI-induced Vt behaviors using our comparative 3D simulation approach.

A. Vt roll-off and Avt characteristics

As a part of variability work, we have studied Vt roll-off simulation in terms of process models by two- and three-dimensional executions. The typical simulated Vt for saturation regions are plotted for various adopted models with experimental data in Figs. 3(a) and 3(b). As can be seen, the Vt roll-off characteristics depend on adopted models and reproduce well experimental data together with LER/RDF models and Monte Carlo ion implantation model. Moreover, it is understood from Fig. 3(b) that two-dimensional calculation (blue diamond symbol) can not trace the roll off at all.

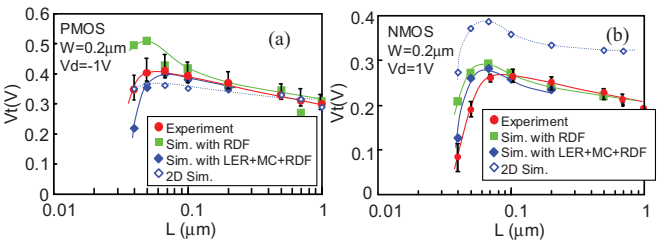

Fig.3 Vt roll-off in terms of adopted models for (a)PMOS and (b)NMOS in saturation region. Each symbol on observed curves stands for value averaged over 40 experimental points.

We have also intensively examined individual impurity distribution with three dimensional visual aids. Fig. 4 shows the simulated impurity distributions for various adopted models. Fig. 4 (a) shows a result with taking into accounts of both RDF, LER and Monte Carlo ion implantation. Some parts of channel areas are observed narrower which result in Vt roll-off as reported in Fig. 3. As shown in Fig. 4(b), front edge of metallurgical junctions has become rough caused by RDF effect though the gate line edge is straight completely. The FER effect increases the variability similarly to LER.

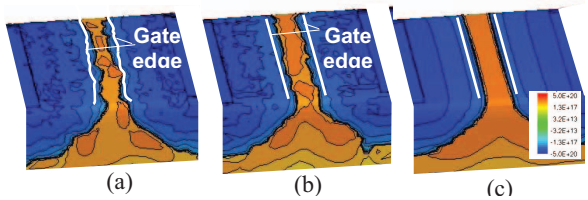

Fig.4 Typical simulated impurity distributions underneath gate area (a) taking into accounts of both RDF, LER and Monte Carlo ion implantation., (b) RDF, and (c) continuum models. L_{poly} is of 40 nm.

The values of the standard deviation of threshold voltage (σVt) are plotted in Fig. 5. A value of Avt is a linear coefficient shown in the inset of the figure.

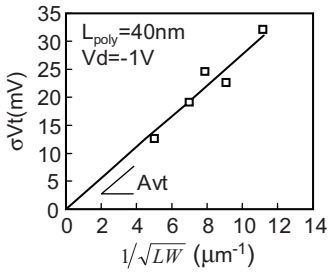

Fig.5 Typical Pelgrom plot of simulated threshold voltages.

Avt values are important indices for scaled CMOS SRAM. We have studied Avt characteristics in both linear and saturation regions for PMOS and NMOS. Hereupon, we have focused on saturation region characteristics, since LER, RDF and FER effects would be markedly appeared in device behaviors. The simulated Avt-L_{poly} characteristics for PMOS are shown in Fig. 6 for the different models together with experimental data. The L_{poly} length(L) and the channel width(W) were varied from 40 nm to 1μm and 0.2μm to 2μm, respectively. It has been observed from the experiment that Avt data depend on L_{poly} definitely. Comprehensive comparison of the simulated and experimental results revealed that RDF effects in halo region caused by discrete impurity atom fluctuations are dominant in Avt variability over a range of L_{poly} of 0.1 to 1μm. In the shorter L_{poly} range of 40 nm to 0.1μm, it was revealed that FER effect and local dose fluctuations of halo implantation process overlay on RDF effect. As a result, the Avt value increases with decease in

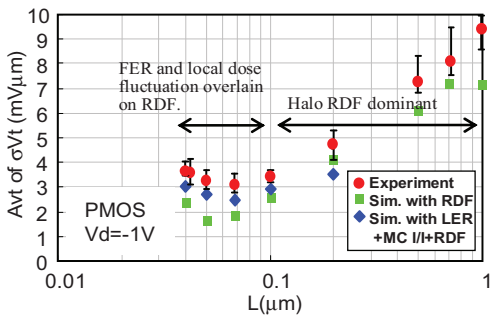

Fig.6 Avt characteristics of σVt in PMOS. The standard deviation of LER is of 2nm. Simulations have been done with three dimensional.

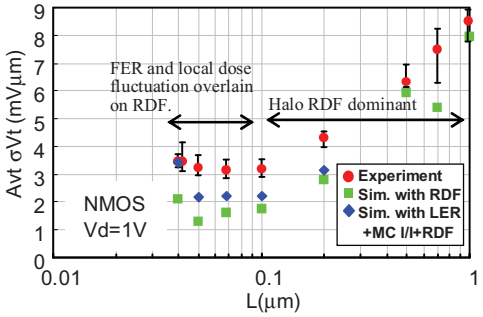

Fig.7 Avt characteristics of σVt in NMOS.

L_{poly} as can be seen in Fig. 6. We can also discuss same analogy to NMOS, however, there is still a small discrepancy between simulated and experimental results as shown in Fig. 7. In order to improve the discrepancy, we have studied intensively several features such as (i)to develop precise tilted BF_2 implantation and dissociation models, (ii)to observe precise gate edge structures in especial NMOS with n^+ re-crystallized poly-silicon involving various orientations, and (iii)to estimate work function variability caused by re-crystallized poly silicon orientation fluctuation in NMOS.

B. Feasibility study of Fin devices and size dependent NBTI-induced Vt fluctuation

Fin device is one of promising candidates for 32- to 22-nm-node CMOS SRAMs. Employing a typical published process[7], we used our simulation tool to evaluate LER, RDF and FER effects. Fig. 8(a) shows a typical intermediate output structure of FinFET SRAM cell in which we can see narrow walls of poly-Si/Si_3N_4. We have carefully optimized ion implantation process, particularly to S/D areas in a whole process sequence of Fin SRAM, because ion implantation angle margins (tilt and rotation angles) are markedly limited due to tall photo resist walls. Some of dimensions of the Fin are listed on Table 1. A magnification of the transistor is given on Fig. 8(b). We have examine two kinds of LER; gate LER shown in Fig. 8(c-1) and Fin LER in Fig. 8(c-2). Typical four simulated results of impurity distributions with the gate LER are shown in Fig. 9(a), where S/D metallurgical junction front edges have been seen. 3D current distributions are also given on Fig. 9(b) for four typical Fins with the Fin width LER. Summary is listed on Table 1. Although junction front edge roughness has been seen in Fig. 9(a), variability of Vt have been improved on both gate LER and Fin LER shown in Table 1. The Vt variability characteristics could be interpreted in terms of well-controllability of current by dual gate in Fin device.

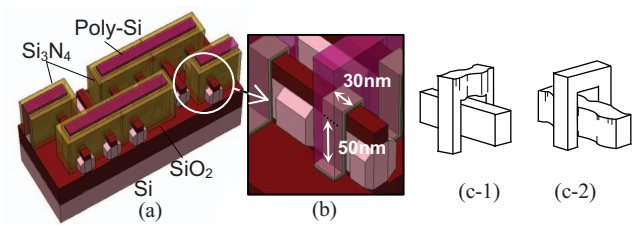

Fig.8 FinFET structure for simulation. (a) Snap shot of cell structure for ion implantation process, (b) magnification of Fin devices, (c-1) gate LER, and (c-2) Fin LER.

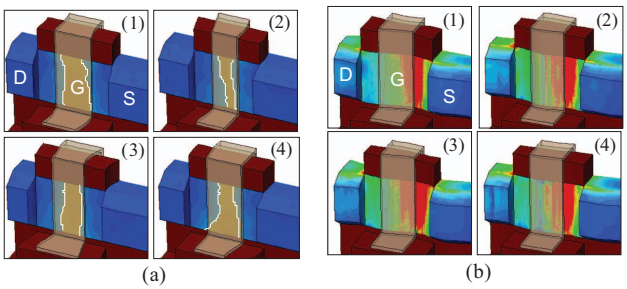

Fig.9 Typical four simulated results of LER and RDF. (a)Impurity distribution at S/D in case c-1, and (b)current distribution for saturation conditions in case c-2.

Table 1 Comparison of simulated results of Fin device with planar device. Simulation has been done at Vd=-1.0V. Symbol of * stands for mean value.

		Fin FET	Planar MOS
L		30nm	40nm
W		50nm×2	0.2μm
Fin width		20nm	-----
Channel concentration		1e18 /cm^3	2e18/cm^3
Gate LER +RDF	σVt	30mV(0.31V)*	34mV(0.17V)*
	σIon	3.6μA(72.1μA)*	5.5μA(106μA)*
	σIoff	4.4e-11A(2.7e-11A)*	-----
RDF	σVt	15mV(0.35V)*	27mV(0.495V)*
Gate LER	σVt	22mV(0.35V)*	-----
Fin LER	σVt	12mV(0.35V)*	-----

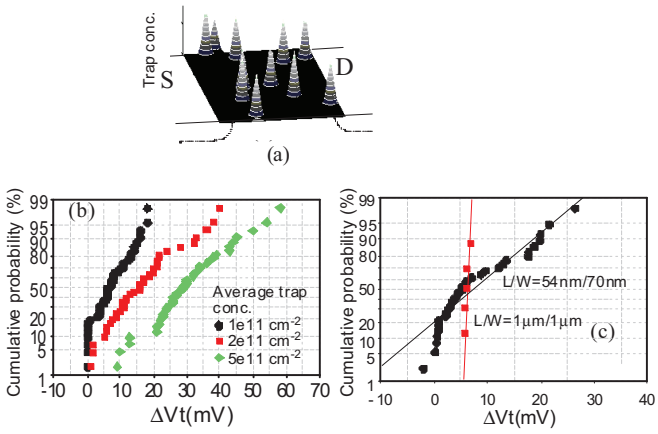

Fig.10 NBTI results for PMOS stressed with Vgs=-1.4V and Vd=0V at 125ºC. (a) Net-number/spatial fluctuation for hole trap, (b) preliminary simulation results for three different stress durations(L/W=40nm/0.2mm), and (c) experimental results of size dependence of Vt degradation.

NBTI(negative bias temperature instability) is one of major issues in scaled CMOS SRAM. Several works such as physical NBTI mechanism discussion, process feedback for

dielectric film improvements and so on have been already reported in many literatures[8]. Herein we have focused on size dependence of NBTI-induced Vt degradation fluctuation estimation from a view point of device reliability. We have called upon our tool with net-number/spatial fluctuations of impurity and trap sites for this job. We have simulated fluctuation of Vt degradation (σVt) on the assumption that both hydrogen passivation and depassivation reactions are Poisson processes[9]. As shown in Fig. 10(a), traps have been scattered at channel area based on the net-number and the spatial fluctuation functions. Preliminary results of σVt variability in a small device of L/W=40nm/0.2um are shown in Fig. 10(b), which can be seen reproduced well qualitatively the experimental curve of small size device of L/W=54nm/70nm shown in Fig. 10(c). Using this simulation procedure in conjunction with LER/RDF/FER effects, we could predict more realistic NBTI-induced Vt variability and also discuss reliability including worst-case scenario of scaled CMOS SRAM.

IV. SUMMARY

We have presented a comparative 3D simulation approach based on extensive measured Vt/Avt data in order to evaluate LER/RDF/FER effects in actual practice and to provide feedback. Through intensive examinations of impurity implantation/diffusion models and customizations and creation of net-number/spatial fluctuation, we have reproduced well Vt/Avt characteristics and have discussed individual magnitude of LER/RDF/FER effects. Moreover, we have reported variability of Fin device as one of promising candidates for 32- to 22-nm-node CMOS SRAMs. Furthermore, using our three dimensional tools with net-number/spatial fluctuations of impurity and defect sites, we have simulated size dependent NBTI-induced Vt fluctuation as a possible application for device reliability

V. ACKNOWLDGE

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