Cost-Effective Variability Reduction Approaches to Enable Future Technology Nodes

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ABSTRACT

This paper will describe a comprehensive study of the primary sources of variability and their effects on active devices, interconnect and ultimately product performance and yield. We will first provide an overview of process variability sources and the resulting random and systematic variability down to 28nm. Next we will present the evolution of yield loss mechanisms and characterization methods for assessing process-design interactions with a focus on layout printability for 28nm and below. To overcome the impact of such a high level of variability on product performance, circuit designers should adopt advanced statistical process characterization, performance verification and optimization techniques. We will describe robust design methodology requirements based on statistical optimization approaches with realistic process/device characterization for logic, memory and analog circuits. We will then present an extremely regular layout methodology for 28nm and below. The key to the practical implementation of this methodology is the creation of a design fabric with a limited number of printability friendly patterns that enable the co-optimization of circuit, process and design. We will demonstrate that this methodology will enable future technology nodes utilizing current generation lithography while minimizing cost per good die.

978-1-4244-7700-5/10/$26.00 ©2010 IEEE