Numerical investigation of the total SOA of trench field-plate LDMOS devices

S. Poli, S. Reggiani, G. Baccarani, E. Gnani, A. Gnudi,
ARCES and DEIS, University of Bologna
Bologna, Italy, email: spoli@arces.unibo.it

M. Denison, S. Pendharkar, R. Wise
Texas Instruments, Inc.
Dallas, Texas

***Abstract*— A numerical investigation of electrical and thermal properties of a lateral trench field-plate (TFP) LDMOS is proposed. Beside the advantage in terms of specific on-resistance (R_{SP}) vs. breakdown voltage (V_{BD}) trade-off, achieved with a proper optimization of the geometrical and doping parameters, the use of deep trenches is discussed here with particular attention to their impact on the electrical safe-operating area (SOA), hot-carrier stress (HCS) reliability, self-heating effects (SHE) and thermal SOA.**

I. INTRODUCTION

Recently, different architectures have been proposed to optimize the performance of lateral double-diffused power MOSFETs (LDMOS) for high voltage applications (breakdown voltage in the 20─100 V range). The use of dielectric RESURF [1] or of lateral trench field plates [2, 3] has been proposed as a cost efficient methodology to improve the specific on-resistance (R_{SP}). Even though experimental demonstration of their applicability has been given [1-3], no thorough investigation has been proposed on the use of deep trench oxides and their impact on the thermo-electrical properties of the device and just little information has been given for hot-carrier stress (HCS) reliability [4].

In this work we focus on a 3D lateral trench field-plate LDMOS (TFP-LDMOS) as a promising solution among those presented in literature. A thorough numerical investigation of the performance of this device concept is given, and, for the first time, a TCAD-based analysis of the key issues for smart power applications, namely, electrical safe-operating-area (SOA), hot-carrier stress reliability and self-heating effects (SHE) in pulsed regime behavior, is addressed, with the final purpose of characterizing the total SOA of the TFP-LDMOS.

II. DEVICE CONCEPT AND NUMERICAL METHODS

Fig. 1 reports the 3D schematic view of the n-channel TFP-LDMOS transistors investigated in this paper. The device structure can be considered as a layout variation of a standard STI-based LDMOS device, from which the doping profiles have been derived [5]. Along the drift region, laterally interleaved silicon fingers and deep oxide trenches are introduced and they represent the key feature of the architecture. MOS capacitor-like structures are thus created filling the trench with polysilicon and biasing it through the gate. The obtained lateral depletion effect in the silicon finger is capable of protecting the device at large drain voltages (V_{DS}), and allows for having higher n-well doping levels without affecting the device breakdown voltage (V_{BD}). In addition, the oxide trench vertically extends deep to the p-substrate, obtaining a uniform vertical distribution of the current flow. The sketch reports also the main geometrical features that will be considered as design parameters for the optimization of the device performance, namely, the drain-side spacing between the polysilicon-trench edge and the drain contact (ΔL_D), the source-side spacing between the polysilicon-trench edge and the source contact (ΔL_S), the overlap between the polysilicon gate and the lateral oxide trench (ΔO_V), and, finally, the oxide and silicon finger widths, W_{OX} and W_{SI}, respectively. Beside those geometrical parameters, an optimization of the n-well doping dose (N_D) has been also considered.

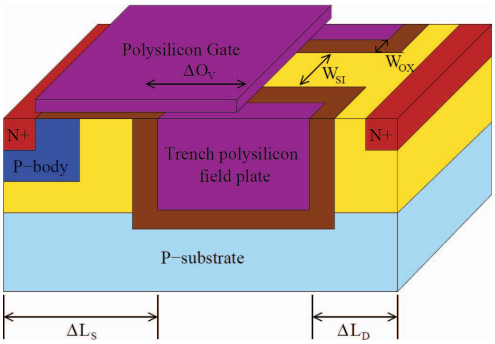

Figure 1. 3D sketch of the TFP-LDMOS. A deep trench oxide is assumed, filled with the polysilicon gate. The field plate can laterally extend to fully or partially cover the total length of the device. The layout parameters used for the device optimization are reported.

From the numerical point of view, 3D simulations have been carried out using the electro-thermal model available in the Sentaurus-Device tool by Synopsys [6], which couples the drift-diffusion transport equations with the heat transfer equation. The symmetric feature of the structure has been considered to define the device unit cell extending half pitch, from source to drain, and half width, from the center of the

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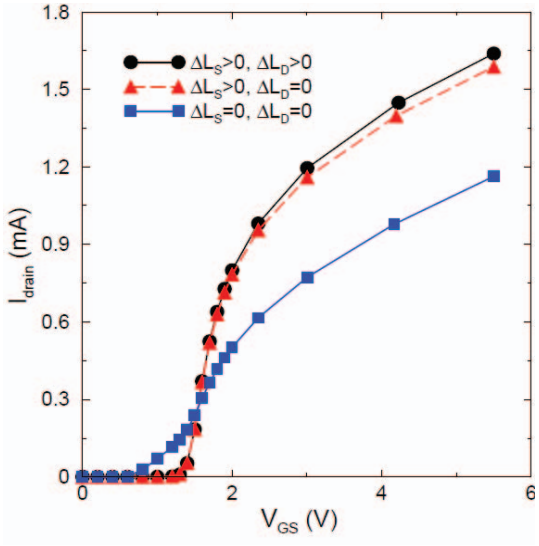

Figure 2. Turn-on characteristics for TFP-LDMOS devices with different trench layouts. When the lateral trench is crossing the channel region ($\Delta L_S = 0$) a drastic performance reduction is observed.

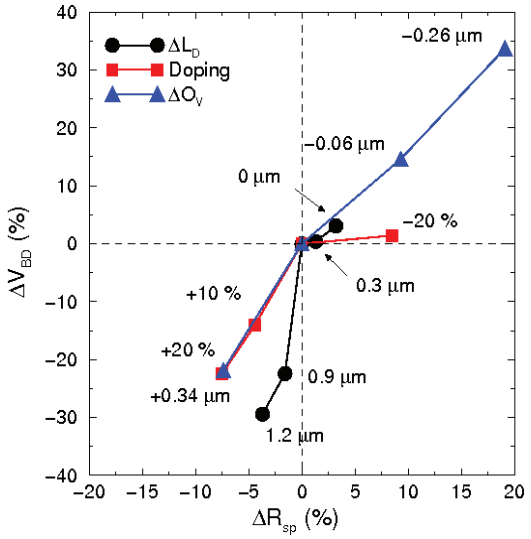

Figure 3. Relative R_{SP} and V_{BD} variations for the TFP-LDMOS with respect to the optimal device. The effects of doping, ΔL_D and ΔO_V variations are addressed. ΔL_D and ΔO_V are defined in Fig. 1.

silicon finger to the center of the polysilicon trench. When performing electro-thermal simulations, the use of a minimum pitch deck in the longitudinal direction allows for a worst case estimate of the self-heating effects, while the unit cell domain in the lateral direction corresponds to the simulation of a single central finger in a wide array. The definition of the analytical doping profiles has been derived from SIMS measurements and process simulations on a reference STI-based LDMOS device [7]. A fine tuning of the deck was then carried out through the comparison with experimental turn-on and output *I-V* curves.

A preliminary analysis of the turn-on characteristics is reported in Fig. 2, where, the results for different device realizations are compared. They represent three limit cases for the layout of the lateral trench: i) with the trench extending through the entire device ($\Delta L_S = 0$ and $\Delta L_D = 0$), ii) with the trench crossing only the drain region ($\Delta L_S > 0$ and $\Delta L_D = 0$), iii) or with an additional spacing between the trench end and the drain contact region ($\Delta L_S > 0$ and $\Delta L_D > 0$). Very similar results are obtained for the devices with $\Delta L_S > 0$, with a slight variation of the linear current at large gate voltages (V_{GS}), induced by the different contribution of the drain-side resistive component, which is modulated by the spacing ΔL_D. On the other side, when the trench crosses the channel region ($\Delta L_S = 0$), an unacceptable performance degradation is experienced with both a threshold-voltage shift and a maximum transconductance reduction, due to the creation of non conformal lateral and vertical channels [3]. For this reason, only the case of devices with $\Delta L_S > 0$ has been considered in order to have satisfactory channel properties, still comparable with those of the starting LDMOS device.

III. Device Optimization

The optimal device layout has been defined fixing a target $V_{BD} = 40$ V and looking for R_{SP} minimization. In addition, technological issues related mainly with the minimum achievable W_{OX} and W_{SI} have been accounted for in the optimization. In Fig. 3, the analysis of the dependence on N_D, ΔL_D, and ΔO_V for a fixed value of W_{OX} and of the W_{SI}/W_{OX} ratio, is reported, showing the relative variation of both R_{SP} and V_{BD} obtained by independently changing the different parameters. ΔR_{SP} and ΔV_{BD} values are expressed with respect to the ones of the optimal TFP-LDMOS. The largest sensitivity has been found when varying the overlap between the polysilicon gate and the trench field plate, leading, in particular, to a detrimental reduction of V_{BD} when the gate edge is pushed too far over the trench, drastically reducing the effective length of the drift region. In a similar way, even though the variation of N_D leads to the expected trade-off between R_{SP} and V_{BD}, an excessive reduction of the doping value gives a drastic reduction of the specific on-resistance without beneficial effects on the breakdown voltage. A less trivial dependence is found on ΔL_D variations. The use of a lateral trench extending trough the drain contact ($\Delta L_D = 0$) shows, in this case, a performance very close to the optimal case. On the other side, depending on the thickness of the oxide trench, this choice becomes a limitation to the maximum V_{BD} when larger drain voltages are considered. This is due to the increase of the critical electric field peak at the drain-contact interface with the oxide trench, which fixes a maximum V_{BD}. The use of a spacing at the drain end removes this constraint and allows for the use of small W_{OX} also at larger V_{DS} (≥ 40 V), as for example reported in Fig. 4. Here, the dependencies on W_{OX} and W_{SI}/W_{OX} have been considered. An optimal value of the finger-widths ratio, $W_{SI}/W_{OX} = 2$, has been found. In this case, a complete depletion of the silicon finger can be obtained through the lateral capacitive effect even with high N_D values. On the other side, a clear performance enhancement can be achieved only considering the scaling of both the silicon and oxide trench widths, with a two-fold beneficial effect: (i) a strong reduction of the pitch in the width direction and hence of the R_{SP}, (ii) an optimal electric field distribution along the finger, as reported in the inset of Fig. 4, where the device with the thinner oxide shows,

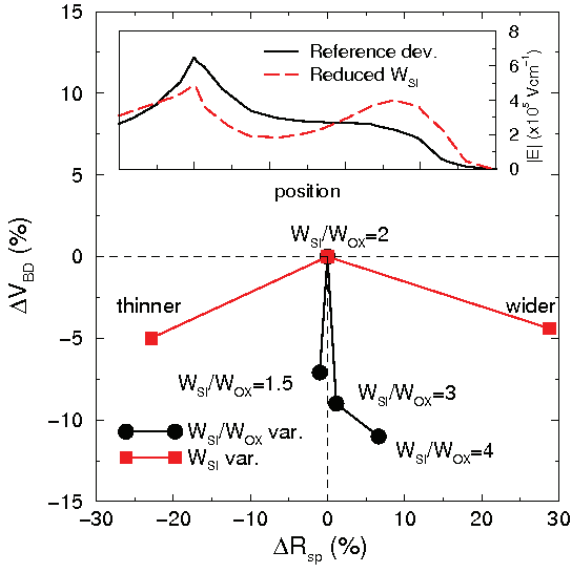

Figure 4. (Top) Relative R_{SP} and V_{BD} variations with respect to the optimal device. The effects of W_{SI} and W_{OX} are addressed. $W_{SI}/W_{OX} = 2$ turns out to be the optimum ratio. A further R_{SP} reduction for a small V_{BD} decrease could be obtained by scaling down W_{SI}, reaching an optimal distribution of the electric field along the drift region (inset).

at the breakdown condition, two equally distributed field peaks at the end of the gate and at the drain contact. This optimal distribution ensures a small variation of V_{BD} even with a large R_{SP} reduction.

IV. Characterization of the Safe Operating Area

A numerical analysis of the electrical, thermal and HCS properties has been performed for the optimized TFP-LDMOS. The TLP characterization for different pulse lengths has been carried out to obtain the failure condition induced by electrical (short pulses, no SHE) and thermal (long pulses and strong self-heating) stress. Simulation results are compared with those obtained for the standard STI-based LDMOS in order to highlight the issues connected to the use of a deep oxide trench structure. HCS degradation has been mainly investigated by monitoring the key quantities causing the interface trap formation at each stress bias and the interface-trap impact in the linear regime operating condition.

A. *Electrical properties*

In Fig. 5, the *I-V* output characteristics simulated in DC condition without the inclusion of the thermal effects are reported up to large drain and gate voltages, in order to investigate the electrical SOA of the device. First, we note that even at large V_{DS}, no electrical failure due to the snap-back effect is reported. This feature is achieved through the use of a heavily doped buried p-body, derived from the doping profiles of the STI-based LDMOS, that prevents from the onset of the parasitic NPN bipolar transistor [5]. Second, at large gate voltages, the key features of the rugged LDMOS are found, with the typical quasi-saturation effect at low V_{DS} and the successive current expansion effect ($V_{GS} = 6$ V, $V_{DS} > 25$ V) due to the enhancement of the electric field peak at the drain

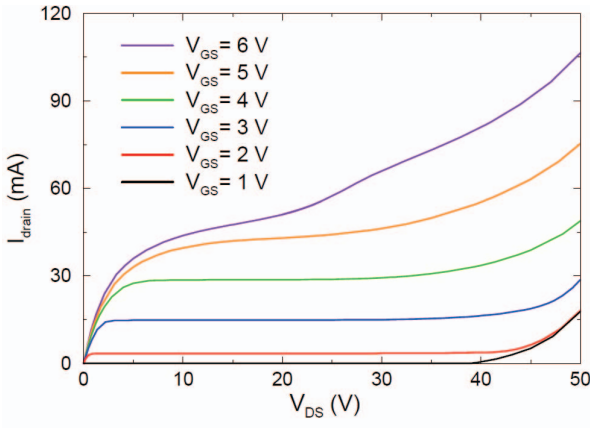

Figure 5. (Top) Simulated *I-V* charateristics for the optimal TFP-LDMOS up to the electrical failure, without the inclusion of thermal effects. No electrically activeted snap-back is obsvered due to the use of a heavely doped buried body. At large V_{DS} and V_{GS} the current "enhancement" effect is observed.

n/n+ junction and the consequent impact-ionization current generation.

B. *Hot-carrier stress reliability*

Hot-carrier stress induced degradation has been analyzed monitoring the local distribution in DC condition of critical quantities, namely, the electron temperature (T_n) and electron density (n) at the stress bias, and the total current density (J_n) at the maximum linear current bias, with the aim of giving a preliminary insight on the reliability concerns for the TFP-LDMOS. As representative of a typical worst case condition, only one stress bias configuration has been considered, with $V_{GS} = 2$ V and $V_{DS} = 39$ V. At such bias the standard STI-based LDMOS reports a large linear current degradation, induced by the trap formation at the source-side STI-corner [8, 9]. Even though the STI is removed, a large and critical electric field spot is expected at the polysilicon gate end. In Fig. 6, top, the 3D T_n distribution is reported at the stress bias investigated, showing critical "hot spots" at both the top and lateral oxide interfaces. In addition, in Fig. 6, bottom, the 1D cross-sections of T_n and n at the top oxide interface along the cutlines A and B defined in the 3D view are reported and compared with the current distribution along the same cutlines in turn-on condition. Critically high and uniform values are observed for both quantities along the entire drift region. In this condition, a high interface trap density can be expected, with a subsequent large effect on the device performance. In particular, this can induce a strong linear current degradation, as confirmed by the current density in turn-on condition, which is high and uniformly distributed along the finger interface.

C. *Thermal properties*

Finally, electro-thermal simulations have been performed to evaluate the impact of self-heating effects on the device SOA. TLP characteristics have been simulated considering the single-pulse response for different pulse durations (τ_P) varying from 100 ns to 1 ms. A comparison between the TFP-LDMOS and the conventional STI-based LDMOS has been set so to have a comparison between structures with and without deep oxide trenches. Equivalent thermal boundary conditions are

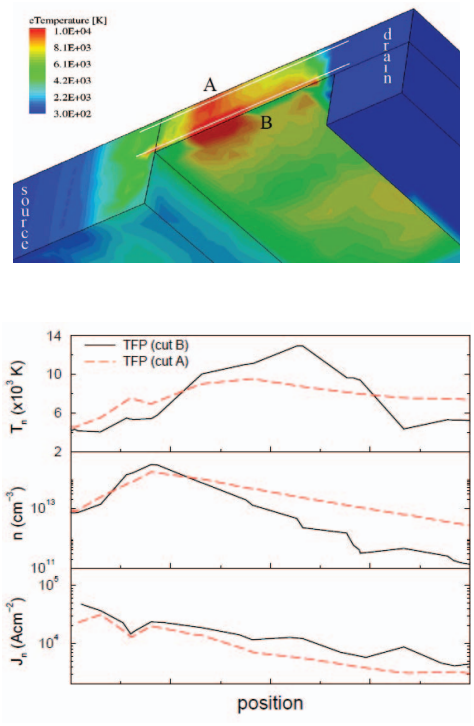

Figure 6. (Top) 3D electron temperature distribution for the TFP-LDMOS at a worst-case stress bias (V_{GS} = 2 V, V_{DS} = 39 V). High-temperature spots are distributed along the drift region nearby the oxide interfaces. Oxide and polysilicon regions have been removed in the plot. A and B: 1D cutline directions at the center and trench-side of the silicon finger, respectively. (Bottom) Electron temperature, electron density at the stress bias, and total current density at the maximum linear current bias condition (V_{GS} = 5.5 V, V_{DS} = 0.1 V), along the silicon/oxide interface for sections A and B.

considered for both devices in order to give a worst case estimate. The maximum internal temperature variations are defined as $\Delta T = T_{max}-T_o$, where T_o = 300 K is the external ambient temperature and T_{max} is local hottest spot within the device. ΔT values are reported in Fig. 7 as a function of the total power ($P = I_D \times V_{DS}$) for different pulse lengths (τ_P = 100 ns, 10 µs, and 100 µs). Since both devices reach a stationary condition for $\tau_P >$ 100 µs, the curves obtained for longer pulses are not reported. Two different gate voltages, V_{GS} = 2 and 4 V, have been considered, corresponding to strongly different current levels and different operating regimes of the intrinsic MOSFET. Clearly, a faster increase of ΔT is observed for the TFP-LDMOS. This is due to the effect of the lateral thermal isolation induced by the deep oxide trenches. Even though similar asymptotic behaviors are reached (similar thermal resistance), in accordance also with the use of identical thermal boundary conditions, the faster thermal response leads the TFP-LDMOS to a lower power to failure, in particular for the short pulse lengths. The trend observed for the thermal impedances is in accordance with previous studies on the impact of the use of deep isolation trenches or multiple oxide fingers [10]. On the other side, a larger maximum V_{DS} is reached by the TFP-LDMOS before the thermal failure caused by thermal runaway (not shown). This is due to the higher doping concentration for the lateral trench architecture along

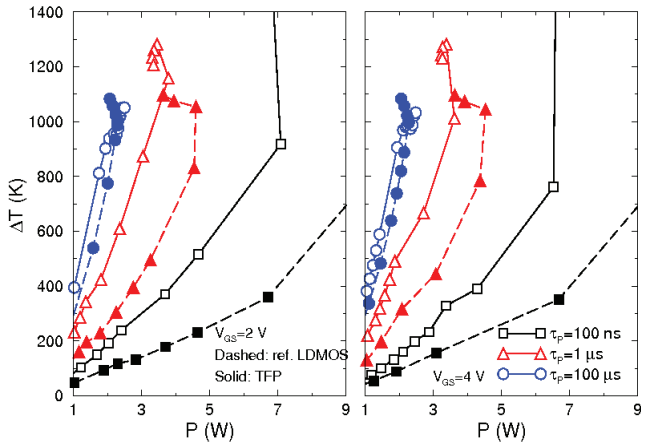

Figure 7. Comparison of the maximum temperature variations vs. power for different single-pulse lengths. A faster increase of ΔT is observed for the TPF-LDMOS, while, really close asymptotic behaviors (thermal resistances) are reported. The TFP-LDMOS reaches the thermal runaway failure at higher temperatures due to the higher doping value in the drift region.

the drift region, where the critical temperature spots are found, allowing the device to sustain larger temperatures when compared to the LDMOS.

V. CONCLUSIONS

A thorough investigation has been carried out on trench field plate LDMOS to the purpose of gaining an insight on the total SOA. After a proper optimization of the device, capable of achieving promising R_{SP} vs. V_{BD} values, an investigation of the electrical, thermal, and HCS degradation performance has been carried out. While SHE analysis showed a faster rising of the internal temperature for short pulse lengths, HCS reliability needs further investigations on the role played by the deep oxide-trench interfaces.

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