Microscopic Simulation of Electron Transport and Self-Heating Effects in InAs Nanowire MISFETs

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***Abstract*— We use a newly developed three-dimensional electrothermal Monte Carlo simulator, using finite-element meshing, to study metal-insulator field-effect transistors (MISFETs) based on a single InAs Nanowire. The model involves the coupling of an ensemble Monte Carlo simulation with the solution of the heat diffusion equation, and is carefully calibrated with data from experimental work on these devices. The simulator is applied to investigate electron transport and demonstrate the importance of self-heating in such devices characterized by high current densities.**

I. Introduction

Maintaining the current device miniaturization trend faces several technological roadblocks and fundamental challenges. It is widely accepted that future improvements in device performance should be expected from profound change in geometry rather than reduction in device dimensions. While advances in nanolithography allowed the design of complex-geometry nanostructures such as FinFETs [1] and ballistic switches [2], recent developments in "bottom-up" fabrication techniques led to the realization of a wide variety of nanowire structures [3]. In this context, the development of reliable three-dimensional (3D) simulation models is essential to help designing structures with an optimum performance, and provide insight into their physical behavior which is still not fully understood [2], [4]–[6].

We report results from the study of omega-shaped gate MISFETs [7] based on a 50nm-diameter InAs nanowire, using a suitably calibrated three-dimensional (3D) electrothermal Monte Carlo (MC) simulator. InAs nanowire MISFETs are of great interest, since they exhibit superior transport data compared to InAs channel heterostructure FETs. Properties of interest include excellent saturation behavior, and high breakdown voltage, current density and transconductance [7]. While this work aims for a better understanding of transport at the microscopic scale, it also has the purpose of demonstrating the importance of self-heating effects in these devices; the high current density in the nanowire may be accompanied by high power densities in regions characterized by high electric fields, giving rise to considerable temperature increase in the device, inversely influencing transport and device long term reliability and lifetime. Furthermore, the low thermal conductivities of InAs nanowires [8] and silicon nitride (SiN_x) [9] are physical factors that may also negatively affect thermal management in these devices.

II. Simulation Method

The simulator self-consistently couples 3D electron dynamics with a solution of the 3D time-independent heat diffusion equation, using an iterative procedure. At the end of a Monte Carlo simulation (iteration), the power density distribution is determined from counting the net phonon emission in the active region of the device. The thermal power distribution is then fed into a heat diffusion equation solver to determine the temperature distribution in the device. The obtained temperature distribution is then used in the subsequent Monte Carlo simulation as the device lattice condition, and the process is repeated until electrothermal convergence is reached. The number of Monte Carlo iterations necessary to achieve thermal self-consistency does not generally exceed five. The general concept of electrothermal Monte Carlo coupling is thoroughly explained in [10].

Both Poisson's and the heat diffusion equations are solved using a finite-element package (NETGEN/NGSOLVE [11]) integrated into our simulator, providing efficient device meshing and a reliable solution of these equations in complex geometry structures, such as the studied nanowire devices. The electrothermal Monte Carlo method has been applied successfully to conventional FET structures based on several material systems including silicon [12], [13], III-As [10] and III-N [14], [15] compounds. In these simpler geometries, employing solvers based on compact models or finite-difference meshing is sufficient for a reliable analysis of the carrier transport and heat transfer phenomena. While nanowires are considered as one-dimensional structures, three-dimensional finite-element based simulations, correctly accounting for the real device geometry, including the form of the metallic contacts as well the nanowire diameter, gate-oxide thickness and the buffer and

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substrate layers, are necessary for an accurate analysis of the performance of these devices.

Since this work focuses on the study of the electrothermal effects, a spherical non-parabolic model is used to describe the bandstructure of InAs. The simulation model considers all the important scattering processes, including intravalley acoustic and optical phonon scattering, intervalley phonon scattering, ionized impurity scattering, and electron-electron interactions. The hot-phonon effect [16], a phenomenon directly associated with electrothermal effects, is not expected to influence significantly the device thermal behavior, and therefore is not considered here. Instead, equilibrium phonon occupation numbers, calculated from the Bose-Einstein distribution, are used in the phonon scattering rate formulas.

While the studied (experimental-based) devices are characterized by relatively large length and nanowire diameter, the presence of quantization effects, due to electron confinement in the nanowire, may influence electron transport. These effects may play an important role in determining the electron distribution in the (two-dimensional $y-z$) plane perpendicular to the direction of transport (x-direction). Nonetheless, such effects are not expected to affect significantly the quantitative and qualitative conclusions made in this work concerning electrothermal effects, and therefore are not included in the simulations. Such effects can be readily included in our simulator, by applying quantum corrections involving the coupling of the solution of Poisson's equation with the solution of Schrödinger equation, which allows the calculation of the wavefunctions along this plane and the discrete electron energy levels in the nanowire [17]. However, this is verified to increase considerably the computational demand: the inclusion of quantum corrections, involving the solution of Schrödinger equation tens of thousands of times in one Monte Carlo simulation, results in lengthy simulations, especially when studying nanowire-based FETs incorporating gate contacts which are few microns in length.

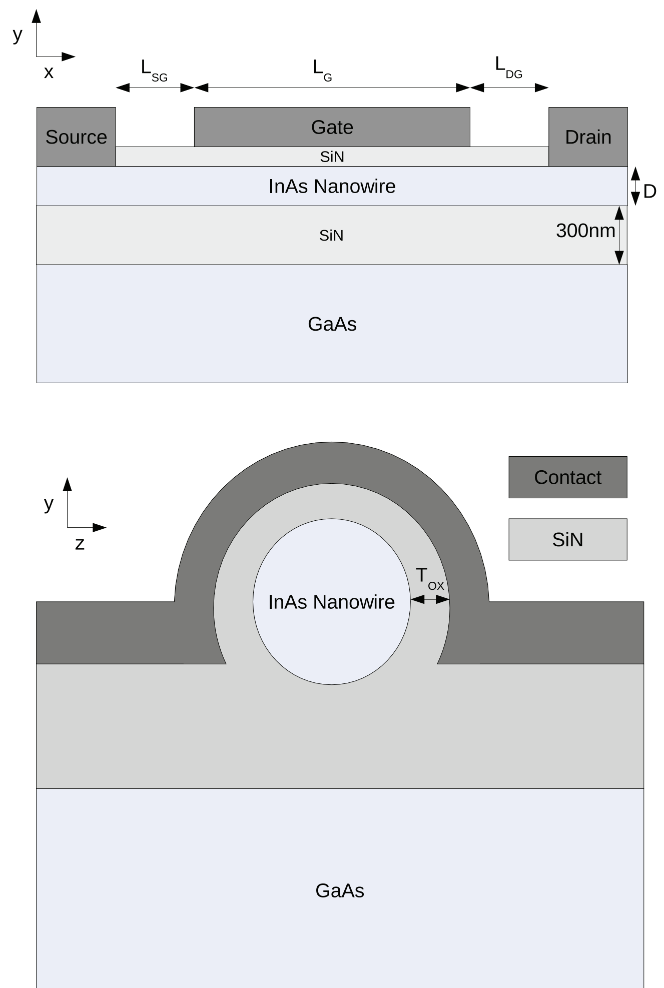


Fig. 1. The simulated three-dimensional geometry of the InAs nanowire MISFET: (top figure) cross-section along the x-direction (direction of transport), and (bottom figure) cross-section along the z-direction. In this example, the nanowire diameter (D), the gate length (L_G) and the gate-oxide thickness (T_{OX}) are set to 50nm, 1μm and 30nm, respectively. The source-gate (L_{SG}) and the drain-gate (L_{DG}) separations are both set to 0.5μm.

III. Simulated Structure

Below, we present results from the simulation of the omega-shaped gate InAs nanowire MISFET studied in [7]. The device is characterized by a nanowire diameter (D) of 50nm, a gate length (L_G) of 1μm and a gate-oxide thickness (T_{OX}) of 30nm. The separations between the source and gate contacts (L_{SG}) and the drain and gate contacts (L_{DG}) are both taken to be 0.5μm. Fig. 1 shows the 3D geometry used in the simulations. The nanowire and the contacts lie on top of a 300nm SiN_x layer. The structure is assumed to be built on a single GaAs die including a fixed-temperature heat-sink (300K) placed at its base (as explained in our previous work [10]). For the solution of the heat-diffusion equation, adiabatic thermal boundary conditions are applied at the other die surfaces, allowing heat to be evacuated only through the base surface of the die. The die length, width and depth are all set to 100μm. The simulator includes carefully the temperature-dependent thermal conductivity properties of the GaAs substrate, the InAs nanowire, the SiN_x layers, and the Ti/Au metallic contacts incorporated in the device. A positive surface charge of approximately 10^{12}cm^{-2} is included at the nanowire surface, which is similar to the reported experimental values [18]. It is noteworthy that the choice of simulating experimental structures (with gate lengths ranging from one micron to few microns) is motivated by the need to validate our simulator and establish its reliability. This is to provide a reliable investigation of electron transport and a realistic prediction of the impact of self-heating in existing nanowire MISFET structures.

IV. Results, Analysis and Discussions

Fig. 2 shows the measured and the simulated I_d-V_{ds} and I_d-V_{gs} characteristics of the 2μm gate length MISFET studied in [7]. This figure illustrates the excellent agreement between the experimental data presented in [7] and the results we obtained from the simulation of this device. The relatively small deviations are believed to be due mainly to the slight

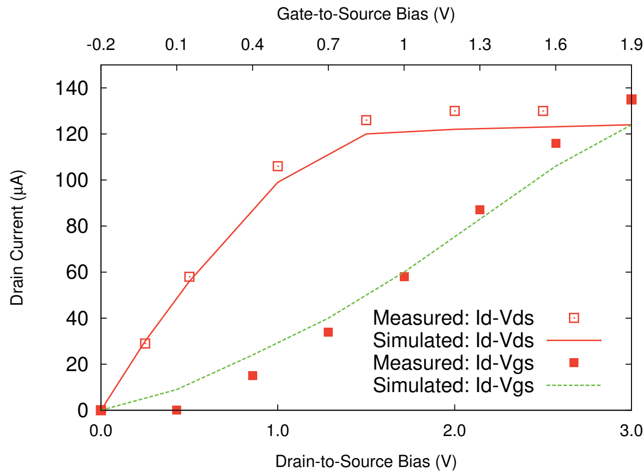


Fig. 2. The measured and simulated I_d-V_{ds} characteristics of the 2μm gate length MISFET studied in [7] at $V_{gs} = 1.9$V, and the measured and simulated I_d-V_{gs} characteristics of this MISFET at $V_{ds} = 3.0$V.

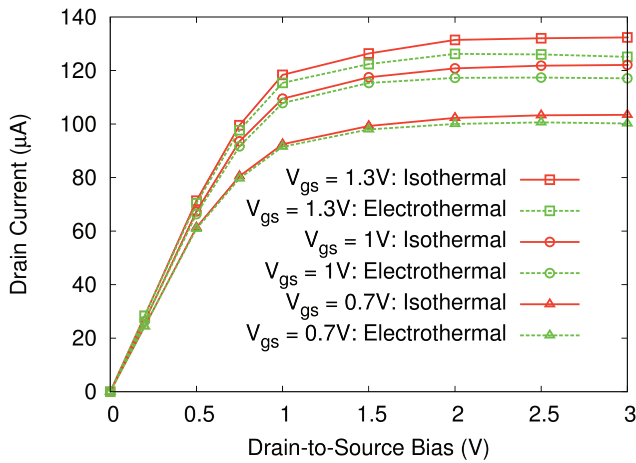
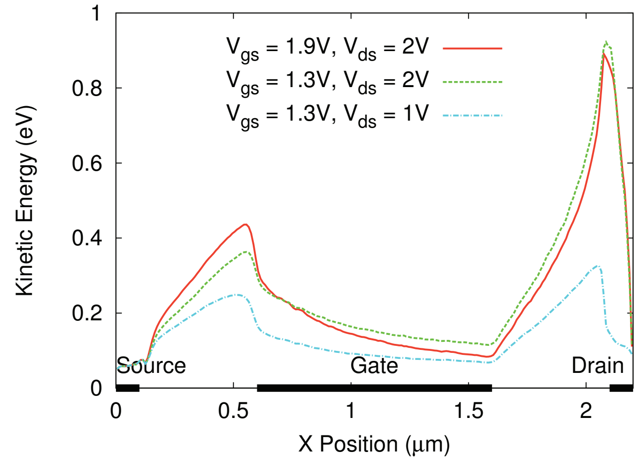


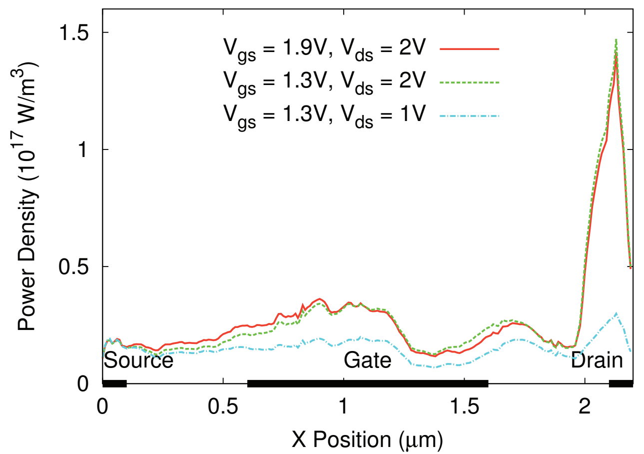
Fig. 3. The isothermal and electrothermal I_d-V_{ds} characteristics of the 1μm-gate MISFET studied here, for different gate biases (0.7V, 1V and 1.3V).

difference between the simulated and real device geometries. Fig. 3 shows the isothermal and electrothermal I_d-V_{ds} characteristics of the 1μm gate length device described in Fig. 1. Fig. 3 demonstrates self-heating effects at the macroscopic level, by showing the drain current reduction upon the inclusion of electrothermal self-consistency. Such reduction increases with the increasing gate and drain biases.

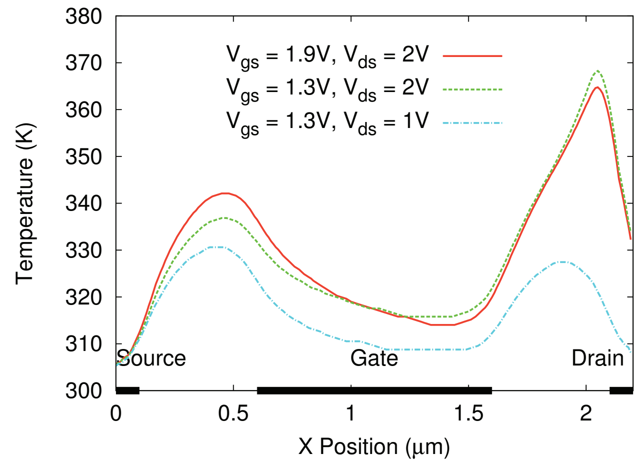
To demonstrate the electrothermal effects at the microscopic scale, we show in Fig. 4 some microscopic results including the average electron energy, power density and lattice temperature along the nanowire for various biases. Fig. 4 demonstrates heat-generation in the nanowire, which is most important near the gate-end of the drain, where strong non-equilibrium transport takes place. This is illustrated in the energy profiles where a population of hot-electrons is visible in this region. Heat generation is also visible under the gate, especially near the source-end of this terminal, where a population of relatively high-energy electrons is observed. As expected from the power density profiles, the temperature distribution profiles



(a)



(b)



(c)

Fig. 4. Variation of (top figure) the mean electron kinetic energy, (middle figure) the average power density, and (bottom figure) the lattice temperature along the nanowire, for electrothermal conditions, at different gate and drain biases.

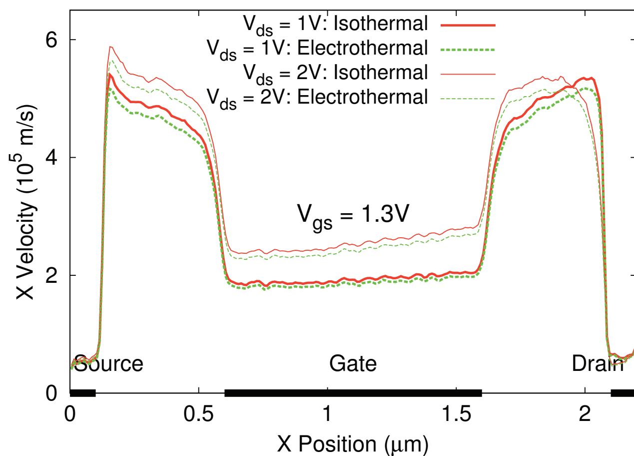


Fig. 5. Variation of the mean electron velocity in the x direction along the nanowire, for isothermal and electrothermal conditions, at $V_{gs} = 1.3$V for two different drain biases (1V and 2V).

illustrate how the peak temperature occurs near the gate-end of the drain, where most of the heat is generated. A secondary peak is visible in the source-end of the gate, in spite of the reduced heat generation in this region. This is because heat evacuation is more challenging in this region (where a very low thermal conductivity material (SiN_x) surrounds the nanowire), as compared to the drain region (where the drain metallic contact does not seriously impede heat diffusion). At biasing conditions where the influence of gate voltage is more important than that of the drain voltage, the location of the peak temperature shifts to the source-end of the gate, as illustrated in Fig. 4 at gate and drain biases of 1.3V and 1V, respectively.

Fig. 5 also shows microscopic results including the variation of the isothermal and electrothermal mean electron velocity in the x direction along the nanowire, for different biases. The expected reduction in the electron x velocity due to self-heating is illustrated, which is observed to be generally more important at higher biases. This reduction is more important in regions where temperature rise is more significant, including the source and drain sides of the device. The visible reduction in both the isothermal and electrothermal velocity values near the gate-end of the drain, at higher drain biases, is mainly due to the increased number of intervalley phonon scattering events in this region, where high kinetic energy values encourage transitions to the upper satellite valleys.

V. Conclusion

This work is a microscopic study of electron transport and thermal effects in InAs nanowire MISFETs, using a well-established thermally self-consistent Monte Carlo simulator based on finite-element meshing. Although these devices are characterized by a low power dissipation, significant temperature rise is observed in the structures (more than 100°C), which inversely affects the performance and reliability of these nanodevices. This is a result of the high power density levels combined with the poor thermal management in these structures, which is attributed mainly to the low thermal conductivity of SiN_x and the InAs nanowire. This study is performed for InAs nanowire MISFETs, but the findings may be extended to similar field-effect nanostructures.

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