Optimal Design of III-V Heterostructure MOSFETs

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Background: III-V semiconductors are promising candidates for future high-speed, low-power MOSFETs. Most of the effort so far focused on passivation of the III-V/dielectric interface which still remains a major issue [1]. On the other hand III-V systems offer unique features such as nearly lattice matched type-I heterostructure, insitu doping etc. which can be intelligently used to mitigate some of these issues & improve the device performance. However, a detailed analysis is needed to optimize the design of the heterostructure based III-V MOSFETs for I_{ON}/I_{OFF}, sub-threshold swing (SS), band-to-band tunneling (BTBT), DIBL; specifications relevant for logic design.

Introduction: In this paper we study the design of the double gate (DG) heterostructure MOSFET (Fig. 1) using charge profiles and band structure calculated using 8 band k.p approach. Use of modulation doping to aid charge confinement in the channel material is explored. Electrostatics and BTBT leakage in the heterostructure design is compared using 2D TCAD simulations. Effect of interface states (D_{it}) on the heterostructure vs. surface channel device is compared. Performance enhancement in the optimal design is quantified.

Methodology: Looking at the band energies vs. lattice constant (Fig. 2) we choose to study 2 lattice matched type-I heterostructure systems (1) $In_{0.53}Ga_{0.47}As/InP$ which has excellent electron mobility in the Narrow Bandgap (NB) $In_{0.53}Ga_{0.47}As$ channel, and has been widely studied experimentally [1]. (2) The $GaSb/AlAs_{.08}Sb_{0.92}$ which has been shown to exhibit good hole mobility [2] and has good offsets between the NB and Wide Bandgap (WB) material. The electron/hole mobilities and the Conduction/Valence Band Offsets (CBO/VBO) between the NB/WB layers are summarized in Table.1. Device dimensions/voltages are taken from the IRTS 2009 specifications for the 2016 MG MOSFET. 8 band k.p Schrödinger [3] and Poisson equation are solved in a self-consistent manner along the cross section in Fig. 1. The k·p Schrödinger equation is discretized along the grid points using the approach of [4]. For a grid point at the interface of two different material layers, the differential operators are symmetrized similar to [5] to make the eigenproblem Hermitian. Dirichlet boundary condition is applied at the III-V/dielectric interface. Fig. 3 plots the bandstructure for InAs : bulk and for DG device with 5nm body width (T_{BODY}), which have been calibrated against results from empirical pseudopotential method [3]. Effect of confinement and thin body are accounted for in our approach.

Book keeping of the charge: A heterostructure design provides extra barrier from the offset between the NB/WB materials to confine the carriers away from the III-V/dielectric interface, in the center of NB channel which has lower E-field (Fig. 4). Fig. 5 plots the charge and conduction band profile for $InP/In_{0.53}Ga_{0.47}As$ NMOS vs. T_{CAP} for a fixed T_{BODY} =8nm and V_G=0.4V. Increasing the T_{CAP} causes spillover of the charge in the low mobility WB material (Fig. 6), hence a thin T_{CAP} sufficient to screen D_{it} and meet BTBT requirement (discussed later) is desired. Fig. 7 plots percentage of charge in the low mobility WB material as a function of total sheet charge for NMOS/PMOS based on the two systems for T_{CAP}/T_{BODY}=2/8nm. We observe that charge spillover is worst for $InP/In_{0.53}Ga_{0.47}As$ NMOS because of low CBO (Table. 1) and m_{DOS} for the electrons. Sb based system-2 (Table. 1/Fig. 2) offers sufficient barriers for both electrons and holes and appears optimum for heterostructure MOSFET design (Fig. 7).

Modulation Doping: Modulation doping which is readily available during III-V growth can be combined with work function engineering to produce a deeper quantum well for confining the charge in the high mobility NB material (Fig. 8(a)). Use of n-type modulation doping for confining electrons in $In_{0.53}Ga_{0.47}As$ channel (which has worst charge spill over) is demonstrated in Fig. 8(c).

***D_{it}* :** Interface states at the III-V/Dielectric interface cause degradation of SS and transport properties. Assuming a bell shaped D_{it} distribution which is typically associated with III-V semiconductors [6] (Fig. 9) we observe that introducing a thin WB channel material causes the Fermi level (E_F) movement required to turn the device ON to shift from a region of high D_{it} in the NB material to low D_{it} region in the WB material (Fig. 9). In our simulation an exponential distribution of D_{it} is assumed for the interface between dielectric and III-V material with D_{it} of $1\times10^{14}eV^{-1}cm^{-2}$ at the band-edges and mid-bandgap D_{it} of $3\times10^{10}eV^{-1}cm^{-2}$ for both the surface and buried channel devices. The interface between two III-V materials is assumed to be defect-free. Improvement in SS by the avoidance of high D_{it} is shown in Fig. 10. As T_{CAP} is further increased, SS degrades due to extra EOT added by the WB material.

SS/DIBL: One of main concerns with buried channel devices is degradation in electrostatic control due to the channel being further away from the gate dielectric interface. Meanwhile, high mobility materials with high permittivity in general result in worse short channel effects (SCE) [7]. Thus, the

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electrostatics is carefully studied by 2D TCAD simulation [8]. Fig. 11 plots SS and DIBL vs. L_G for different T_{CAP}. We observe that the electrostatic control of the heterostructure device is comparable to its surface channel counterpart, while the dominating factor of two-dimensional electrostatics is still the combined body thickness and L_G. For L_G=17nm there is only 5% (10%) variation in SS (DIBL) for varying T_{CAP}=1-3.5nm. This can be attributed to the excellent electrostatic control of the fully depleted DG MOSFET. The high permittivity of the cap layer results in only a small penalty on the gate control.

BTBT: Most high-mobility III-V materials have a smaller and direct bandgap, leading to high band-to-band tunneling which can limit the OFF state leakage current, I_{OFF} (Fig. 13). In OFF state (high drain voltage, low gate voltage) the maximum electric field occurs at the edge of the gate-drain region (Fig. 12). The heterostructure design moves the high electric field region into the WB material causing a decrease in the BTBT leakage. A non-local path band-to-band tunneling model is used for simulation [8]. For the direct-bandgap III-V materials, parameters are specified for direct tunneling calculation of band-to-band generation rate, which is an extension of Kane and Keldysh models and Franz two-band dispersion is adopted [8]. The effectiveness of reducing the BTBT by increasing T_{CAP} is shown in Fig. 13. With 2nm cap layer thickness, a reduction of three orders of magnitude can be achieved for OFF state leakage.

Performance improvement: I_{Dsat}-V_G's (for V_{DS}=V_{DD}) are plotted in Fig. 15 for varying T_{CAP}. Use of T_{CAP}=1nm confines the charge effectively in the high mobility NB channel, overcomes the effect of D_{it} and can result in over 100% (50%) I_{ON} improvement over the surface channel device in InGaAs/InP NMOS (GaSb/AlSb PMOS). Increasing T_{CAP} further causes spillover of the charge in WB material and the performance gain is lost (Fig. 14). The set of transport models used for simulation include hydrodynamic transport model, density gradient model for quantum mechanical quantization, Philips unified mobility model, enhanced Lombardi model with high-k degradation, high-field mobility degradation [8] and isotropic transport is assumed. D_{it} settings are the same as for subthreshold swing simulation.

Conclusion: Sb based materials offer large VBO/CBO suitable for heterostructure design. The small CBO for InGaAs/InP NMOS can be overcome by intelligent use of modulation doping. A heterostructure design with T_{CAP}=1nm can reduce the effect of D_{it} (Fig. 11), lead to an order of magnitude reduction in BTBT (Fig. 13) and a 100/50% improvement in the I_{Dsat} (Fig. 14) while maintaining good electrostatic control in terms of subthreshold swing and DIBL (Fig. 11).

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Reference

[1] Y. Xuan et. al, Proceedings of IEDM 2008, pp. 371.
[2] A. Nainani et. al, Proceedings of IEDM 2009, pp. 857
[3] A. Nainani et. al., Proceedings of SISPAD 2009, pp. 47.
[4] Y. X. Liu, Physical Review B, v. 54, pp. 5675.
[5] TU-München, nextnano manual
[6] P. D. Ye et. al. , Journal of Vacuum Science & Technology, v. 26, p. 697.
[7] T. Krishnamohan et. al., Transcations on Electron Devices, v. 53, p. 1000.
[8] Sentaurus Device, User Guide, March, 2010.

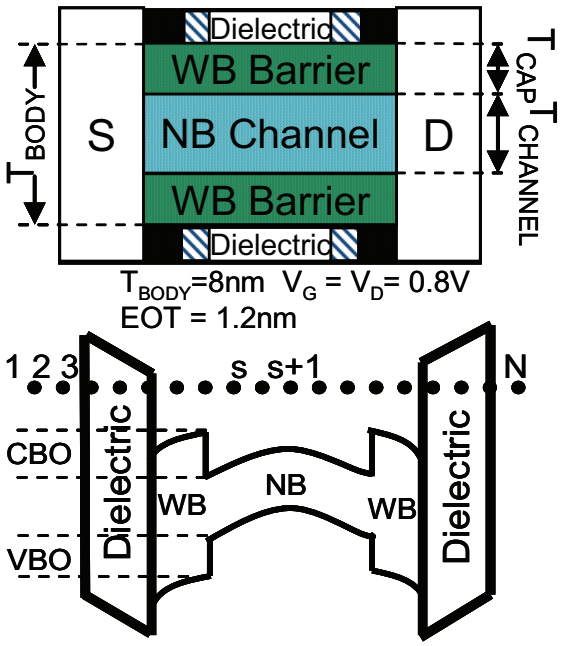


Fig.1 DG heterostrcuture MOSFET (top). Cross section of the device used for bandstructure calculations (bottom).

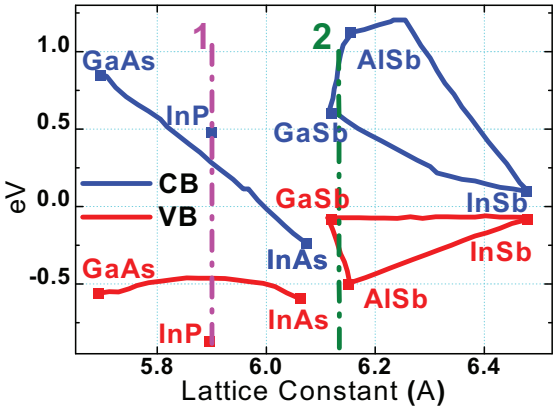


Fig.2: Two lattice matched type-I heterostructure systems are studied for DG MOSFET (Table.1)

Table 1 : $In_{0.53}Ga_{0.47}As$ =InGaAs, $AlAs_{0.07}Sb_{0.93}$ = AlSb

System	1	1	2	2
	WB	NB	WB	NB
	InP	InGaAs	AlSb	GaSb
Eg (eV)	1.344	0.74	1.696	0.726
CBO (eV)		0.22		0.49
VBO (eV)		0.38		0.47
ε_o	12.5	13.9	12.04	15.7
Lattice Constant (A)	5.867	5.868	6.0959	6.099
μ_e (cm^2/Vs)	5400	12000	200	3000
μ_h (cm^2/Vs)	200	300	400	1000

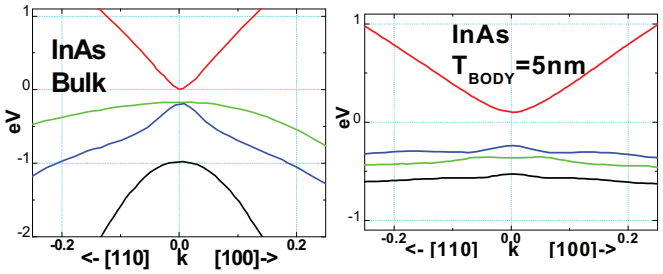


Fig.3: Bandstructure of InAs from 8 band k.p for bulk (left) & T_{BODY}=5nm (right) are calibrated against results from empirical pseudopotential method [3].

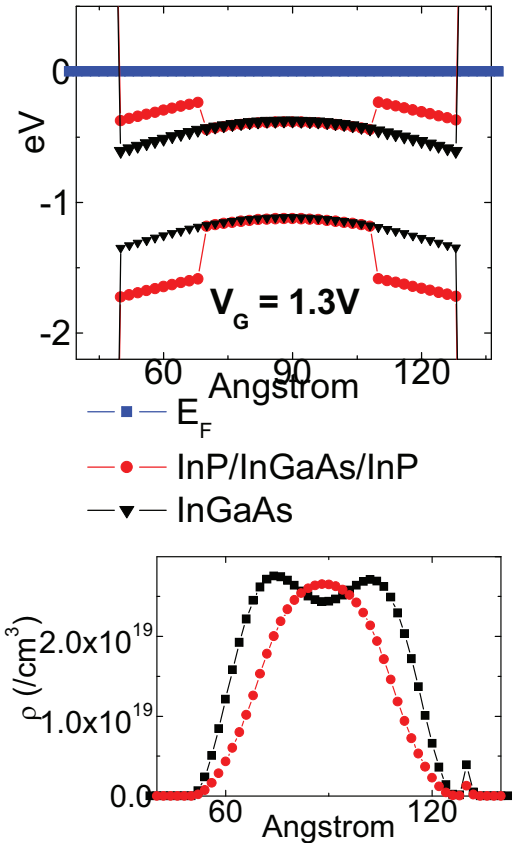


Fig.4: Potential from quantum well in the heterostructure design (top) helps in confining the charge in center of the NB material (bottom).

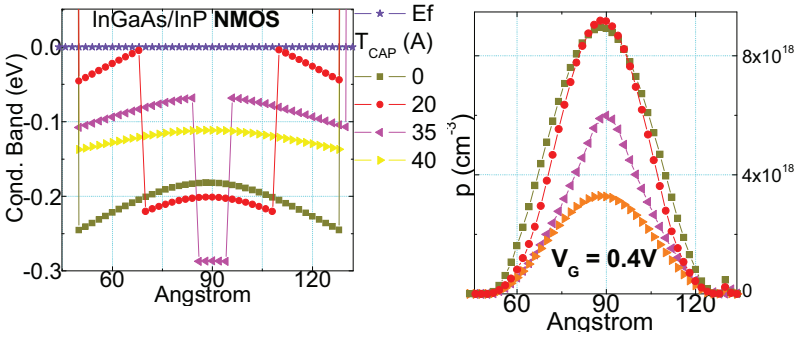


Fig.5: Conduction band energy (left) and charge profile (right) with varying T_{CAP}.

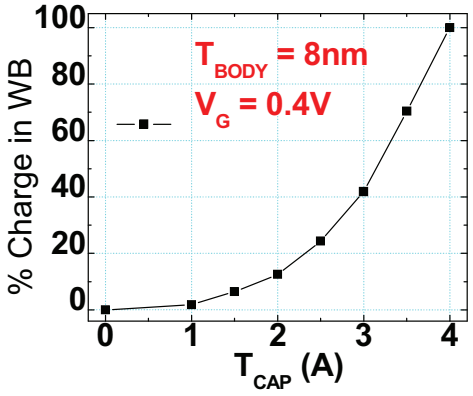


Fig.6: Charge in low mobility WB material as function of T_{CAP}.

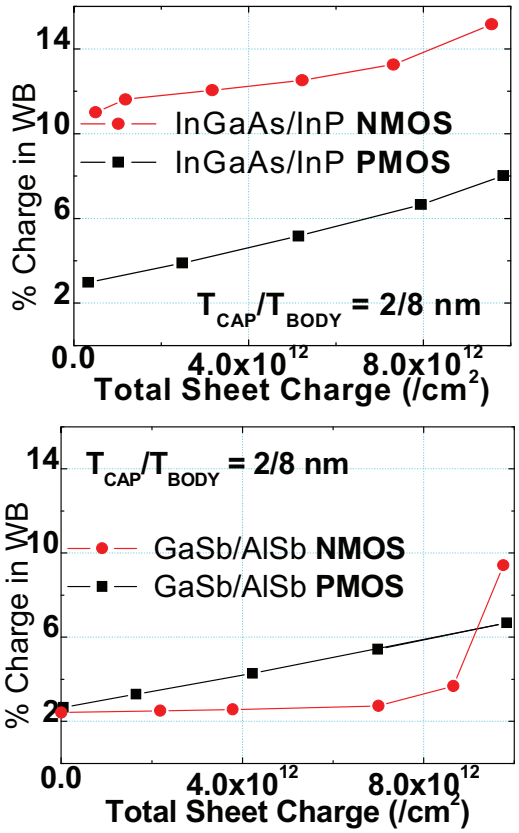


Fig.7: Percentage of charge in WB material with increasing sheet charge for InGaAs/InP (top) & GaSb/AlSb (bottom) systems

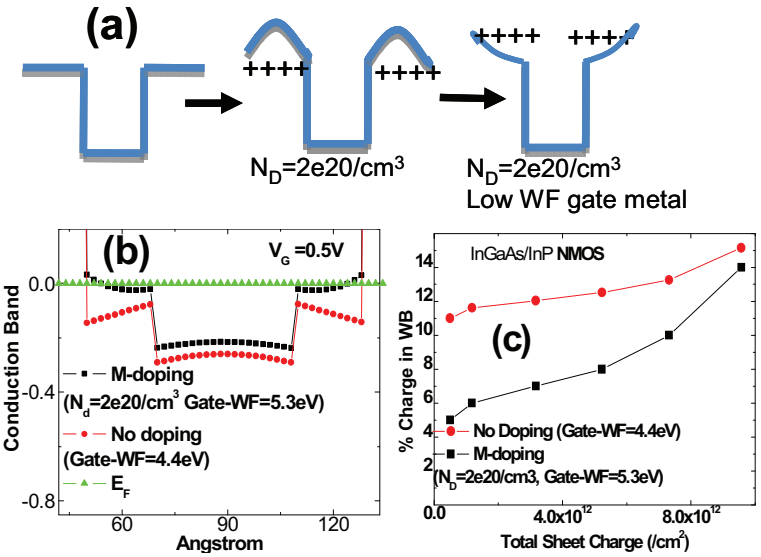
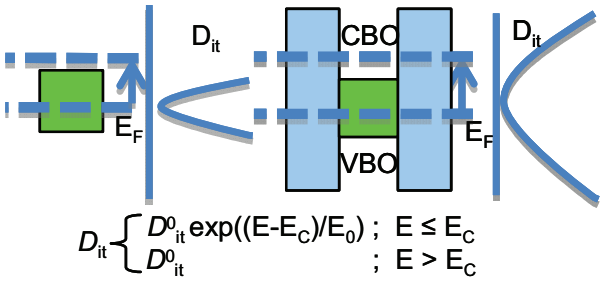


Fig.8: (a) Use of modulation doping to confine charge in the NB channel (b) conduction band profile at V_G=0.5V & (c) Reduction in charge in WB material using modulation doping.



$$D_{it}\begin{cases} D^0_{it}\exp((E-E_C)/E_0) ; & E \le E_C \\ D^0_{it} ; & E > E_C \end{cases}$$

Fig.9: E_F movement for the applied gate voltage & the corresponding D_{it} region scanned for surface channel (left) vs. heterostructure (right) design.

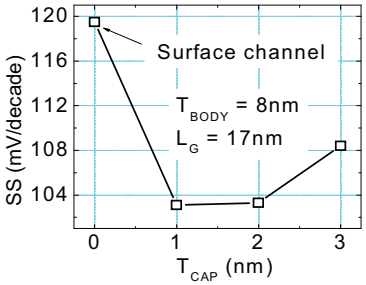


Fig. 10: SS vs. T_{CAP} taking into account the effect of D_{it} (Fig. 9).

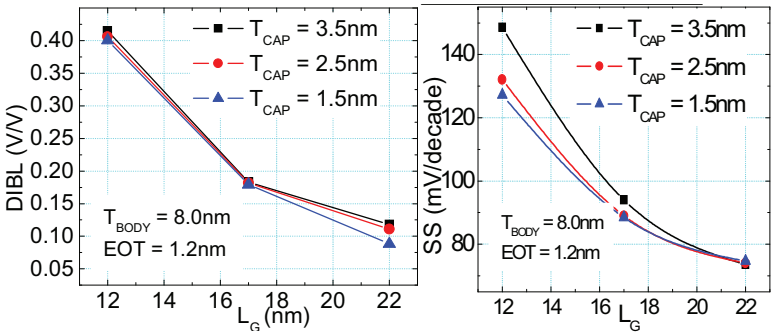


Fig.11: Short Channel Effects: DIBL (left) & SS (right) vs. L_G are compared for different T_{CAP}.

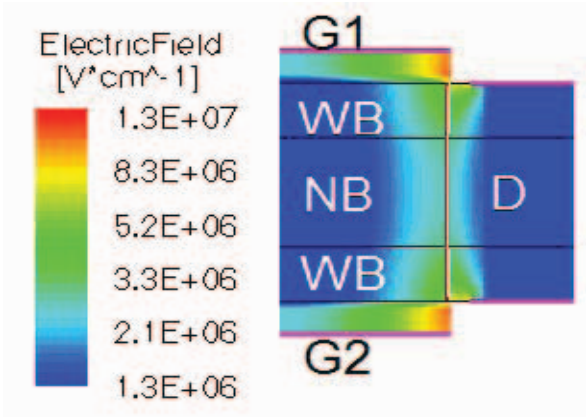


Fig. 12: E-field profile for VG = 0, V_D = 0.75V Use of heterostructure design moves the E_{max} region in the WB material.

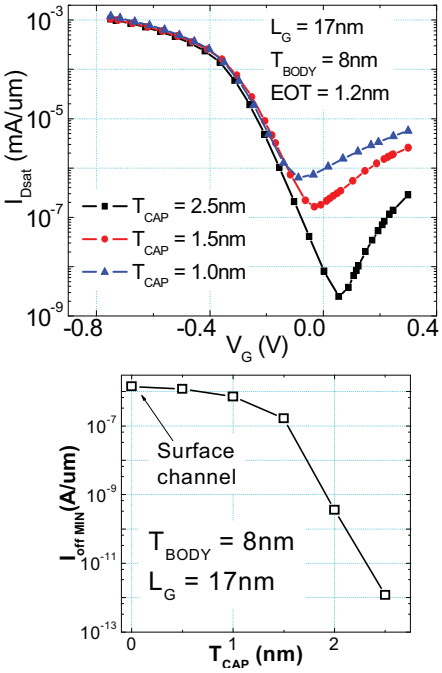


Fig.13: The off current is limited by the BTBT (top); Suppression of BTBT with increase in T_{CAP} (below).

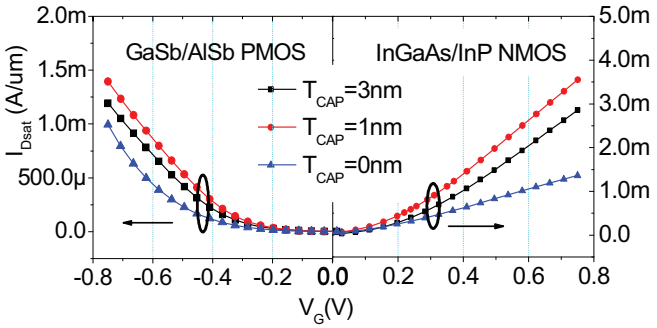


Fig.14: Saturation current for different values of T_{CAP} for PMOS (left) and NMOS (right).