Schrödinger-Poisson and Monte Carlo analysis of III-V MOSFETs for high frequency and low consumption applications

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***Abstract*—III-V MOSFET (Metal Oxide Semiconductor Field Effect Transistor) with high-κ gate dielectric stack appears as a viable alternative to enhance not only microwave performance but also logic circuits with low supply voltage. This allows fulfilling high-speed and low-power specifications for intelligent applications. Indeed, combining weak gate leakage of standard MOSFETs and good RF performance of HEMTs (High Electron Mobility Transistors), they could outperform end-of-roadmap standard Si-MOSFET. Using full 2D Poisson-Schrödinger solver and a semi-classical Ensemble Monte Carlo device simulator, various 50nm MOSFET and HEMT are investigated in terms of gate charge control and both static and dynamic I-V performance. In particular, Y parameters are carefully extracted from time-varying currents. This comparative study allows us to propose an optimized III-V nano-FET architecture with high-frequency performance under low power supply.**

I. INTRODUCTION

The future high-speed and autonomous specifications for ambient intelligent functions require very low supply voltage [1]. Next generations of Si-CMOS circuits should not meet this kind of specification [2]. Indeed, their optimal frequency-performance/power-consumption trade-off is limited by poor Si carrier mobility and relatively large supply voltage required for circuit operation [3]. Moreover, conventional Si-CMOS scaling approaches the end of the roadmap. High-mobility III-V materials appear as a viable alternative to enhance DC/AC device performance [4]. Promising microwave but also logic potentialities have recently been demonstrated in InGaAs HEMTs [5]. But, due to high gate leakage current inducing high DC power consumption, they tend to reach their scaling limits in terms of gate length and layer structure. MOS topologies with high-κ dielectric gate stacks compatible with III-V channel [6] are expected to improve the electrostatic gate control and to drastically reduce the gate leakage [7-8]. Very promising microwave and noise performance for long-channel case (1 µm) was characterized by pioneering work [9]. Nevertheless, high mobility III-V MOSFET performance might be affected by rough channel/oxide interface, by their low Density Of States (DOS) and by band to band tunneling current leakage [10]. The originality of this work is to asses the potentiality of III-V MOSFETs operating at low supply voltage (200 mV) to overcome their intrinsic limitations.

Both electrostatic gate charge control via capacitance-voltage characteristics and static/dynamic I-V characteristics are investigated theoretically. Four InGaAs MOSFET and one HEMT architectures are compared using 1D-2D Poisson-Schrödinger simulations and a semi-classical Ensemble Monte Carlo simulator.

II. SIMULATED DEVICE

The first considered structure is a 50 nm-long-T-shaped gate HEMT whose layer structure and device parameters were described in Ref [11]. It consists of a 100 nm-thick $In_{0.52}Al_{0.48}As$ buffer layer on (001) InP substrate, a 7.5 nm $In_{0.53}Ga_{0.47}As$ sub-channel, a 7.5 nm $In_{0.8}Ga_{0.2}As$ main channel, a 3 nm undoped $In_{0.52}Al_{0.48}As$ spacer, a 3 nm planar Si-doped layer ($1\times10^{13}/cm^2$), a 10 nm $In_{0.52}Al_{0.48}As$ Schottky barrier layer and a 26 nm Si-doped $In_{0.53}Ga_{0.47}As$ cap layer. Other devices are 50 nm-long-MOSFET structures (cf. Fig. 1) with $In_{0.53}Ga_{0.47}As$ channel and self-aligned Al_2O_3/TaN gate stack. Since the performance of conventional bulk-MOSFET structures is known to be affected by scattering on rough dielectric interface and doping impurities, three other alternative structures are proposed in Fig. 1 to overcome these detrimental effects. The so called Thin Body TB-MOS structure is inspired by the Silicon On Insulator (SOI) technology. In the HEMT-MOS structure, a wide bandgap III-V spacer is inserted between the channel and the dielectric. The COMB-MOS transistor is a combination of the two previous ones.

III. CHARGE CONTROL- POISSON SCHRÖDINGER ANALYSIS

Thanks to a self-consistent Poisson-Schrödinger solver [11], the charge control in bulk MOS structures was investigated in

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terms of gate capacitance-voltage characteristics. The quantum, degeneracy and nonparabolicity effects were carefully considered [11].

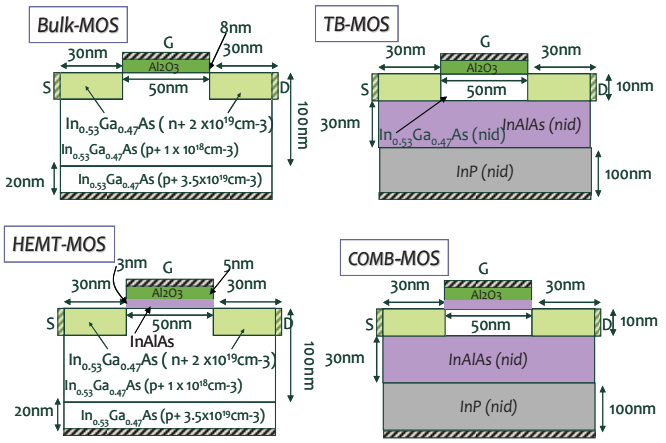

Figure 1 Cross section of the four MOSFET structures under investigation (nid: non intentionally doped).

We first examine the 1D-behavior of the long-channel gate capacitance C_G which results from a series connection of the inversion charge capacitance C_{INV} and the oxide capacitance C_{OX}. The surface confinement orientation is (001). In Fig. 2, we plot C_{INV} and C_G as a function of the gate voltage for an Al_2O_3 gate oxide thickness T_{OX} of 6 nm. The inset shows the electron distribution over Γ and L valleys as a function of gate voltage and total electron density. At low gate voltage, only the low-DOS Γ valley is occupied and the inversion charge capacitance C_{INV} is small. The limitation in overall gate capacitance C_G comes from this finite inversion-layer capacitance in this gate voltage range [12]. Thus, in contrast to Si-devices, C_G does not strongly increase when reducing T_{OX}, which yields specific scaling rules for III-V MOS [11].

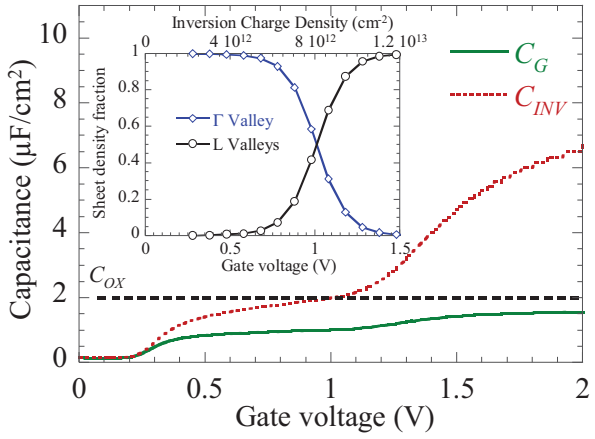

Figure 2 Capacitances C_G and C_{inv} as a function of V_G for a 1D Bulk MOS capacitance with T_{ox} = 6 nm. Inset: fraction of electron density in L and Γ valleys vs. V_G and electron density.

When increasing the gate voltage, the electron density in L valleys is enhanced, which leads to higher C_{INV} and C_G. The transfer into L valleys with much higher conduction mass is favorable to get an efficient charge control with a high C_G capacitance close to the limit value C_{OX} = 2 μF/cm^2, but it is detrimental to the carrier transport properties. Thus, a V_G swing from 200 mV to 700 mV is appropriate to provide a high enough density of 'fast' Γ electrons (cf. the inset of Fig. 2) to give good RF performance.

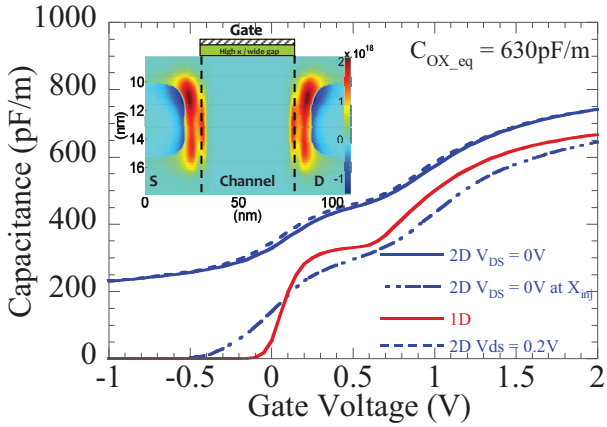

Figure 3 2D vs. 1D total gate capacitances C_G for the 50 nm COMB-MOS as a function of the gate voltage V_G. Inset: 2D cartography of the difference in electron density (cm^{-3}) between V_{GS} = -1 V and V_{GS} = -0.8 V at V_{DS} = 0 V.

The above 1D approach is questionable to evaluate the capacitances for deca-nanometer III-V FETs. Indeed III-V semiconductors have a higher permittivity than Si, which may enhance short-channel effects (SCE) and fringing effects. Hence, full 2D Poisson-Schrödinger analysis was used to refine the previous 1D estimations by capturing geometry effects. Fig. 3 shows C_G as a function of V_G for a COMB-MOS structure where the channel is undoped. In the subthreshold regime, a high value of C_G is obtained in 2D simulations due to fringing capacitance C_F (about 240 pF/m). This capacitive fringing effect at the off state is illustrated by the inset which shows the difference in electron density between 2 gate biases (V_{GS}=-1V and -0.8V). The variation of electron density at low V_G is indeed localized close to the fringe of source and drain regions. Besides, from 2D simulation the charge in a small slice at the top of the source-side injection barrier X_{inj} was calculated at V_{DS} = 0 V and compared to the 1D results. SCE induces a shift in the C-V curves at X_{inj} compared to 1D C_G. The modulation of the 2D space charge layer degrades the gate capacitance in strong inversion condition compared to 1D calculation. Furthermore, 2D simulations can take into account the influence of source/drain bias, i.e. the lateral field along the channel. Drain-induced barrier lowering (DIBL) induces a shift in the C-V curves toward negative values. At high gate voltage (V_G = 1.3V) for COMB-MOS, C_G exceeds the limit value C_{OX} (630 pF/m), due to the occurring of a parasitic channel in the wide gap spacer (with heavy conduction mass). Unfortunately, as the L valley transfer, the spacer transfer is detrimental to device performance.

IV. MONTE CARLO SIMULATION

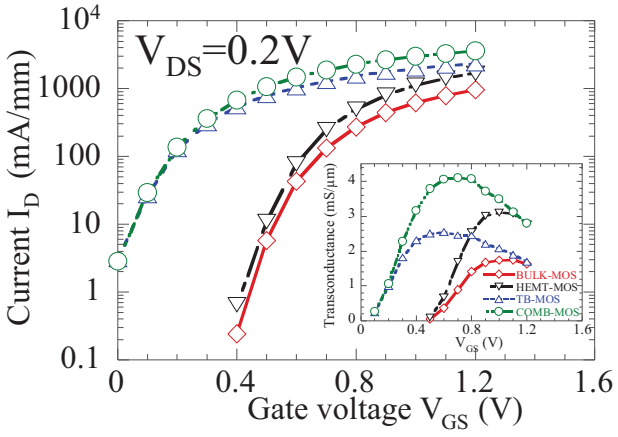

Figure 4 I_D-V_{GS} characteristics for four 50 nm MOSFET structures. Inset: transconductance g_m -V_{GS} curves.

Besides, using a semi-classical (no quantum correction) Monte Carlo (MC) device simulator with convenient scattering mechanisms (phonon, roughness, alloy and piezo scattering) and energy band model (analytical non parabolic Γ and L valleys) described in Refs [11,13], we carried out I-V studies. The simulator has been previously calibrated in static regime against experimental data for HEMTs [11]. Fig. 4 shows intrinsic (no external parasitic elements are included) I_D-V_{GS} transfer characteristics for the four MOSFET structures at V_{DS} = 0.2 V. The corresponding intrinsic transconductances g_m are presented in the inset of Fig. 4. For low power specifications, the subthreshold swing (SS) should be as low as possible [8]. According to these criteria, structures with undoped channels appear unsatisfactory. Indeed, even with a 10 nm-thick body, the subthreshold control in TB-MOS and COMB-MOS is poor. In contrast, Bulk-MOS and HEMT-MOS exhibit a good normally-off behaviour. Thanks to the effective mobility improvement in the channel, I_D and g_m are enhanced for the three alternative structures, in particular for devices with undoped channel (i.e. TB-MOS and COMB-MOS) in comparison with Bulk-MOS. Besides, the percentage of fully ballistic electrons in these devices (no scattering mechanisms undergone) at the end of channel was calculated: 8% for Bulk-MOS, 22% for HEMT-MOS, 37% for TB-MOS, and 55% for COMB-MOS. Thanks to strongly out of equilibrium or even quasi ballistic transport, these alternative III-V structures present high performance even at low V_{DS} (0.2 V), which is mandatory to achieve low dynamic power consumption. Moreover, in static regime, we can also estimate the intrinsic current gain cutoff frequency by the quasi-static formulas $f_T=g_m/2\pi(C_{GS}+C_{GD})$, where $C_{GS}+C_{GD}=d(Q_{tot})/dV_{GS}$ for a given value of V_{DS} (here 0.2 V). Q_{tot} is the average total charge inside the device of static MC simulation. f_T values are showed as a function of the gate voltage in Fig. 5. The results are compared to the 50 nm long HEMT with and without realistic external parasitic resistances R_{ds}. It should be mentioned that f_T strongly decreases when realistic parasitic elements are included. However, the study of the intrinsic performance is fully sufficient to provide a relevant benchmark between devices.

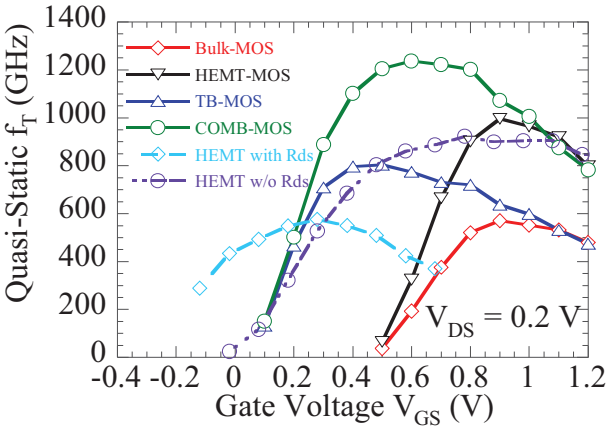

Figure 5 Estimated cut-off frequencies in quasi-static regime. R_{sd} represents the parasitic resistance of the source and drain

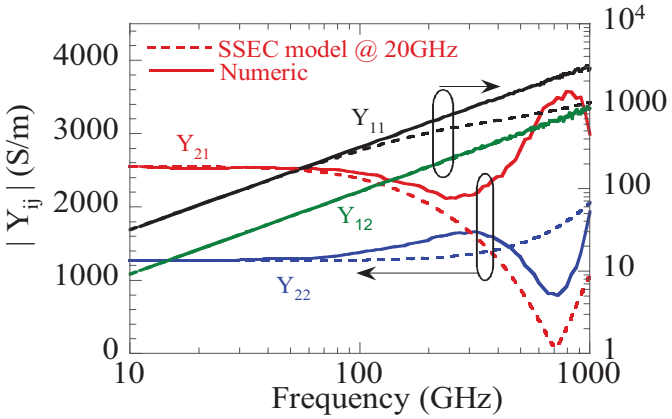

Figure 6 Calculated admittance parameters Y_{ij} as a function of frequency for TB-MOS at V_{GS} = 0.5 V and V_{DS} = 0.2 V.

Among the numerous advantages of semi-classical MC simulation, the transient analysis of the device allows advanced investigations of the frequency response. Accurate complex frequency-dependent two-port admittance parameters Y_{ij} can be directly extracted over a wide frequency range directly from transient currents provided by MC simulation. The instantaneous terminal currents were calculated on the basis of the Ramo-Shockley theorem for time-varying electrode potentials [14-17]. In RF analysis, the DC bias point is tuned to reach maximum g_m. Thus V_{GS} is chosen equal to 1.0 V for Bulk-MOS, 0.5 V for TB-MOS, 0.9 V and 0.6 V for HEMT-MOS and COMB-MOS, all biased at V_{DS} = 0.2 V. Fig. 6 shows the Y parameter extracted for the TB-MOS structure as a function of frequency up to 1 THz. The small-signal equivalent circuit (SSEC) is also frequently used to provide a more functional characterization of the device. We considered the typical intrinsic SSEC for the studied MOSFETs in common-source configuration, whose different elements were calculated from the Y

parameters [16]. The Y parameters extracted using these SSEC elements at 20 GHz are also plotted in dotted lines in Fig. 6. Y_{11}, Y_{21} and Y_{22} from SSEC show significant differences above 200 GHz, but the proposed equivalent circuit is valid for lower frequencies. Thanks to Y parameter extraction, we can derive different RF figures of merit such as the intrinsic cut-off frequency f_{T_exact} via the absolute value of current gain $h_{21} = |Y_{21}|/|Y_{11}|$ directly calculated from MC simulation. Fig. 7 shows the current gain with drain short-circuited as a function of the frequency for the four MOSFET structures. Above 200 GHz its behavior cannot be described within the quasi-static approximation (-20 dB/dec extrapolation to obtain f_{T_extrap}, see Fig. 5). These MOS structures and in particular HEMT-MOS and COMB-MOS exhibit performance comparable to or even higher than that of HEMT, as summarized in Table I (without any external parasitic impedances).

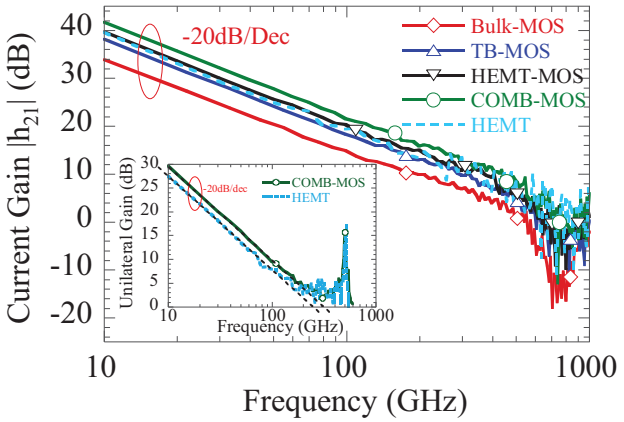

Figure 7 Current gain against frequency with drain short-circuited. Inset: unilateral gain versus frequency.

L_{ch} 50nm	f_{T_extrap} (GHz)	f_T (GHz)	f_{MAX} (GHz)	SS (mV/dec)
Bulk-MOS	530	520	200	75
TB-MOS	800	600	300	102
HEMT-MOS	990	690	580	80
COMB-MOS	1230	750	600	102
HEMT	900	630	540	110

Table 1 Summary of intrinsic RF and OFF-State performance at low V_{DS}

Our simulator allows us to evaluate other RF figures of merit as the maximum oscillation frequency f_{MAX} [18]. The inset of Fig. 7 shows the behavior of the unilateral gain G_u as a function of frequency for COMB-MOS and HEMT. The decay of 20dB per decade corresponds to the 'low frequency' behavior. At about 500 GHz, G_u shows a resonance peak in both structures. At the resonance frequency, another pole is added to the frequency behavior of G_u [19], which can lead to a substantial difference between the extrapolated f_{MAX_extrap} (COMB-MOS: 200 GHz in the inset of Fig. 7) within quasi-static approximation and the exact value of f_{MAX} (600 GHz in the inset of Fig. 7).

V. CONCLUSION

The charge control in several structures of InGaAs-based capacitors has been studied using a Schrödinger/Poisson solver. The use of low gate voltage is needed to avoid electron transfer into heavy L valleys and thus to take advantage of good transport properties of InGaAs. However, only relatively low gate capacitance can be achieved (about 50% of the C_{ox} limit) using an 8 nm-thick Al_2O_3 gate oxide due to low InGaAs DOS. Besides, our 2D calculations show that geometry effects such as fringing capacitances (up to more than 50% of C_G) and DIBL are important in undoped 50 nm long FET structures.

Four different III-V MOSFETs have been compared to a standard HEMT structure with the same gate length in both static and dynamic regimes using Monte Carlo device simulation. The validity of the standard small-signal equivalent circuit model appears questionable for frequency beyond 200 GHz since results obtained from MC time-varying simulations significantly differ at higher frequency. Finally, even with disappointing C_G, III-V MOSFETs exhibit remarkable performances at low V_{DS} (0.2 V). III-V Bulk-MOS and even better HEMT-MOS devices with reasonably thin oxide (8 nm) appear to be very promising low power architectures.

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