# **Steep-Slope Nanowire Field-Effect Transistor (SS-NWFET)**

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Abstract—In this work we propose a novel device concept with nearly ideal switching properties: i) a sustained inverse switching-slope as small as 3 mV/dec at room temperature; ii) no appreciable degradation of the on-current and, iii) a large output conductance at low drain voltage, which represents an essential property for rail-to-rail switching in logic applications. These extraordinary properties could posibly be achieved by shaping the density of states in the conduction band so as to generate a first subband with a small energy extension, and a second subband widely displaced in energy, so that its contribution to the drain current is negligible. Computer simulations accounting for the idealized band structure depicted thus far confirm the steep-slope turn-on characteristics of this ideal device, and give an insight on the optimal band-structure parameters.

#### Introduction

Power consumption is reportedly the most important limitation for high-performance logic. For this reason, the clock frequency of advanced processors has not improved beyond the limit of 4 GHz, and further progress is being sought at the architectural level by exploiting parallelism, rather than reducing the cycle time. The growth of power consumption over the years is due to several reasons: i) the supply voltage has not been scaled in direct proportion with the feature size due to the nonscalability of the oxide thickness; ii) static power dissipation due to channel leakage grows exponentially with the reduction of the threshold voltage and, iii) the gate oxide has become leaky due to electron tunneling. While the latter problem has been addressed by working out high- $\kappa$  dielectrics, the two former problems are related with the non-scalability of the subthreshold slope, which has not found any viable solution vet.

The objective of a steeper current turn-on rate has been pursued by several approaches, which can be classified in two main categories. The first class of devices is based on the introduction of a positive feedback in the turn-on mechanism. Examples of this approach are the impactionization MOS (I-MOS) [1], the nano-electromechanical FET (NEMFET) [2], [3], and the negative gate-capacitance ferroelectric FET (Fe-FET) [4]. The second class of devices is based instead on a filtering of the high-energy electrons injected into the channel. The typical example of this device class is the tunnel FET (T-FET) [5], [6], [7], where the filtering function is demanded to the band-to-band tunneling mechanism.

Positive-feedback devices can be characterized by very steep switching slopes, but are affected by severe limitations. The I-MOS FET requires the application of a drain voltage large enough to allow for avalanche multiplication to occur at the drain end of the channel. This means that, even for an optimized design, the drain voltage  $V_{DS}$  must exceed the breakdown voltage  $V_{BD}$  which, in turn, cannot be smaller than  $\simeq 1.5 E_g/q$ ,  $E_g$  being the semiconductor band gap. Thus, an inverter made by two I-MOS FETs would exhibit a logic swing between  $V_{BD}$  and  $V_{DD}-V_{BD}$ . Stacking a few devices for multiple-input logic gates would thus become impossible.

The NEMFET is also affected by several drawbacks: besides requiring a scaling of the metallic cantilever down to a nanometric size, stitching and reliability problems related with fatigue make its use for logic applications highly unlikely. Finally, the Fe-FET [4] is perhaps the most promising device in its class, but replacing the gate oxide with a ferroelectric insulator rises severe fabrication, contamination and scalability problems, and ferroelectric materials are again subject to fatigue-related degradation. The T-FET exhibits severe limitations as well. First, the on-current is heavily degraded by the injection mechanism; next, the switching slope is not uniform due to the changing barrier width against gate and drain voltages, and its average value over an extended range of drain currents is fairly disappointing. Finally, the upward curvature of the output characteristics and the related small drain conductance at zero  $V_{DS}$  would again prevent rail-to-rail logic swings. Even carefully optimized designs based on strained-SiGe or Ge heterostructure T-FETs and high- $\kappa$  gate dielectrics achieve an improved on-current, but can hardly compete with standard CMOS FETs at the same supply voltage [8], [9].

In this work we reverse the usual simulation approach which starts from a realistic device, both in terms of materials and geometry, and aims to optimize its performance by suitably modifying some details of its morphology. Rather, we focus on an idealized band structure which ensures a filtering of the high-energy electrons injected into the channel and aim to identify the band-structure parameters which ensure an optimal device performance both in terms of its on-current and of its static and dynamic power dissipation. In order to do so, it is necessary to work out the steepest possible transition between the on and off conditions, so that the supply voltage and the switching threshold can be scaled down without appreciably impairing the leakage



Fig. 1. Potential energy vs. position within the NW-FET. Inset: dispersion relationships for the two lowest subbands. Top: at low  $V_{GS}$  electrons from the lowest subband cannot be injected into the device channel, since the potential barrier at the source end is higher than the top edge of the first subband. Bottom: at higher  $V_{GS}$  electrons are injected from the source into the channel, since the potential barrier is lower than the top edge of the first subband.

current. Quantum simulations properly accounting for the device subband structure are carried out using a cylindrical nanowire FET, but any other geometry could be conceivably used for the purpose of this work. The identification of the appropriate materials and geometries which best approach the idealized band structure worked out here will be the subject of a subsequent work.

### **Band structure description**

The MOSFET turn-on characteristic in subthreshold is expressed by the law  $I_D = I_{D0} \exp\{q(V_{GS} - V_T)/nk_BT\}$ , with  $k_B$  the Boltzmann constant, T the lattice temperature and n an ideality factor close to unity. This constant slope on a log plot (at most one current decade every 60 mV at room temperature for n = 1) is rooted in very basic thermodynamic principles which are a consequence of Fermi statistics, i.e. the law which governs the electron energy distribution in equilibrium among the available electronic states within the semiconductor at a given temperature.

As we cannot change Fermi statistics, we intend to shape the density of states within the conduction band so that current injection into the device channel is prevented in subthreshold. This goal can be achieved if the upper edge of the first subband at the source contact  $E_{cu}(0)$  is lower than the height of the energy barrier at the virtual source  $E_c(x_m)$ , and if the second lowest subband is widely displaced from the first one, as depicted in the inset of fig. 1, so that the current flowing in the second subband is negligible. A similar subband structure has been found in thin nanowires of different materials with specific channel orientations [10].

If this is the case, electrons in the first subband will be unable to surmount the potential barrier at low  $V_{GS}$ , as shown in the upper part of fig. 1. At the same time, the



Fig. 2. SS-NWFET turn-on characteristics at  $V_{DS} = 50 \text{ mV}$  for different values of the subband extension  $\Delta E_c$  and source impurity concentration  $N_S$ . The switching voltage increases as  $\Delta E_c$  varies from 400 to 200 meV and for increasing  $N_S$  values. The inverse switching slope is roughly SS = 3 mV/dec. The dotted line represents the analytical model (1) with  $N_S = 10^{20} \text{ cm}^{-3}$  and  $\Delta E_c = 0.2 \text{ eV}$ .

second and higher subbands will be nearly empty due to the decay of the Fermi function. Thus, no appreciable current will flow in subthreshold. On the other hand, when the barrier is lowered by the increasing gate voltage below  $E_{cu}(0)$ , the superposition of the subbands in the source, channel and drain allows electrons in the energy window  $E_c(x_m) < E < E_{cu}(0)$  to be injected into the channel, as shown in fig. 1, bottom. The NW-FET is thus expected to turn on suddenly with a sharp transition to the on-state due to the relatively-large occupation probability of the energy states close to  $E_{cu}(0)$ .

Another requirement of the device band structure is that the narrow subband cannot extend up to the drain. Otherwise, the ovelap window of the subbands in the source, channel and drain becomes more and more restricted at large drain voltages, as can be inferred from figure 1, with the consequence of an undesired current falloff. In order to prevent such a misalignment, it is necessary to restrict the narrow-subband material either within the source extension, or in the first half of the channel up to the top of the barrier, or in both the above regions. This goal can be achieved by shaping the nanowire diameter, to make it wider near the drain.

#### Simulation results

Fig. 2 shows a quantum simulation of the SS-NWFET turn-on characteristics at  $V_{DS} = 50 \text{ mV}$  for different values of the subband extension  $\Delta E_c = E_{cu} - E_{cl}$  and of the source impurity concentration  $N_S$ . The simulation approach [11] accounts for the assumed dispersion relationship, which is a periodic and even function extended from  $-\pi/a$  up to  $\pi/a$ , with a the lattice constant. E(k) is parametrically modeled in order to provide the desired values of the lower and upper subband edges, and the requested effective masses at k = 0 and  $k = \pm \pi/a$ .



Fig. 3. SS-NWFET turn-on characteristics both in log and linear plots. The metal work function has been adjusted to fix the switching voltage at  $V_{sw} = 50$  mV. By lowering the carrier effective mass from  $m^* = 2.5 m_0$  to  $m^* = 0.35 m_0$ , the switching slope SS degrades from 3 to 9 mV/dec, as shown by the dashed curve.

With the chosen parameters, the inverse switching slope is as small as 3 mV/dec and its finite value is due to a source-drain tunneling current which develops when the energy barrier  $E_c(x_m)$  approaches  $E_{cu}(0)$ . Such an inverse slope is weakly dependent on  $\Delta E_c$  and/or the position of the subband relative to the Fermi level in the source, but is also a sensitive function of the electron effective mass, as discussed below. The switching voltage  $V_{sw}$  differs from the traditional threshold voltage and is instead strictly related to  $E_c(x_m) - E_{cu}(0)$  at  $V_{GS} = 0$ . Thus, lowering  $\Delta E_c$  and/or the position of the subband relative to the Fermi level increases  $V_{sw}$  without appreciably altering the shape of the on-portion of the drain current. On the other hand, the metal work function  $\Phi_M$  is an independent parameter which can be adjusted to shift the characteristics to the appropriate switching voltage.

By neglecting source-to-drain tunneling effects, a compact model based on an analytical solution of the BTE under ballistic conditions can be derived by integration of the carrier flow from  $E_c(x_m)$  to  $E_{cu}(0)$ . We find

$$I_D = \frac{2qk_BT}{h} \left\{ \log\left(\frac{1 + \exp\left(\eta_{FS} - \varepsilon_c(x_m)\right)}{1 + \exp\left(\eta_{FS} - \varepsilon_{cu}(0)\right)}\right) - \log\left(\frac{1 + \exp\left(\eta_{FD} - \varepsilon_c(x_m)\right)}{1 + \exp\left(\eta_{FD} - \varepsilon_{cu}(0)\right)}\right) \right\}$$
$$\Theta(\varepsilon_{cu}(0) - \varepsilon_c(x_m)) \tag{1}$$

where  $\varepsilon_c(x_m)$  represents the normalized lower edge of the first subband at the virtual source;  $\varepsilon_{cu}(0)$  is the normalized upper edge of the first subband at the source contact;  $\eta_{FS}$  and  $\eta_{FD}$  are the normalized Fermi energies at the source and drain contacts, respectively, and  $\Theta(x)$  is the step function. Clearly,  $\eta_{FD} = \eta_{FS} - qV_{DS}/k_BT$ ; also, by defining  $\varepsilon_{c0}(x_m)$  the normalized barrier height at  $V_{GS} = 0$ , we may assume  $\varepsilon_c(x_m) = \varepsilon_{c0}(x_m) - qV_{GS}/nkBT$  with n



Fig. 4. SS-NWFET output characteristics. The perfect saturation of these curves is due to the vanishing DIBL exhibited by this device, and the large drain conductance at zero  $V_{DS}$  ensures rail to rail switching in logic applications.

an ideality factor, thus making the current dependence upon gate and drain voltages fully explicit. In eq. (1) the first term in braces represents the electron flow from source to drain, while the second term represents the opposite flow from drain to source. Eq. (1) is plotted in figure 2 as a dotted line with  $N_S = 10^{20} \,\mathrm{cm}^{-3}$  and  $\Delta E_c = 0.2 \,\mathrm{eV}$ . The agreement with the corresponding numerical turn-on characteristics is nearly perfect above threshold, while the transition from the off to the on state is made abrupt by the step function. Fig. 3 shows the SS-NWFET turn-on characteristics at  $V_{DS} = 50, 200, 300$  and  $400 \,\mathrm{mV}$ . The computation is carried out with a work function  $\Phi_M = 4.13 \,\mathrm{V}$ , a value fairly close to that of an n<sup>+</sup> poly-gate. With a subband extension  $\Delta E_c = 200 \text{ meV}$  and  $N_S = 10^{20} \text{ cm}^{-3}$ , the above choice fixes  $V_{sw}$  at around 50 mV. It should be noticed that the switching transitions are perfectly overlapped for all characteristics, indicating that the drain-induced barrier lowering (DIBL) is negligible in this device structure.

As is well known, in 1D ballistic transport the effective mass of the carriers plays no role, as the effectivemass dependences of the density of states and of the group velocity cancel out. Therefore, the on-current is only marginally affected by the group velocity, giving slightly different carrier and potential distributions. However, the effective mass plays an important role in the SS-NWFET switching slope, which is due to source-drain tunneling. In our simulation, we used an effective mass  $m^* = 2.5 m_0$ compatible with a superlattice filter structure. The dashed turn-on characteristic has been computed instead with an effective mass  $m^* = 0.35 m_0$ . As may be seen, the inverse switching slope is degraded in this case to roughly 9 mV/dec on average over the whole simulation range.

The output characteristics of the nanowire FET are shown in figure 4. A nearly-perfect saturation of the drain current is observed and, most important, a large drain conductance



Fig. 5. SS-NWFET output characteristics with a uniform band structure extended from the source to the drain contacts. For increasing values of the drain voltage, the energy window allowing the carrier free motion at constant energy from source to drain becomes narrower and narrower, until it closes completely. Hence, the current falloff exhibited by the output characteristics.

at zero  $V_{DS}$  is shown. Therefore, complementary logic gates using this kind of switch are expected to operate from rail to rail, as for standard CMOS gates. With the selected device geometry the on-current  $I_{on} \simeq 6 \,\mu\text{A}$  at a supply voltage of  $V_{DD} = 400 \,\text{mV}$  and  $I_{on} \simeq 0.6 \,\mu\text{A}$ at  $V_{DD} = 200 \,\text{mV}$ . Thus, this device can operate both as a high-performance (HP) FET with no subthreshold leakage and as a low-power (LP) FET at the same switching voltage, i.e. with improved performance and no structural modifications.

Finally, figure 5 clarifies the motivation for an energyextended subband in the drain region. If we keep a uniform subband from source to drain with  $\Delta E_c = 0.2$  V, at larger drain voltages the energy window seen by electrons traveling ballistically from source to drain becomes narrower and narrower, until it closes completely. Correspondingly, we observe a current falloff and a negative drain conductance until the drain current drops to zero. The consideration of scattering would probably smear out this effect, but the main avenue to prevent it is that of modulating the subband extension at the drain end of the channel and within the drain by profiling the channel diameter.

## Conclusions

In this work we propose a novel concept for the achievement of an enhanced switching-slope FET based on the filtering of the high-energy electrons injected into the channel. In this device, the switching from the off to the on-state occurs when the summit of the energy barrier at the virtual source crosses the upper edge of the first subband. Therefore, the switching voltage differs from the threshold voltage, traditionally defined as the onset of strong inversion, and the former can be adjusted by fixing two independent parameters, namely the metal-gate work function and the subband extension.

From our quantum simulations, it turns out that the SS-NWFET switching properties are nearly ideal, and promise to make it possible scaling the supply voltage down to 200 mV, if the variability issue is under control. Another strength of this device is the large drain conductance at low drain voltages, required to ensure rail-to-rail voltage swings in logic gates. Finally, the switching slope of the turn-on characteristics is a sensitive function of the carrier effective mass, which must be as large as possible in order to limit source-to-drain tunneling. In this case, however, the steeper slope would be achieved at the expence of a slightly-reduced on-current due to an increased scattering rate.

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