Si Nanowire Device and its Modeling

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***Abstract*— Because of its nature of effectively suppressing the off-leakage current with gate around configuration, the Si nanowire FET has been thought be the ultimate structure for for ultra-small CMOS devices towards their downsizing limit. Recently, several experimental data of Si nanowire FETs with very high on-current much larger than that of planar MOSFETs have been published. Thus, Si nanowire FETs are now drawing attention as the most promising candidate for the mainstream CMOS devices in 2020s. In order for the Si nanowire FETs to be introduced into integrated circuits, good compact models which circuit designers can easily handle with are essential. However, it is a really challenging task to establish the compact model, because I_d-V_d characteristics of the Si nanowire FETs are affected by the band structure of the nanowire, and the band structure are very sensitive with the nanowire diameter, cross-sectional shape, crystal orientation, mechanical stress, and interface states. In this paper, recent research status of Si nanowire FETs in experimental and theoretical works are described.**

I. INTRODUCTION

Three dimensional Si nanowire structures provide us many possibilities for new applications such as transistors, memories, sensors, light-emitting diodes and photovoltaic cells. Among them, Si nanowire FETs are now drawing attention. Because of its nature of effectively suppressing the off-leakage current with its gate around configuration, Si nanowire FET has been thought be the ultimate structure for ultra-small CMOS devices towards their downsizing limit [1]. Recently, several high-performance experimental data of Si nanowire FETs with very high on-current much larger than that of planar MOSFETs have been published [2-5], and thus, Si nanowire FETs are now regarded as the most promising candidate for the mainstream CMOS devices in 2020s. In fact, according to ITRS 2009, planar MOSFETs will disappear from the advanced MOSFET structure, and 3D multiple gate (or Fin type) structure will be introduced because of its nature to easily suppress the short-channel effects (SCE) as shown in Fig. 1 [6]. It is a natural trend that the Fin FETs will change to nanowire FETs, because of more control of SCE and more channel area as the nanowire surface in a unit area as shown also in the figure.

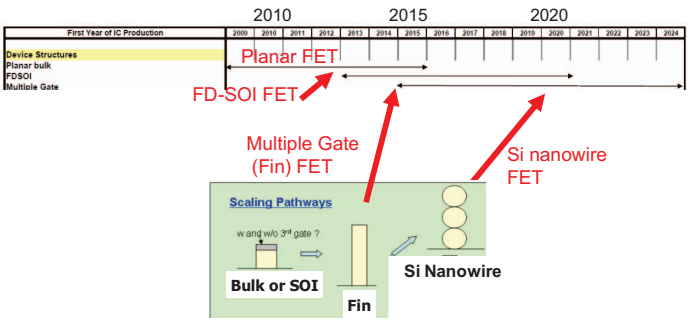

Figure 1 MOSFET structure trend in ITRS 2009

In order for the Si nanowire FETs to be introduced into integrated circuits, good compact models which the circuit designers can easily handle with for the design are essential. However, it is a really challenging task to establish the compact model, because the I_D-V_D characteristics of the Si nanowire FETs are affected by the band structure and the band structure are very sensive with the nanowire diameter, cross-sectional shape, crystal orientation, mechanical stress, and interface states. In this paper, recent research status of Si nanowire FETs in experimental and theoretical works are described.

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II. SI NANOWIRE FET ADVANTAGE

Si nanowire FETs have several advantages as the candidate of main stream CMOS devices for 2020s as shown in Fig. 2 [1].

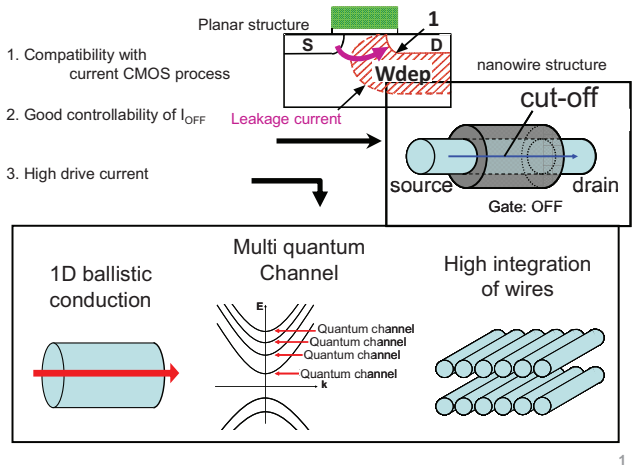

Figure 2 Advantages of Si nanowire FET over planer

First of all, the ability of the suppression of the short-channel effects and thus, the suppression of the off-leakage current of Si nanowire FETs are expected to be very good, because of the gate surrounding configuration.

Secondly, Si nanowire FETs are expected to have high on-current because of the following 3 reasons. One is the nature of quasi-one-dimensional conduction of thin nanowire with small freedom of the carrier scattering angle [7]. Because of the small freedom of the carrier scattering, its conduction will be high. Second is the use of multi-quantum channels for the conduction. Si nanowire band structure is quite different from that of the bulk and many conduction sub-bands appear near the lowest sub-band [8] as shown in Fig.3. Those sub-bands contribute to the conduction as the gate voltage increase.

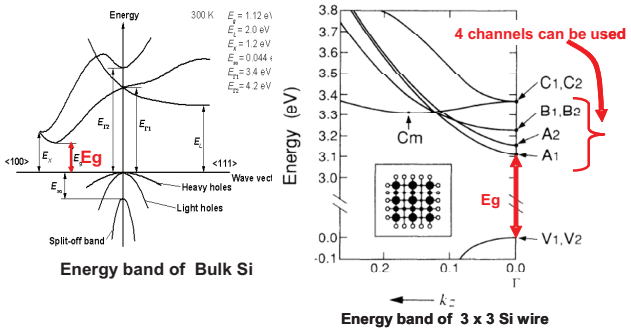

Figure 3 Band structure for Si bulk (right) and nanowire (left).

Thirdly, multilayer nanowire can be implemented easily by utilization of Si/Ge multi-layers [2,9] as shown in Fig.4

For the fabrication, basically, today's conventional Si CMOS integrated circuit production process can be used almost as it is to fabricate Si nanowire FET, although process tuning kind of developments are necessary. This is a very big advantage for the production to minimize the risk and cost of the new process technology development. Furthermore, number of Si nanowire FET fabrication process will be smaller than that of today's planar CMOS. It is assumed that no channel implantation including that of halo is necessary because of good short-channel effect control of the nanowire structure, assuming that threshold voltage control can be done by the workfunction control of gate stack. In some future, metal or silicide source/drain is assumed to be introduced into ultra-short channel Si nanowire FETs because of the necessity of abrupt junction, resulting in the further elimination of source/drain doping.

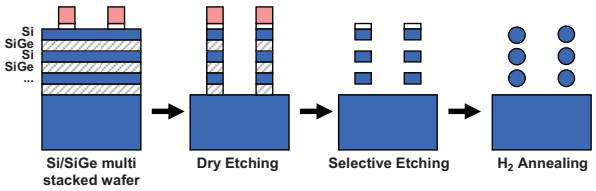

Figure 4 Fabrication of multilayer nanowire.

III. MODELING

For modeling of the conduction of the Si nanowire FETs, information of the band structure or *E-k* relation of the band is necessary.

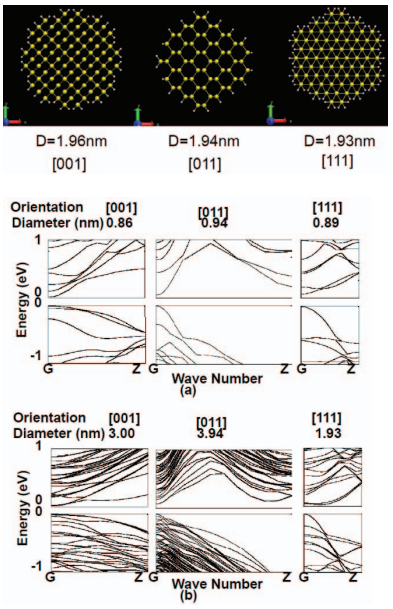

Figure 5 Calculated nanowire band structures

Figure 5 show the calculated nanowire band structures by first principle method with different wire orientation and diameter [10]. With increasing the diameter of the Si nanowire from 0.86 nm (middle in the figure) to 3.0 nm (bottom), the number of the sub-bands or the number of the quantum channel increases. This means the increase in the conduction. However, it is careful that that carrier scattering between the sub-bands increases with in crease in the number of the sub-band. Thus, there will be the optimum diameter of the nanowire, considering the trade off between the quasi-one-dimensional ballistic conduction and number of the

quantum channels. The diameter also needs to be determined by the suppression of SCE or the off-leakage current. Recently, the band structure of Si nanowires with diameter to 10 nm with 10,000 Si atoms even with surface roughness can be calculated with first-principle Real Space Density Functional Theory (RSDFT) [11] as shown in Fig. 6, and diameter and orientation dependence of the nanowire FET conduction being analyzed using this method on a massively-parallel computer cluster with a theoretical peak performance of several TFLOPS

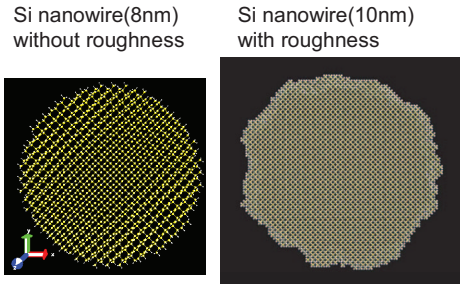

Figure 6 Nanowire cross-section used for the calculation

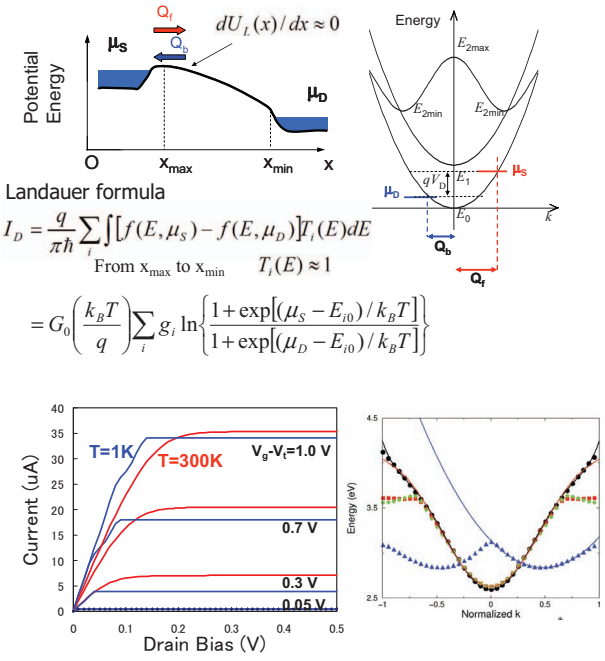

Figure 7 Compact model approach for Si nanowire FET under the assumption of ballistic conduction

Simple compact model of Si nanowire MOSFETs under the assumption of ballistic conduction [12] is obtained using Landauer formula [13] as shown in Fig.12. Here, $f(E, \mu_S)$ is the Fermi distribution function, E is energy, and μ_S and $\mu_D = \mu_S - qV_D$, are Fermi levels associated with source and drain electrodes, respectively. $Ti(E)$ represents the transmission coefficient of the carrier in the ith subband from source to drain, and G_0 is the quantum conductance $G_0 \equiv 2q^2/h = 77.8$ μS. μ_S is obtained by the relationship between the gate overdrive and the carrier density, and E-k relation of the band structure [12]. The calculated I_D-V_D characteristics by employing the subband parameter of the 7 × 7-atom [110] square parameter of the 7 × 7-atom [110] square nanowire extended in the (100) direction derived by the density functional calculation [14] is also shown in the figure. The room-temperature I_D–V_D characteristics are similar to those of an ordinary MOSFET. On the other hand, at low temperatures, the curve shows kink structures when the Fermi level crosses the subband minimum and displays a similar magnitude to that of room-temperature curves.

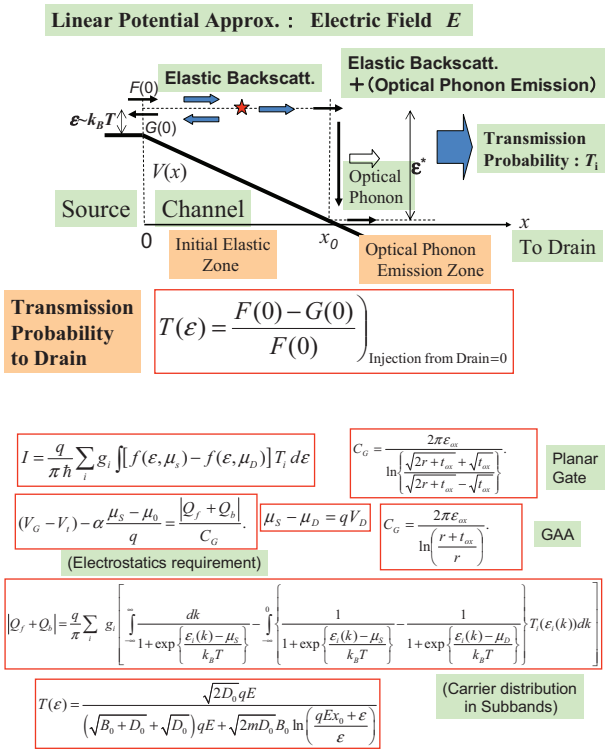

Figure 8 Compact model approach including scattering

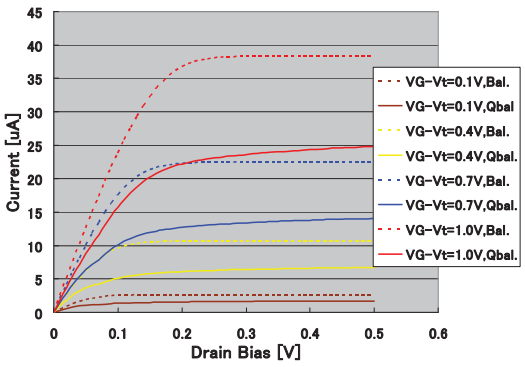

Figure 9 Calculated I_D-V_D characteristics with the scattering model. Solid line: ballistic model, Broken line: with scattering B_0 : 700cm^2/Vs D_0 : 4×10^{-13}sec

In order to include the carrier scattering effect, the channel area is modeled to be divided into 2 regions; the first region next to the source, where the carrier energy is assumed to be smaller than the optical phonon energy and only elastic

scattering occurs; the second region next to the first, where the carrier has a larger energy than the optical phonon caused by the acceleration of the lateral electric field and inelastic scattering with the optical phonon decreases the carrier energy as shown in Fig.8 [15, 16]. The pseudo-one-dimensional Boltzmann equation with a constant electric field is transformed into a pair of carrier flux equations. They are analytically solved neither with the relaxation time approximation nor with the perturbation expansion. The calculated results assuming the parameters B_0 and D_0 is shown in Fig. 9.

IV. EXPRERIMENTAL RESULTS

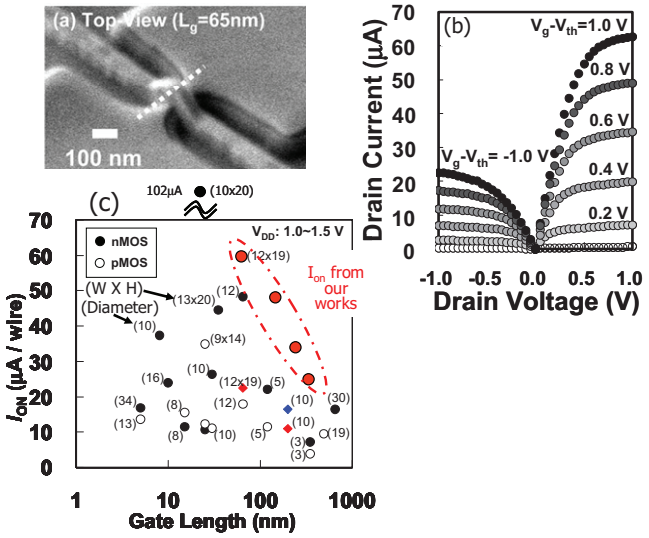

Figure 10 Experimental data: (a) SEM Photograph, (b) I_D-V_D Characteristics, (c) Bench marking with published data

The experimental data for Si nanowire FETs show very high drain current with good off-leakage control (I_{on}/O_{off} = 10^6), just for example [17]. Based on these experimental data, future Si nanowire FET on-current is estimated to be much higher than that predicted by ITRS 2009.

V. CONCLUSIONS

Si nanowire FETs show very good experimental results for the future main stream CMOS devices. There are many things to do for the modeling for the Si nanowire FETs to be introduced into the future products.

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