Topography simulation of BiCS memory hole etching modeled by elementary experiments of SiO_2 and Si etching

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***Abstract*—A topography simulation of BiCS memory hole etching is performed. The model parameters are fitted by elementary experiments of Si and SiO_2 etching, and BiCS topography simulation is performed without parameter fitting. Our new model describes the experimental topography of BiCS memory hole, including taper angles and undercuts of stacked films. The point of the modeling is that it takes into consideration removal of O-oriented deposition films by reflected ions from tapered SiO_2 sidewall.**

I. INTRODUCTION

Bit Cost Scalable (BiCS) flash memory (Fig.1) technology is a new concept of low-cost memory proposed by Toshiba [1]. One of the difficulties in the BiCS process is how to etch stacked films for making memory hole. The more stacked films can be etched in one lithography step, the lower the bit cost. We tried to model the BiCS etching process by the topography simulation. The model parameters were fitted by means of elementary experiments of Si and SiO_2 etching. And BiCS topography simulation was performed without parameter fitting to make a predictable model including basic phenomena.

II. MODELING

To model the etching process, we employ the topography simulator using the level set method with the surface reaction model, which was developed by Toshiba and released by Synopsys [2] (For BiCS simulation, we use a special version of the source code for BiCS cylindrical symmetry.) In this simulator, we can treat surface coverage, neutral diffusive reflections, and ion mirror reflections on any surfaces.

To etch BiCS memory hole, we used the "switching gas recipe process". We switch two etching gas recipes alternately, one mainly using fluorocarbon gas and the other mainly using halogen gas, for SiO_2 and Si etching, respectively. So we researched the each processes by means of elementary experiments.

A. Fluorocarbon gas process modeling for SiO_2 etching

It is generally known that experimental etching shape of SiO_2 has a taper angle caused by fluorocarbon deposition. In our SiO_2 etching recipe of BiCS memory hole, the taper angles of experimental shapes are about 5-7° and the micro loading effects are not so strong (Fig.2). So in our modeling, the main deposition precursor is CF_2 in this process, whose sticking coefficient is $\eta_{CF_{2gas}} = 0.0292$ [3] [4].

Gas phase reaction

$$CF_{4gas} + e^- \longrightarrow CF_{2\,gas} + 2F + e^- \quad (1)$$

Surface reaction

$$CF_{2\,gas} \xrightarrow{\eta_{CF_{2gas}}=0.0292} CF_{2bulk} \quad (2)$$

Fluorocarbon Deposition Rate

$$GR_{depo} = \frac{\eta_{CF_2}\Gamma_{CF_2}}{\rho_{CF_2}} - ER_{depo} \quad (3)$$

where ρ represents bulk density, Γ represents local flux, and $\mathbf{ER_{depo}}$ is etching rate of fluorocarbon by other species (Ar^+, O^*, and so on). If $\mathbf{GR_{depo}}>0$, deposition films grow. If $\mathbf{GR_{depo}}<0$, we calculate the etch rates of SiO_2.

SiO_2 Etching Rate $(GR_{depo} < 0)$

$$GR_{SiO_2} = -ER_{SiO_2}\left(\frac{GR_{depo}}{ER_{depo}}\right) \quad (4)$$

Our model can describe the taper angles of SiO_2 etching shapes (Fig.2, 3).

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B. *Halogen gas process modeling for Si etching*

In our Si etching recipe of BiCS memory hole, we found strong micro loading effects. The etching depth depends on opening width (Fig.4), and the sidewall erosion width depends on mask taper angle (Fig.5). This phenomenon can be modeled by ion-assisted etching; neutral etching has occurred on bare surface from which O-oriented deposition films are removed by ions (Fig.6).

Gas phase reaction

$$HBr_{gas} + e^{-} \longrightarrow H_{gas} + Br_{gas} + e^{-} \quad (5)$$

Surface reaction

$$O_{gas} + Si_{surf} \longrightarrow SiO_{surf} \quad (6)$$

$$Ar^{+} + SiO_{surf} \longrightarrow Si_{surf} + O_{gas} \quad (7)$$

$$Br_{gas} + Si_{bulk} + Si_{surf} \longrightarrow SiBr_{gas} + Si_{surf} \quad (8)$$

Si Etching Rate

$$GR_{Si} = \frac{\Gamma_{Ar^+}\Gamma_{Br}}{\rho_{Si}\left(\Gamma_{Ar^+} + \Gamma_{O}\right)} \quad (9)$$

Since reflected ions remove O-oriented deposition film on the sidewall, the sidewall erosion depth depends on mask taper angle. Our model can express both open width and mask taper angle dependency (Fig.4, 5). In addition, our model can describe the asymmetric sidewall erosion shape caused by asymmetric mask taper angle (Fig.7c).

III. Results And Disscusions

We performed BiCS memory hole etching simulation using parameters fitted by means of two elementary experiments. In spite of no fitting for stacked films, we can explain BiCS memory hole shapes (Fig.8). The undercut of the first layer is big because of reflected ions from SiO_2 mask. The deeper the layer is etched, the less is the sidewall erosion. This is caused by changing the amount of reflected ions from the tapered SiO_2 sidewall.

The etching shape was predicted for BiCS with more stacking, too (Fig.9).

IV. Conclusions

We have shown a topography simulation of BiCS memory hole etching based on the elementary modeling. The points of the modeling are

1. Sidewall taper angle caused by fluorocarbon depositions in SiO_2 etching

2. Removal of O-oriented deposition films by reflected ion from tapered SiO_2 sidewall in Si etching.

Our etching model facilitates 3D device developments, for example, inputs of device simulations, predictions of memory with more stacked films, and fabrication-less investigations of other types of 3D device.

Acknowledgment

The authors would like to thank Masao Iwase, Katsunori Yahashi, Mitsuhiro Omura, and Masaru Kido of Toshiba Corp. for helpful discussion.

References

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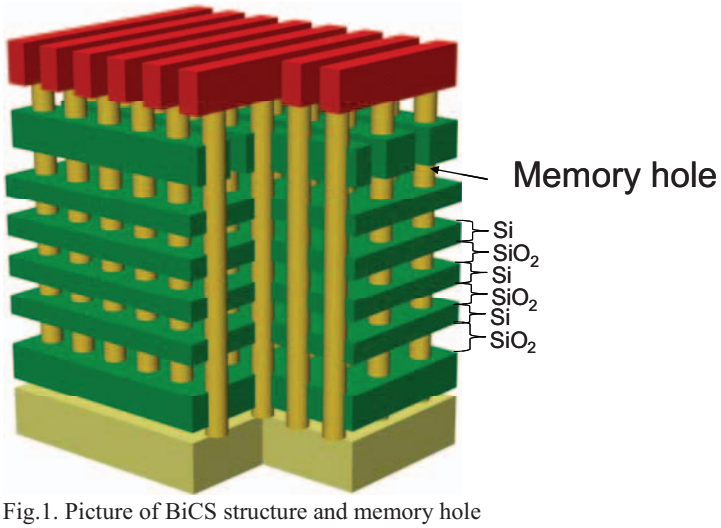

Fig.1. Picture of BiCS structure and memory hole

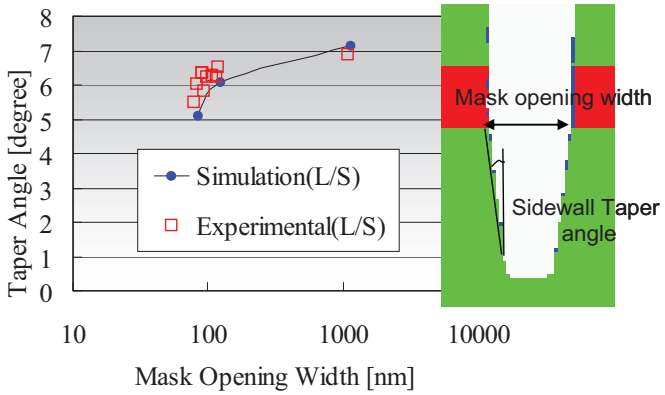

Fig.2. Experimental and topography simulation results of SiO_2 sidewall taper angle dependency on mask opening width

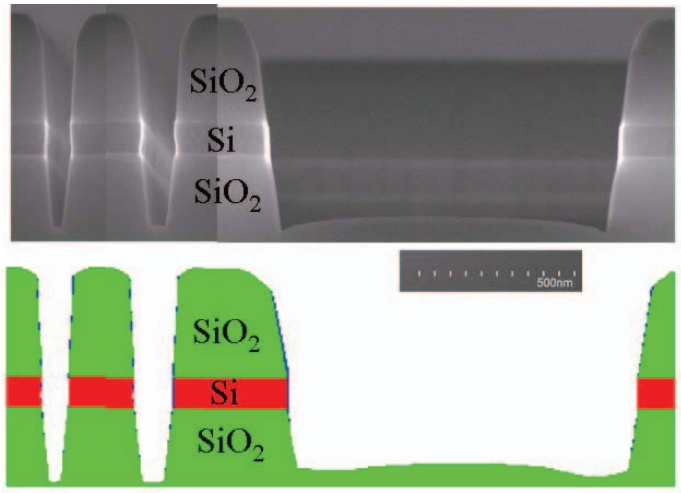

Fig.3. Experimental SEM and topography simulation results of SiO_2 etching by using fluorocarbon gas process. The taper angle assumed to be caused by fluorocarbon deposition on sidewall.

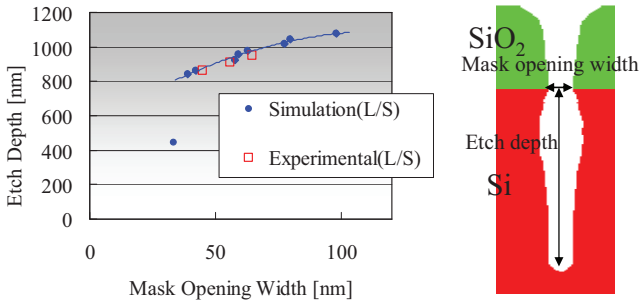

Fig.4. Experimental and topography simulation results of silicon etch depth dependency on mask opening width

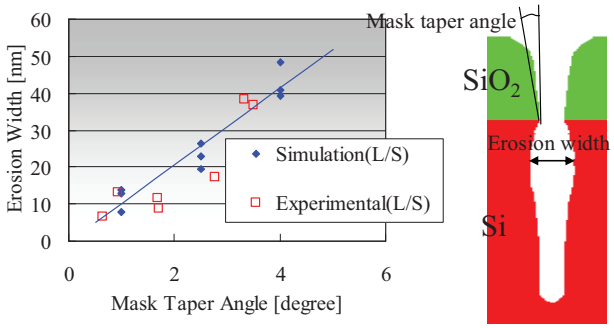

Fig.5. Experimental and topography simulation results of silicon side etch erosion width dependency on mask taper angle

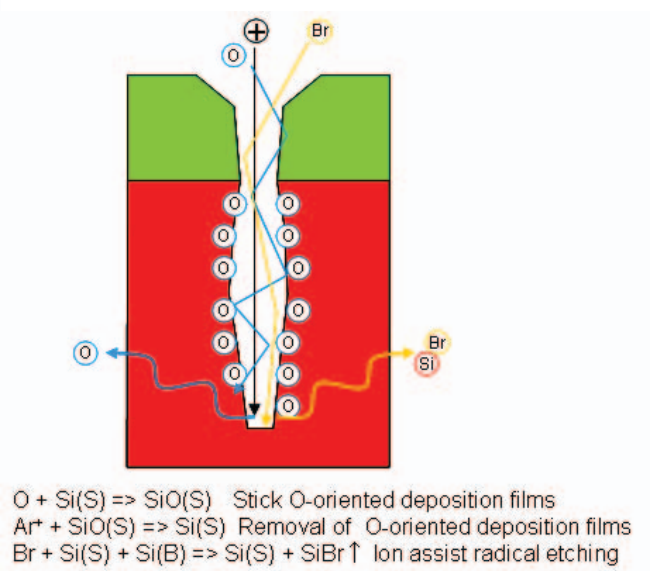

Fig.6. Modeling of Si etching process using halogen gas

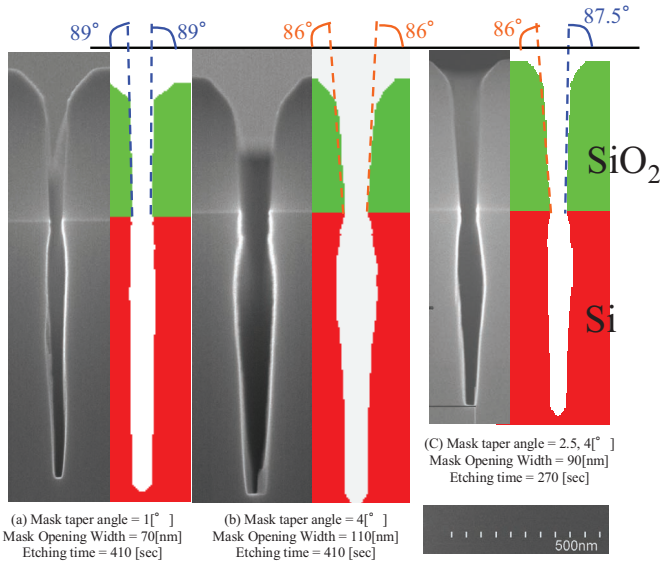

Fig.7. Experimental SEM and topography simulation results of Si etching by using HBr gas process. The erosion assumed to be caused by mask taper angle.

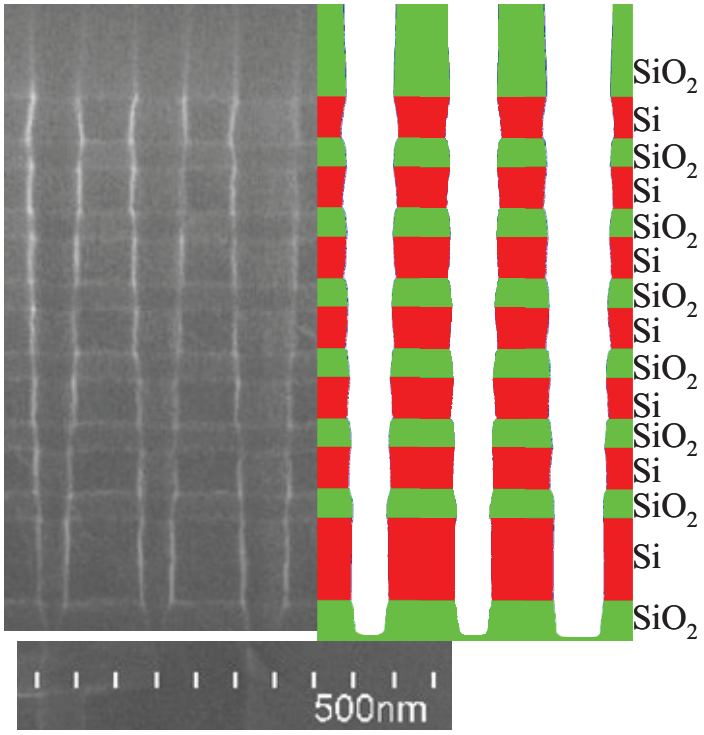

Fig.8. Experimental SEM and topography simulation results of BiCS memory hole

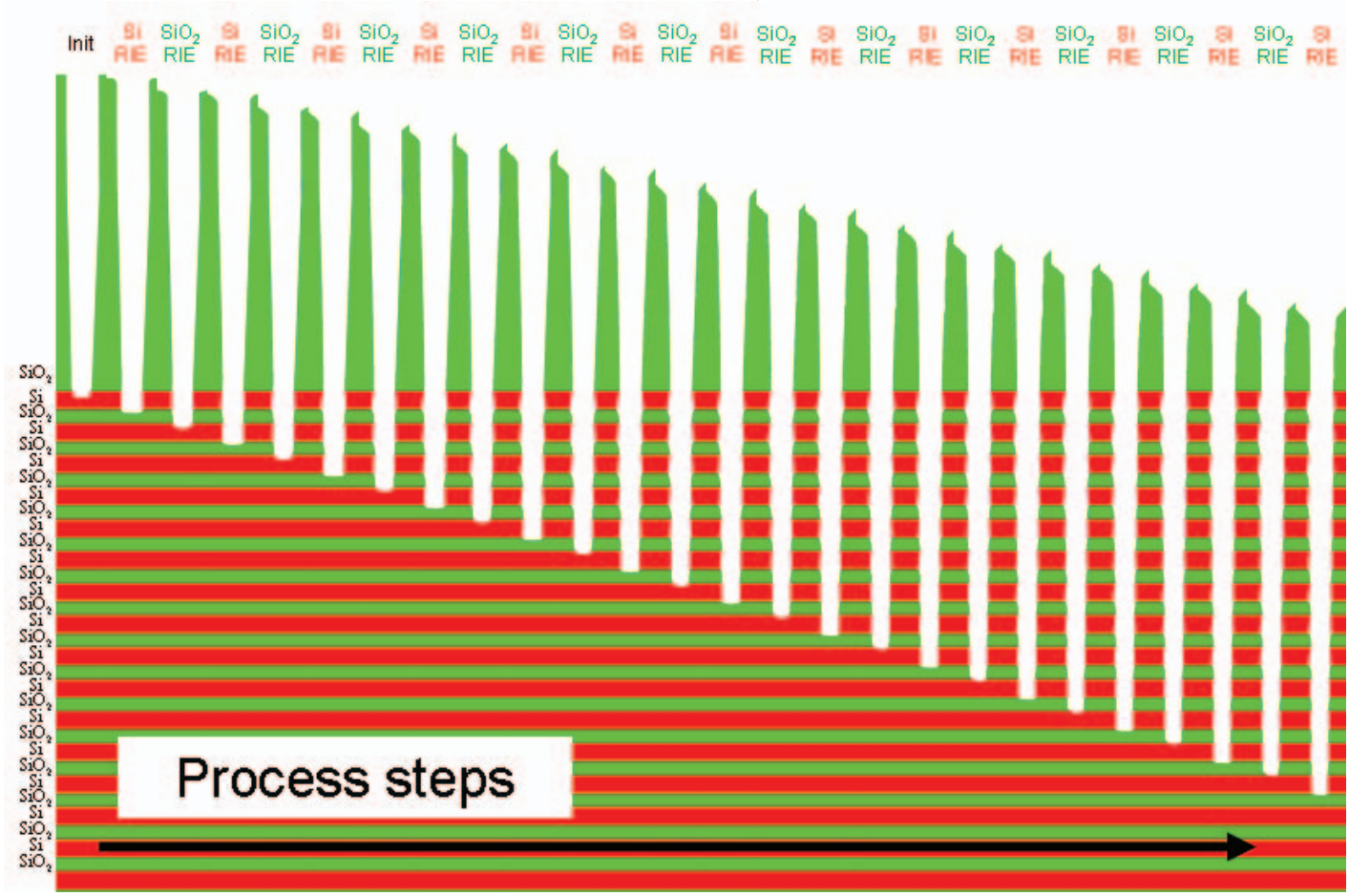

Fig.9. Topography simulation of BiCS with more stacking