2D Quantum Mechanical Simulation of Gate-Leakage Current in Double-Gate n-MOSFETs

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Abstract-The direct gate leakage current in double-gate ntype MOSFETs with physical gate lengths of 10 nm is investigated. This work uses a combination of a two-dimensional non-equilibrium Green's function (NEGF) based upon a realspace expansion method and Poisson's equation, which are solved self-consistently. In the conventional 1D analysis of the gate leakage current, an optical potential or an imaginary energy has been necessary to broaden the energy level in the triangular quantum well for reduction of computational costs. It is found that, however, different from the results in the conventional 1D analysis, peaks in the current density energy spectra, equivalently the energy levels, are broadened even under zero drain bias condition due to the quantum mechanical scatterings in the presence of the source and drain electrodes. This fact proves that the optical potential used in the conventional 1D simulation merely models the effect of the existence of the electrodes and the 2D analysis gives more sound results.

I. INTRODUCTION

As the metal-oxide-semiconductor (MOS) devices in Si LSIs are aggressively scaled down to less than 50 nanometer regime, scaling of the gate dielectric thickness has simultaneously reached as thin as a few nm. With decreasing thickness of the oxide layer, the tunneling current through the gate oxide layer increases in a nearly exponential manner. This increase in the leakage current not only detrimentally affects the MOSFET performance but also greatly increases the power consumption of the VLSIs, which should be overcome to extend further development in VLSI technologies. Thus, understanding and predicting the tunneling current at high as well as at low bias levels is quite important for the continuous development of advanced nano-scale MOS devices and meaningful TCAD applications.

The aim of this paper is to quantitatively verify gate leakage current by using a full two-dimensional (2D) non-equilibrium Green's function (NEGF) analysis with open boundary conditions at every electrode (source, drain, top-gate, and bottomgate), which can consider wave nature of electrons in the nanoscaled devices coupled with Poisson's equation.

II. SIMULATION APPROACHES AND DEVICE MODEL

In this study, we investigate gate-leakage current caused by direct tunneling through thin gate oxide in a double-gate (DG) n-type MOSFET with physical gate length of 10nm by using a 2D NEGF based upon a real-space expansion method (RSEM)[1], [2]. In the conventional 1D analyses [3], [4], although either the Quasi-Bound State (QBS) model or the NEGF was used, they had to assume a life-time or an optical potential which broadened the quantum levels in the triangular well at the SiO_2 -Si interface to reduce much computational time.

The present full 2D NEGF approach treats quantummechanically the device and each contact from which electrons can exit and impinge freely. In the popular 2D modespace expansion technique[1], [5], we have to separate the longitudinal and the transverse directions by assuming the modes in the transverse direction should be confined rigidly. We have adopted full 2D RSEM instead of the mode-space approximation since we have to allow electrons to enter and exit the source and drain, and gate electrodes, i.e. both in the longitudinal and transverse directions.



Fig. 1. Schematic structure of a symmetric DGMOSFET considered in this paper. Dashed lines show the drain and gate-leakage current path, respectively.

To model the open boundary conditions at each contact, we have used natural boundary free energies Σ_i , where *i* runs through s:source, d:drain, gt:top gate, and gb:bottom gate. The introduction of the boundary free energies is physically equivalent to the single-band scattering boundary anzatz[5], [6]. In the present full 2D NEGF is calculated as

$$G^{R}(E_{xy}) = \left[E - H_{0}^{D} - \Sigma_{d} - \Sigma_{s} - \Sigma_{gt} - \Sigma_{gb}\right]^{-1}$$
(1)

where H_0^D is the Hamiltonian matrix of the intrinsic device region. All the matrices are obtained by a finite difference model. This linear equation system is solved for each impinging energy E_{xy} and for the six degenerated conduction valleys of Si (Fig.1). The z-direction is assumed to be periodic in our model. Electron density is then given by

$$n = \frac{2}{\Delta_x \Delta_y} \sum_{k_z} \int \frac{dE_{xy}}{2\pi} \sum_i A_i f_{\rm FD}_i, \qquad (2)$$

where A_i is the spectral function, or equivalently local densityof-states in each electrode defined with the aid of the broadening function:

$$\Gamma_i = i \left(\Sigma_i - \Sigma_i^\dagger \right), \tag{4}$$

as

$$A_i = G\Gamma_i G^{\dagger}, \tag{5}$$

and Δ_x, Δ_y are the mesh spacing in the x and y direction, respectively. $f_{\text{FD}i} = f_{\text{FD}}(E, \mu_i)$ are the Fermi-Dirac distribution functions depending on the Fermi level μ_i at each electrode *i*.

Current flowing between two terminals, *e.g.* source and drain electrodes, is then given by

$$I = \frac{2e}{h} \sum_{k_z} \int dE_{xy} \operatorname{Tr} \left(\Gamma_{\rm s} G \Gamma_{\rm d} G^{\dagger} \right) \left(f_{\rm FDs} - f_{\rm FDd} \right)$$
$$= \frac{2e}{h} \sum_{k_z} \int dE_{xy} T(E_{xy}) \left(f_{\rm FDs} - f_{\rm FDd} \right) \tag{6}$$

where $T_{sd}(E_{xy})$ is the transmission coefficient which can be expressed in terms of the Green's function as

$$T_{\rm sd}(E) = {\rm Tr}[\Gamma_{\rm s}G\Gamma_{\rm d}G^{\dagger}] \tag{7}$$

These equations show that the current density between two electrodes is determined by the Green's function, the broadening functions and the Fermi-Dirac distribution functions of each electrode. Current between other terminals can be calculated by permuting the suffixes.

The structure of n-type symmetric DG-MOSFET of 10nm gate length with channel thickness $t_{\rm Si}$ of 3 nm considered in this paper is schematically shown in Fig.1. The channel is intrinsic and the source and drain electrode doping concentration is $N_D = 6.0 \times 10^{26}$ m⁻³, respectively. Parameters used here are determined by experimental data and theoretical data: gate work function $\phi = 4.25$ eV, $\chi_{\rm Si} = 4.05$ eV, $m_{\rm SiO_2} = 0.61m_0$, $m_l = 0.91m_0$ and $m_t = 0.19m_0$.

Both the potential profile and each electrode current are computed by solving the coupled Green-Poisson equations self-consistently. Self-consistency is finally achieved by iterative solution. The $I_{\rm DS}$ - $V_{\rm GS}$ and $I_{\rm GS/GD}$ - $V_{\rm GS}$ characteristics are calculated for the gate oxide thickness of 1 nm and 2 nm, respectively, for comparison. Ballistic transport is assumed and no optical potential adopted in the conventional 1D gateleakage simulation is introduced throughout the present 2D analysis.

III. RESULTS AND DISCUSSION

A. The potential profile and The carrier density distribution

Figure 2 (a) and (b) show the 3D carrier concentration profile and both the carrier concentration and conduction band profile along the center of the channel, respectively, for the oxide thickness of 1 nm. At the first sight of Fig. 2 (a), one may feel that although the donor concentration is uniformly doped



Fig. 2. (a) 3D Carrier Concentration Profile ($V_{\rm DS} = 0.5$ V, $V_{\rm gtop} = V_{\rm gbot} = 0.5$ V) for $t_{\rm ox} = 1$ nm. (b) Potential profile and carrier concentration profile along the center of the channel for each bias condition: $V_{\rm DS} = 0.5$ V, $V_{\rm gtop} = V_{\rm gbot} = 0.0/0.5$ V.

at the end of the source and drain electrodes, the electron concentration is *not* uniform along the y axis, which seems to break the charge neutrality condition in the electrodes. The charge neutrality, however, is always satisfied since the surface electron concentration *i.e.* $\int n(y)dy$ is equal to $N_{\rm D} t_{\rm Si}$, which ensures the validity of the present calculation.

For the $t_{\rm Si} = 3$ nm device, the gate potential well controls the channel potential, consequently the channel carriers as shown in the figure, since the thumb rule $L_{\rm ch} > 2 \times t_{\rm Si}$ is satisfied in this case and the short channel effects such as DIBL (drain induced barrier lowering) are suppressed. Now we have found the device behaves sufficiently well in the channel charge control. In the next section, we will study gate leakage current.

B. Gate-Leakage Current

Before proceeding to the 2D results, let us slightly review the results of the conventional 1D simulation of the gateleakage. Figure 3 (a) shows the QBS formed at the SiO₂-Si interface. Figure 3 (b) shows the transmission coefficient whose peak corresponds to each QBS in Fig. 3 (a). When the magnitude of the optical potential increases, each peak in the transmission coefficient becomes broadened and the magnitude becomes smaller. It is shown in the literature that an appropriate introduction of the optical potential can broaden each peak (Fig. 3 (b)) which enables us to reduce computational costs without any loss of accuracy in the leakage current calculation in the 1D simulation [4].



Fig. 3. (a)Quasi-bound states (QBS) at the SiO₂-Si interface. (b) Dependence of the transmission coefficient on the magnitude of the optical potential η in the 1D simulation [4]. Each peak in the transmission corresponds to the QBS in (a).

Figure 4 (a) and (b) compare the energy spectra at different drain bias of the gate-leakage current density at 300K. Each peak in each figure corresponds to the confined levels (QBSs) in each valley with different effective masses. It is found that, different from the results in the 1D analysis[3], [4], these peaks are broadened even under zero drain bias condition due to the quantum mechanical scatterings in the presence of the source and drain electrodes attached to the device region. This fact reveals that the optical potential used in the conventional 1D simulation merely models the effect of the existence of the electrodes.

With the constant gate bias voltage (V_{GS}) , the peak values



Fig. 4. Comparison of the energy spectrum of the current density at 300K: (a) $V_{\rm DS}=0$ V , $V_{\rm GS}=0.5$ V and (b) $V_{\rm DS}=0.1$ V , $V_{\rm GS}=0.5$ V , respectively.

in Fig. 4 become smaller as the drain voltage $V_{\rm DS}$ becomes higher, while higher drain voltage broadens these energy spectra. This is because confined quantum levels gradually shift along the channel due to the channel potential, in addition, the potential difference between two electrodes enhances the quantum scatterings in the channel, which results in broader line widths.

Figure 5 (a) and (b) show the energy spectra of the gateleakage current density at 77K. Drain voltage in each figure is 0 V and 0.1 V, respectively. At the low temperature, the broadening of Fermi-Dirac distribution function in the energy is so narrow that the current densities come only from the ground level of valley3-3' (unprimed ladder) which has the heavy effective masses in the confinement direction. In addition, we can clearly see that the current spectra in this level are broadened by the applied drain voltage.

Figure 6 shows the comparison of $I_{\rm DS}$ - $V_{\rm GS}$ and $I_{\rm G}$ - $V_{\rm GS}$ characteristics for different gate oxide thicknesses ($t_{\rm ox} = 1$ and 2 nm). It shows that although $t_{\rm ox}$ =1 nm suppresses the short channel effects in the drain current on/off ratio, the gate leakage increases in five orders of magnitude compared to $t_{\rm ox}$ =2 nm, which amounts several tenths of the drain off-current. The drain voltage, however, is found to have little



Fig. 5. Comparison of the energy spectrum of the current density at 77K: (a) $V_{\rm DS} = 0$ V, $V_{\rm GS} = 0.5$ V and (b) $V_{\rm DS} = 0.1$ V, $V_{\rm GS} = 0.5$ V, respectively. Current density is comprised of only valley3-3' component.

effect on the magnitude of the gate-leakage current due to channel potential profile. The current between gate and drain electrodes has turned out to be quite small and therefore the leakage current is mainly comprised of that between source and gate electrodes, which is not negligible compared with the drain off current.

IV. CONCLUSION

We have analyzed DGMOSFETs characteristics by using the full two-dimensional non-equilibrium Green's function. In the analysis we have used a real-space expansion method for mainly focusing on the gate-leakage current analysis. In the 2D simulation, different from the 1D case, the broadening of current density spectra is found to be caused by the existence of the source and the drain electrodes and the spatial potential variation by the applied drain bias. It has been understood that optical potential or life time used in the conventional 1D simulation of the leakage current is to model the broadening of the linewidth of the quasi-bound states formed in the quantum well. In the 2D simulation, such artificial parameters are no longer neccessary, which could lead more accurate simulation results. The gate currents of n-type DGMOSFETs with a single SiO₂ dielectric have been studied by the 2D real space NEGF



Gate Voltage $V_{G}[V]$

Fig. 6. $I_{\rm DS}$ - $V_{\rm GS}$ and $I_{\rm G}$ - $V_{\rm GS}$ characteristics calculated for the gate oxide thickness of 1 nm and 2 nm, respectively ($V_{\rm DS} = 0.5$ V).

method. The results show that although a device with $t_{ox} = 1$ nm shows higher performance, *i.e.* in the on-current and S value than that with 2 nm thick oxide, the gate leakage current increases as much as several tenths of the off-current, which can no longer allow further scaling in the thickness of a single SiO₂ dielectric. We have reached a stage of the introduction of the high-K gate stack structures and we can conclude that for the precise design of future nano-MOSFETs with high-K gate stacks, a full quantum 2D simulation is necessary.

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