SPICE Modeling of Self Sustained Operation (SSO) to Program Sub-90nm Floating Body Cells.

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***Abstract*— A SPICE model that predicts the Self Sustained Operation (SSO) used in programming of a Floating Body Cell (FBC) is presented. This model, which is calibrated to the contributions of the MOS, BJT and Impact Ionization (II) currents, is demonstrated to accurately predict the static and switching characteristics of the cell. Accurate modeling of device capacitances and leakages allow for quantitative estimation of static and dynamic retention of cells in an array, greatly enhancing the ability to model floating body memories.**

Keywords- Z-RAM, floating body memory, BSIMSOI, SOI, SPICE modeling.

I. INTRODUCTION

Floating Body SOI memory uses a single transistor (1T) without a capacitor, unlike traditional one transistor plus one capacitor (1T/1C) DRAM bitcells. With no additional processing steps for capacitor fabrication, they offer the simplicity of a single transistor design, and as well as 'tune-ability' for speed, low-power, and high-density (cost sensitive) applications [1]. The introduction of BJT assisted Gen. 2 operation greatly improves both data retention time and cell margin, i.e. the difference between a "1" and a "0". The small cell size and excellent retention characteristic make Gen 2 Z-RAM® a very promising DRAM alternative for sub-45nm nodes [1].

While single FBC and Floating Body Memory (FBM) arrays have been shown with full functionality [3], the ability to model these arrays has been limited. TCAD simulations of FBCs have been reported in [1],[4]. Unfortunately this approach is not feasible for simulation of large arrays and does not account for process marginalities. As multiple voltages and signal timings exist in a memory array, designing an optimal point can also be very complex [5]. These issues are further aggravated by limited understanding of various disturb mechanisms in an array and the various voltages required to address them. Therefore accurate cell models are an essential element for designing memories based on FBC. Standard SOI MOS modeling approach fails to predict the FBC behavior since it lacks accurate modeling of the parasitic BJT and associated currents, which are vital for Gen 2 operation. In this paper we demonstrate that a BSIMSOI 4.0 model calibrated for the BJT and impact ionization current is able to model the DC and programming characteristics of a FBC. Using SPICE simulations, we provide insight into the working of the FBC, while breaking down the current components at each stage of operation. We also demonstrate the use of such a model to predict the cell operating voltages.

II. FABRICATION AND MEASUREMENTS

A. Fabrication

Z-RAM cells with three different gate lengths (Lg) of 54, 70, and 90nm were fabricated using SOI wafers with 145nm BOX and 70nm SOI thickness. The width (Wg) of the cell is 54nm for all Lgs. 50nm DRAM technology was used for the device evaluation. The source/drain was formed by the ion implantation of n-type material and out diffusion from the plug poly, resulting in excellent junction leakage characteristics. TEM cross-sectional image and other process details can be found in [6]. Fig. 1 is a schematic of the floating body Z-RAM cell and the names of the nodes used in simulation.

B. Measurement

An Agilent B1500A with low capacitance femto-amp switch matrix was used for DC and capacitance characterization. Median data from multiple sites was collected for all the channel lengths at $0^{o}C$, $25^{o}C$ and $90^{o}C$ to account for variations and accurately model temperature dependence.

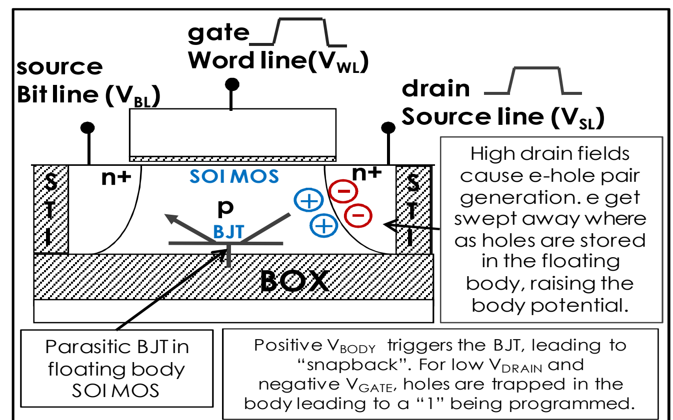

Figure 1. Schematic of a FBC, with floating body SOI, parasitic BJT (n^{+}-p-n^{+}) and the various signals used in simulations.

III. Model Calibration

A. Leakage and Parasitic BJT Modeling

Since leakage modeling is critical for static and dynamic retention, both gate induced drain leakage (GIDL) and drain field dependent junction leakage characteristics are extracted. Body Tied (BT) devices were used to model the junction leakages, GIDL characteristics, as well as the impact ionization currents (II). Fig. 2 shows the model to silicon data correlation for GIDL and MOS related II current. The parasitic BJT in the FB SOI was modeled by measuring gummel characteristics of a BT device of similar geometry and biasing the top gate in accumulation.

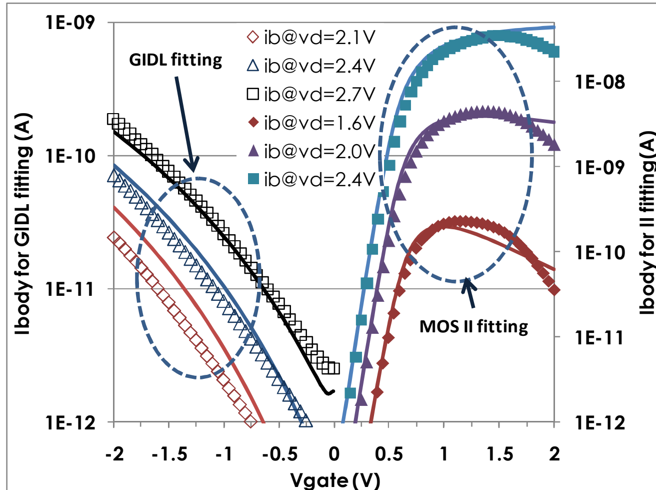

Figure 2. Modeling of GIDL and MOS generated Impact Ionization (II). Leakages determine the body potential in a FBC for Lg=90nm. (Simulation lines, measurements solid points)

In the industrial standard BSIMSOI 4.0 model [7], impact ionization current components due to MOSFET and parasitic BJT were both modeled with the same bias dependence for impact ionization rate. This approximation was quite accurate since the majority of impact ionization current in the strong inversion region is contributed by MOSFET drain current while the II current contributed by parasitic BJT was more than one order of magnitude smaller. Device simulations as well as data has shown that for smaller geometries this no longer holds true and when sub 100nm SOI MOSFET devices operate in subthreshold to accumulation regions. In such situation, parasitic BJT effect starts to dominate nodal drain current at high drain bias. Such II current has very weak dependence on Vgs in subthreshold to accumulation regions, where existing BSIMSOI 4.0 II model tends to give a strong Vgs dependence for parasitic BJT contributed impact ionization current. The drain bias dependence of parasitic BJT contributed II current is dependent on drain-base voltage (V_{DB}) rather than the voltage difference between drain and source (V_{DS}), as was the case in BSIMSOI [8]. An enhanced set of equations to predict this II current were proposed in [8] and implemented in HSPICE [9] in addition to the BSIMSOI4.0 equations. Fig. 3 describes the method to extract the parasitic BJT generated II current from a BT device. The parasitic BJT in the BT SOI FET is biased in common base configuration, while its MOS is turned off by biasing the gate in accumulation. The collector (drain) current as expected for a BJT biased in common base configuration when V_{DB} is increased is shown by a dotted line. Yet the measurements display an I_D in excess of the current that can be attributed to a BJT alone. This excess I_D is due to the II current generated by the BJT. By modeling this excess II current, we can capture this key component in modeling SSO.

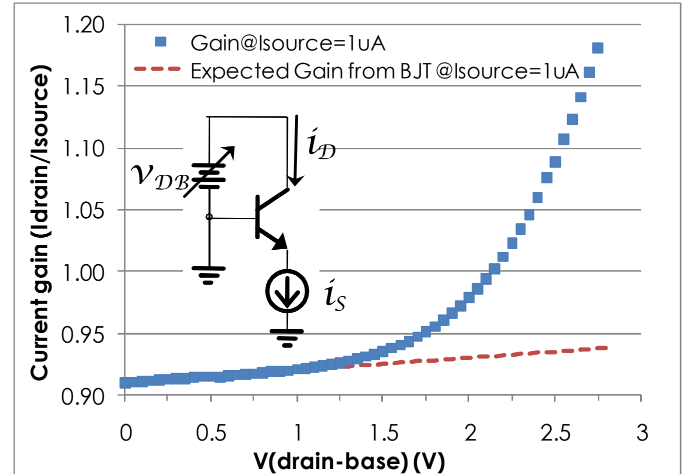

Figure 3. Measured gain of the parasitic BJT biased in common base configuration at 90ºC. The deviation (solid points) from the expected common-base characteristics results (dotted) is due to the extra II generated by the BJT.

B. MOSFET Modeling and SSO Operation

Extraction of leakages and II current were followed by the extraction of BSIMSOI parameters for MOS linear, saturation and subthreshold characteristics. I-V characteristics of MOSFET were modeled in Accelicon's Model Builder Program (MBP) to capture the body dependence of threshold voltage which is vital to cell operation (inset Fig. 4). Fig. 4 also shows the DC behavior of the FBC when the drain bias is swept while keeping the MOS in accumulation (Vg= -1.5V). As Vdrain (V_{SL}) is increased, the reverse diode leakage raises the body potential, biasing the BJT in the forward active regime.

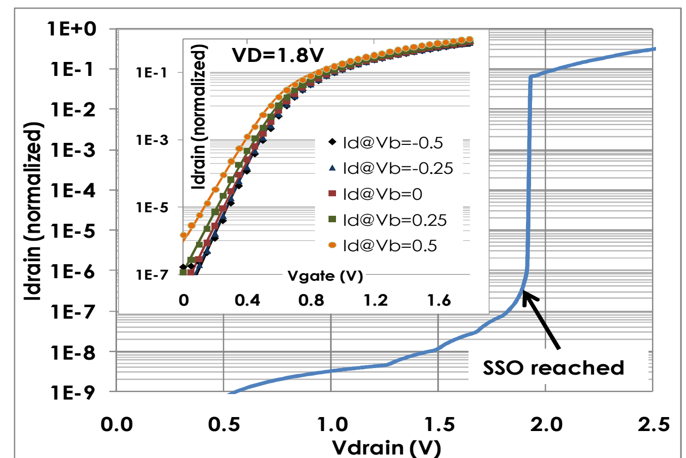

Figure 4. MOS Id-Vg fitted to data for various body biases (inset) and simulated snapback characteristics of a FBC biased at Vg=-1.5V for Lg=90nm. (Simulation lines, measurements solid points)

Further, II due to high V_{SL} creates holes that can provide the base current of the BJT. The forward biased source (emitter) junction then provides a drain (collector) current which in turns creates more holes. The BJT self-sustained operation (SSO) starts when the loop gain reaches unity. At this V_{SL}, current increases by several orders of magnitude, which is accurately predicted by the model. Fig. 5 shows junction capacitance (Cjunction), gate to channel (Cgc) and the total gate capacitance (Cgg) fitting of the Z-RAM cell. Devices with very large width but similar gate length were used for modeling, as individual cell were too small for meaningful capacitance measurements. Once the capacitances are correctly calibrated, the model can be used for predicting array operating conditions.

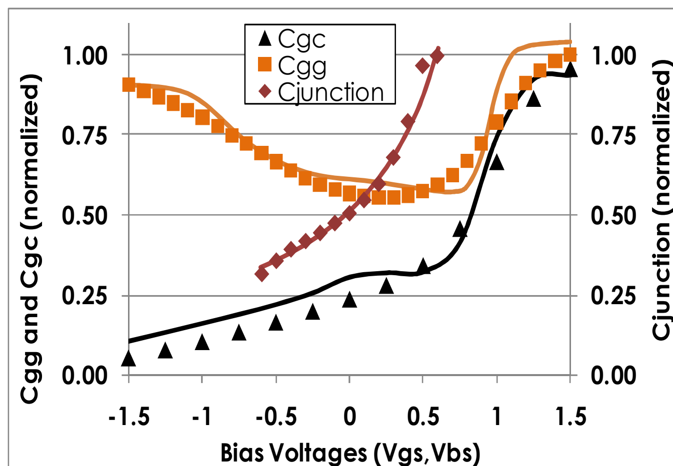

Figure 5. Capacitance fitting for Cjunction vs. Vbs , Cgg and Cgc vs. Vgs for Lg=90nm. These determine the body coupling with other nodes and the retention time of the FBC.

IV. Cell Programming

A. Cell Operation

Fig. 6 shows the operation principle and the timing diagram in terms of the simulated FB potential as write "1", read "1", write "0" and read "0" operations are performed on the cell. At write "1" operation, a combination of gate and drain pulses turns on the npn BJT. The high drain fields generate electron-hole pairs by impact ionization, and the injected electrons from drain are swept away from the body-drain junction. As a result, the cell state is changed to "1" by hole accumulation in the channel body. When "0" is written to the cell, holes are evacuated through source and drain by gate coupling. A positive voltage is applied to BL to prevent the BJT turn-on during "0" writing. When a "1" is successfully written, the FB potential raises to at least 0.4 volts versus less than -0.4 volts when a "0" is programmed. During the read cycle, the floating body holds the state of the cell. The BJT may turn on (reach SSO) or not at the read mode: if the initial body potential is high ("1" state), the BJT is triggered by drain and gate coupling. On the other hand, if the body potential is low ("0" state), there is no SSO in the BJT and the read FB voltage will not exceed 0.1V. Fig. 6 also shows the program voltages for two different V_{SL} levels. When the V_{SL} is low (1.4V), the FBC fails to reach SSO even when a "1" is written and it is no longer possible to distinguish between a "0" and "1" while reading.

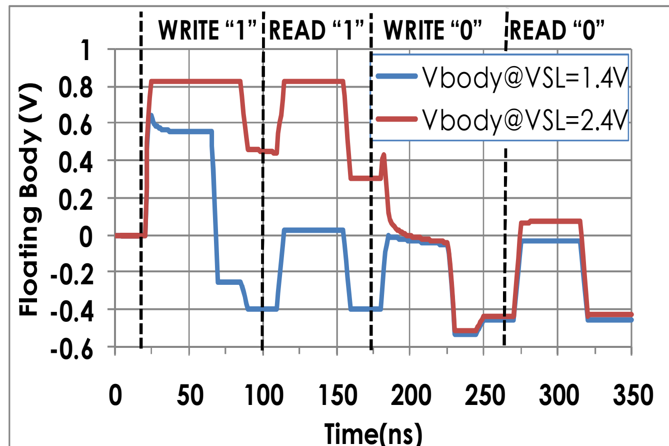

Figure 6. Cell programming simulations, showing successful memory like operation when V_{SL}=2.4V and failure of achieve SSO when V_{SL}=1.4V.

B. Cell Programing Currents.

Fig. 7 shows the relative magnitude of various current components, extracted from SPICE parameters while the FBC is programmed. During the write "1" cycle, the MOS, BJT and the BJT generated II current provide the write current, whereas just the BJT related currents exist during "1" reading. During write "0" operation, there is no SSO, as is evident by the absence of II current and lack of body charging. The gate and drain voltage pulses are the same during a read "1" and a read "0" yet during the read "0" cycles, the net current on the source line is minimal as the device no longer enters SSO. A very large current margin between read "1" and read "0" current is demonstrated. These results are consistent with measurements on FBC [6].

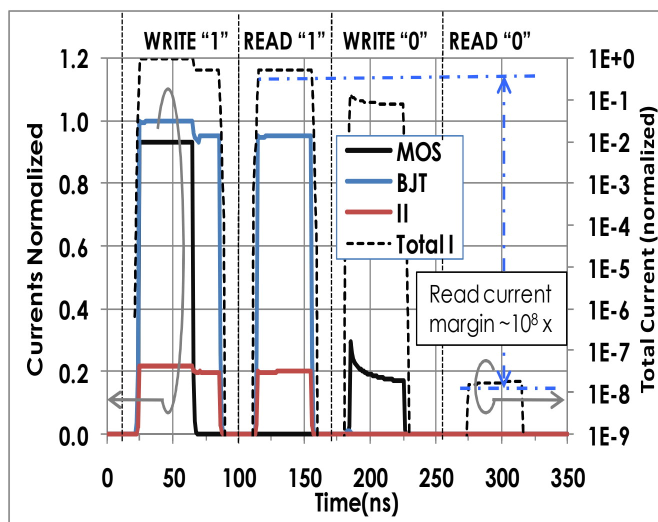

Figure 7. MOS, BJT and Impact Ionization (II) current components during programming for V_{SL}=2.4V, normalized to BJT current component.

C. WRITE V_{SL} Program Window

As Fig. 8 illustrates, using V_{SL} sweep, the model predicts the programming window of the FBC. A very high drain

voltage can cause even the “0”state to be programmed as “1”. This is because even without the gate (wordline) assisted coupling, there are excess holes generated from the high drain-body field such that the body potential rises to 0.4V or more after the “0” write. On the other hand, if VSL is below 1.9V, the BJT fails to reach SSO even with the gate assisting the body to couple up during write “1”. Through the use of the calibrated model, arrays may be designed to meet the program conditions for write “1” and “0” under all circuit operations.

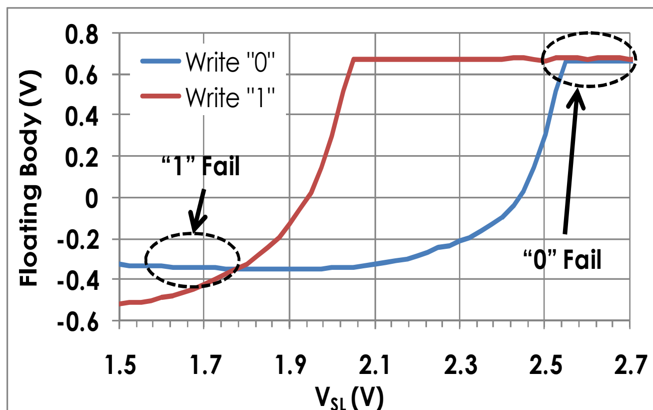

Figure 8. V_{SL} programming window simulations for “0” and “1”.

D. READ V_{WL} Program Window

Similar to the V_{SL} write program window, the SPICE model allows us to correctly predict the Vgate (wordline) read operating window (Fig. 9). The wordline coupling used in [1] allows for a lower V_{SL} as the final floating body is assisted by wordline swing. But this design also places a constraint on the swing that can be applied on the gate to read a programmed cell. One way to ascertain the state of the cell is to monitor the current on the bitline (source) during a read operation (Fig. 7). A high wordline swing can couple up the base potential of the parasitic BJT, unintentionally forcing it into SSO while reading.

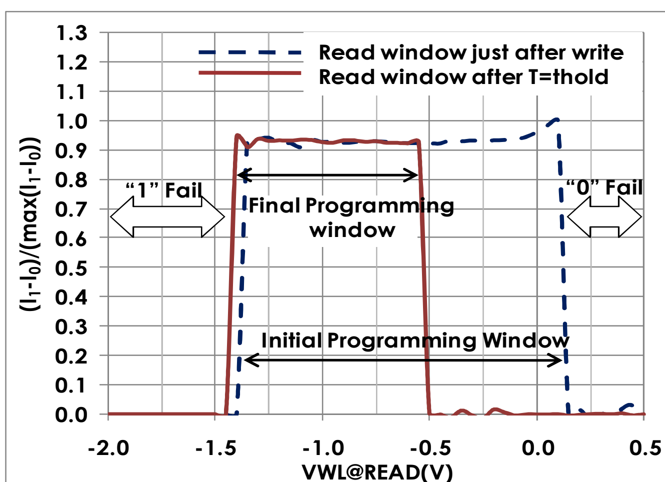

Figure 9. The read current difference just after WRITE (dotted) and after holding (solid) as a function of WL read voltage at 90ºC.

This is indicated by “0” fail. Likewise, if the V_{wl} swing is small, there is minimal WL coupling to assist the floating body, and a “1” state can no longer be successfully read. Fig. 9 also shows the evolution of the WL read window over cell’s retention time. Junction leakage current can charge up the floating body in the “0” state, resulting in a smaller swing WL so that “1” and “0” can still be distinguished.

V. Conclusion

We have demonstrated modeling of SSO in a FBC using standard SPICE models by accurately modeling the MOS, the parasitic BJT, II and leakage currents. Such a model can be used for predicting the behavior of a large array as well as for optimizing cell operation. The model accurately predicts operating windows for WRITE and READ operations and would thus help to ensure margins in signaling while designing large arrays.

Acknowledgment

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