Integrated Stress and Process Calibration in Strained-Si Devices

T-H Yu, K-C Tu, Y-M Sheu, and C. H. Diaz
Taiwan Semiconductor Manufacturing Company (TSMC), R&D
Hsinchu, Taiwan R.O.C.
e-mail: thyub@tsmc.com

***Abstract*—We present a novel calibration methodology that (i) integrates dopant diffusion, mechanical strain and bandgap narrowing for accurate device short channel effect modeling and (ii) deploys stress dependent mobility model for robust device performance projection especially on effective drive current (Ideff). Good agreement is obtained between the model calibration and experimental measurements over the full gate length range examined. Moreover, a general mobility gain with respect to uniaxial stress is presented.**

Keywords e-SiGe; strined-si; band gap narrowing; mobility; calibration

I. INTRODUCTION

With the adoption of key stressor components: embedded SiGe source/drain (e-SiGe) and capping layer (CL) in CMOS architecture, modelling of process induced stress and associated stress induced bandgap narrowing and mobility enhancement has become increasingly important for scaling devices. Though several researchers have derived strain-induced mobility gain from either theoretical band structure calculation [1-2] or wafer bending approach [3], to the authors' knowledge this is the first simulation model that includes both strain-induced bandgap narrowing and mobility enhancement within the framework of doping and stress profile calibration together.

In this paper, we present a combined dopant diffusion and stress tensor simulation approach to model strain effects in sub-nanometer MOSFETs. For the first time, a model that combines both strain induced bandgap narrowing and mobility enhancement is shown to accurately reflect silicon measurements. In this work, the major stressors including e-SiGe and CL are decoupled to identify each component's contribution. Good agreement in electrostatics such as threshold voltage roll-off due to bandgap narrowing and strain-induced Ion gain is obtained between model calibration and experiments over the full gate length range examined. Ideff is a figure of merit of gate delay, which is defined as Ieff=(Id_low+Id_high)/2, where Id=Id_low at Vd=Vdd& Vg=Vdd/2, Id=Id_high at Vd=Vdd/2& Vg=Vdd. The model further predicts Ideff performance and obtains excellent agreement with each stressor measurement, which also validate our strain-induced mobility model implementation.

II. CALIBRATION METHODOLOGY

In this work, the calibration consists of three major components: process, stress, and device calibrations. Dopant diffusion and stress tensor simulations are performed simultaneously in Tsuprem4 and then the stress and doping profiles are fed into Sdevice to obtain electrostatics. For the process calibration, the doing profile is well characterized through SIMS calibration and also has been validated through electrical characteristics. The stress accounts for process induced mechanical stress including major stressors: capping layer, embedded SiGe S/D, and Shallow Trench Isolation (STI). To calibrate the experiments precisely, we designed two categories of experimental samples using 65nm high performance technology. One is without process induced strain and is our calibration reference. Another one is with the stressors. For two strained NMOS samples CL1 & CL2, both have a tensile film and sample CL2 is 1.8X thicker than that in sample CL1. For strained PMOS cases, we decouple stressor effects into compressive CL only, e-SiGe only, and with both compressive CL and e-SiGe. Since calibrated devices utilized in this work have larger active region size, the channel stress can be treated from major stressors and the contribution from STI can be ignored. For the unstrained cases, first we calibrate unstrained transistors including dopant diffusion and electrostatic characteristics. For the strained cases, add stress related models described in next section into strained MOSFETs to simulate the process induced mechanical stress. Electrical characteristics then can be calibrated by adjusting strain-induced mobility parameters while stress-independent mobility parameters obtained from unstrained calibration keeps unchanged.

III. MODEL IMPLEMENTATION

The viscoelastic mechanical model utilized in the process induced mechanical stress simulation consists of volumetric and shear components. The force balance equation can be combined with the viscoelastic flow equation to solve flow velocities. The stress sources included in the analysis are intrinsic film stress, thermal mismatch, oxidation, and lattice constant mismatch. Strain models employed in the device simulation include deformation potential bandgap model [4], piezoresistive electron mobility and six-band **k•p** hole

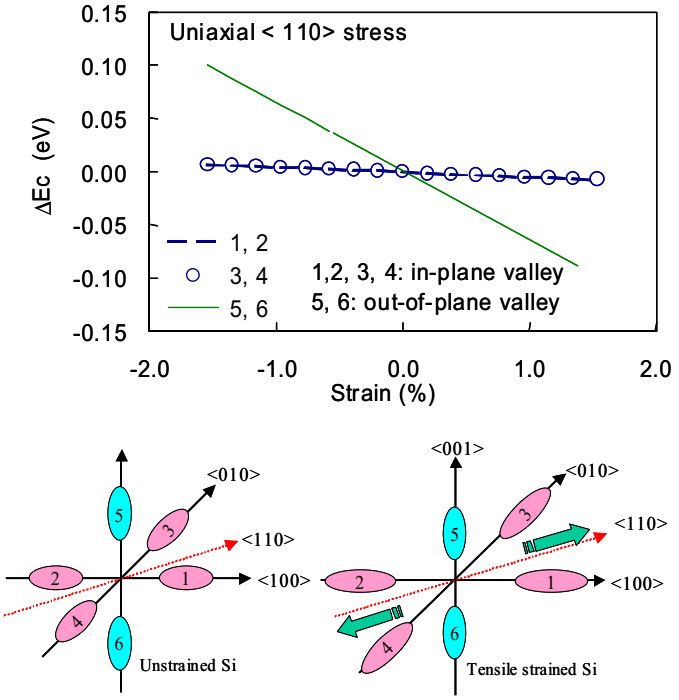

Figure 1. Sub-valley energy splitting of conduction band edge as a function uniaxial <110> strain

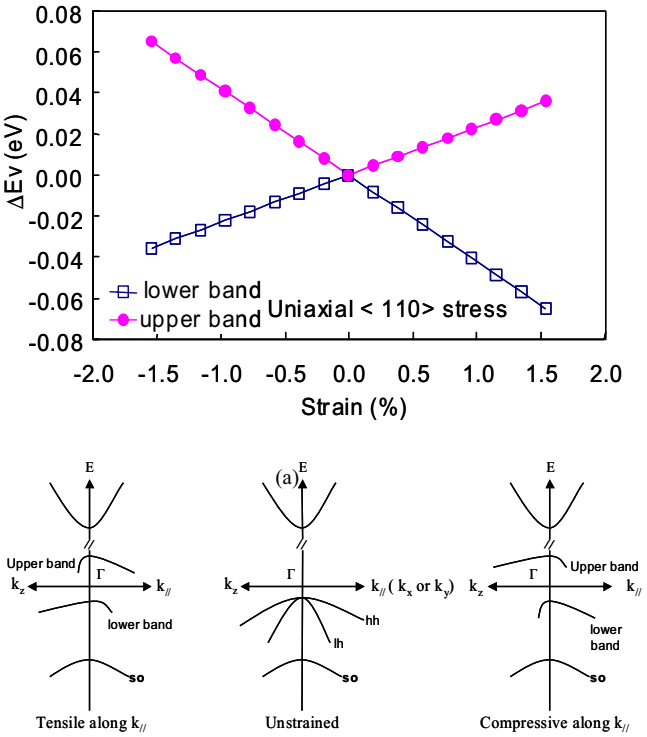

Figure 2. (a)Sub-valley energy splitting of valence band edge as a function uniaxial <110> strain (b)Stain effect on the valance band splitting & band gap energy reduction (c)Valance band constructed from P_x orbital

mobility models [5]. The crystal symmetry and lattice spacing will be altered by mechanical stress. Hence the mechanical stress moves the band edge. This is expressed in terms of deformation potentials. We adopt it to model the stress-induced band gap narrowing and to calculate each subband valley change from the formula derived by Pikus and Bir [4]. Piezoresistive mobility model is used in strain-induced electron mobility gain calibration. The piezoresistive coefficients, function of doping concentration and temperature, are utilized to fit measurements. For strain-induced hole mobility model, a physical-based model incorporated with doping dependent and carrier redistribution between subvalleys is used in the simulation [5].

IV. Simulation Results

Under uniaxial stress, the symmetry of the band edge is broken and the asymmetry results in a redistribution of carriers in k-space. Fig. 1 shows sub-valley splitting in conduction band edge under uniaxial <110> strain. Under tensile stress, carriers will be redistributed into lower energy subvalleys 5&6, where the effective mass is reduced along <110> channel direction due to band warped [6]. Also as the strain increases, the band splitting increases leading to a reduction of inter-valley scattering. The influence of uniaxial strain on valence band edge shift is shown in fig. 2(a). Fig. 2(b) shows that strain has more dramatic effects on the degenerate valence bands near Γ. The degeneracy of heavy and light hole bands at Γ point are broken and the meaning of "heavy" and "light" becomes ambiguous in strained silicon. Instead upper and lower bands proposed by Bir and Pikus [4] denote the band splitting, which will alter their coupling and effective mass significantly. To give a physical picture, a simplified valence band model constructed by the symmetric Px, Py, and Pz orbitals are used to explain the band splitting and energy raised-up [7]. First we analyze the hole transfer in Px orbital shown in Fig. 2(c). Under uniaxial compressive stress, Px orbital is squeezed toward the center which causes an increase of orbital overlap. This makes it easy for hole transfer along x-direction so that the effective mass is low. However, the coupling is quite weak between Px and Pz, the hole transfer to Pz becomes difficult and hence the effective mass is heavy. Consequently, as can be seen in Fig. 2(b), Px hole effective mass becomes light along x-y plane and heavy along z-direction. Also the overlap increases along x-direction so that the orbital energy is raised-up and close to conduction band minimum. Similar analysis for Pz hole, under tensile stress, Pz hole along z-direction becomes light and becomes heavy along x-y plane.

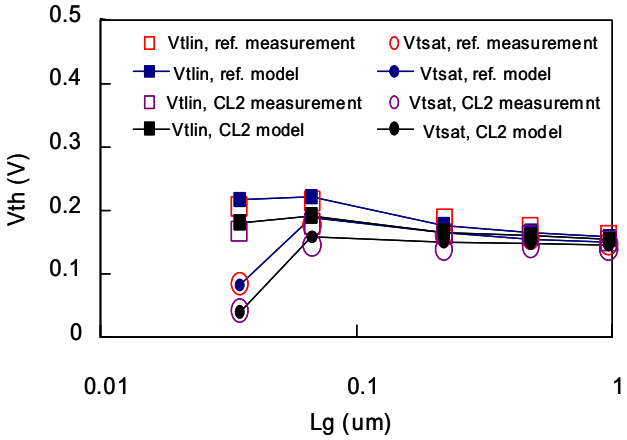

Figure 3. Strain-induced bandgap narrowing causes Vth roll-off in NMOS. The only difference between Ref and CL2 is the capping layer stress. Ref and CL2 are with neutral and tensile capping layers, respectively.

Under uniaxial <110> tensile strain, the conduction band edge of valleys 5&6 are pulled down and the hole band with heavy effective mass is raised up so that the band gap energy is reduced. Due to the band gap narrowing, the intrinsic carrier concentration is increased, which results in surface potential drop and depletion charge reduction. These factors lead to a reduction of threshold voltage. Fig. 3 shows the NMOS threshold voltage shift due to strain-induced bandgap narrowing. The only difference between these two samples is the capping layer stress. One is with neutral CL and another is with tensile film. The impact of e-SiGe effect on Vth shift is shown in fig. 4. Simulation results show good agreement in Vth between model calibration and experiments over the fully examined gate length when applying both dopant diffusion and stress tensors together in the calibration. The impact of CL effect on NFET Ion gain mainly from effective mass and inter-valley scattering reduction is shown in fig. 5. A further increasing in CL thickness obtains 3% Ion gain. As can be seen in fig. 6, e-SiGe in PFET significantly improves Ion due to hole effective mass reduction substantially. To obtain a general formula of mobility gain with respect to uniaxial strain, we

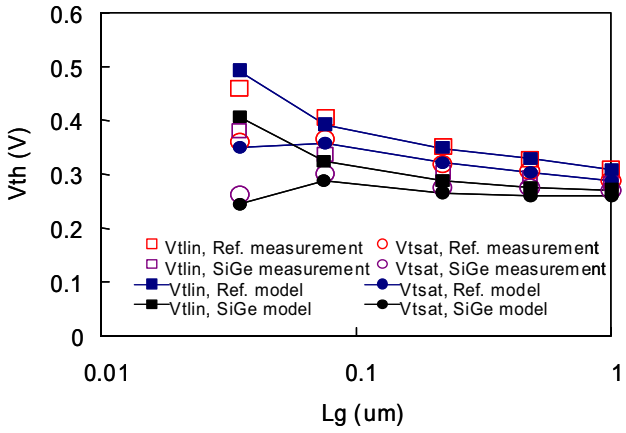

Figure 4. Simulation models include dopant diffusion and stress tensors and obtain good match with experiments in PMOS threshold voltage. Ref and SiGe denote without and with e-SiGe, respectively.

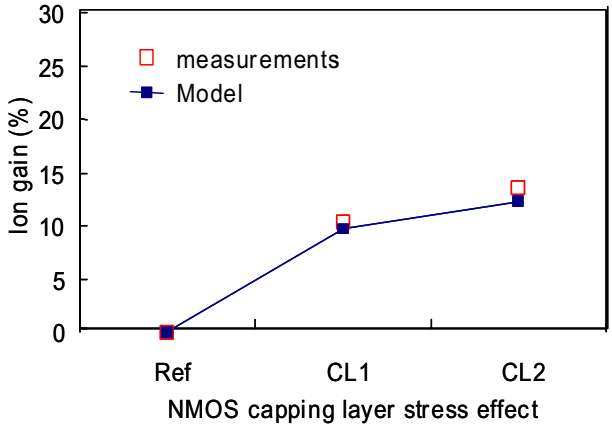

Figure 5. NMOS capping layer stress effect on Ion performance. Ref is a reference with neutral stress in capping layer. CL1 and CL2 are with tensile film but CL2 is 1.8x thicker than that in CL1.

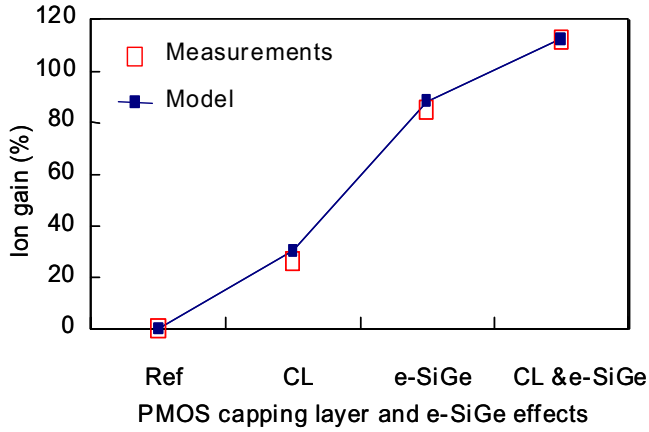

Figure 6. PMOS Ion gain with various stressors: compressive capping layer(CL), e-SiGe, and with both e-SiGe and compressive CL. Ref is a reference with unstrained capping layer and without e-SiGe.

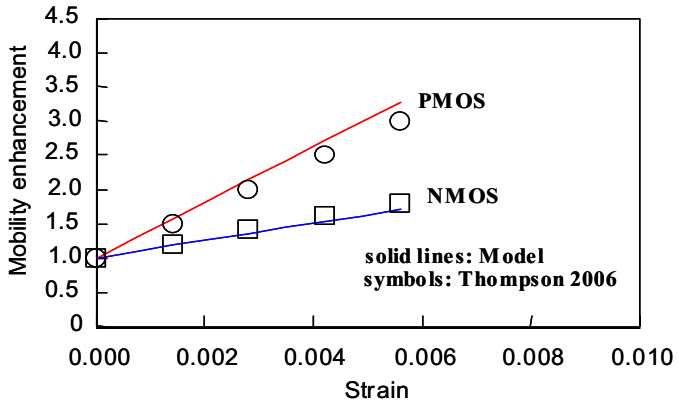

Figure 7. mobility enhancement as a function of uniaxial strain. The enhancement factor is calibrated with experiments.

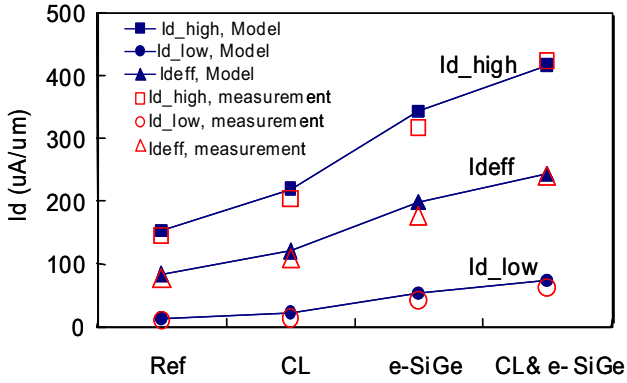

Figure 8. PMOS stress effect on Ideff. Good agreement between model prediction and experiments. Ideff shows strongly correlated to linear condition current, Id_high, depending on mobility enhancement.

apply a uniform uniaxial stress into the channel region with the calibrated strain-induced mobility parameters. Therefore the carrier mobility enhancement as shown in Fig. 7 is obtained. A similar behavior was observed from wafer bending experiments by Thompson [3]. In addition, the channel piezoresistive coefficients can be further extracted from the strain induced mobility gain. Moreover, Ideff, a transistor delay behavior index, is investigated in PMOS. Model prediction is quite well including Ideff, Id_high, and Id_low for all examined cases as shown in fig. 8. The magnitude of strain-induced Ideff gain is strongly correlated to Idlin gain, which indicates low-filed mobility improvement will increase Ideff considerably.

V. CONCLUSION

In this article, we have presented a novel calibration methodology to obtain accurate modelling of short channel effect and drive current performance on strained devices. The calibration methodology employed in this work combines dopant diffusion, strain tensor, and device calibration together. A model that combines strain induced bandgap narrowing and mobility enhancement is presented to reflect threshold voltage shift and drive current gain due to strain. Model obtains good agreement with measurements in terms of electrostatics, Ion gain, and Ideff from unstrained to strained MOSFETs. A general strain related mobility gain can be further derived from model prediction.

REFERENCES

[1] M. V. Fischetti, F. Gamiz, and W. Hansch, "On the enhanced electron mobility in strained-silicon inversion layers," J. Appl. Phys., vol. 92, pp. 7320-7324, Dec. 2002.

[2] M. V. Fischetti, Z Ren, P.M. Solomon, M. Yang, and K. Rim, "Six-band kp calculation of the hole mobility in silicon inversion layers: dependence on surface orientation, strain, and silicon thickness," J. Appl. Phys., vol. 94, pp. 1079-1095, Feb. 2003.

[3] S.E. Thompson, S. Suthram, Y. Sun, Gsun, S. Parthasarathy, M. Chu, and T. NIshida, "Futhure of strained si/semiconductors in nanoscale MOSFETs," IEDM Tech, Digest, 2006.

[4] G.L. Bir and G.E. Pikus, Symmetry and Strain-induced Effects in Semiconductors, John Wiley & Sons, 1974..

[5] Sentaurus Device User Guide, 2006.

[6] K. Uchida, t. Krishnamohan, K. C. Saraswat, and Y. Nishi, "Physical mechanisms of elecron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime," IEDM Tech, Digest, 2005.

[7] J. H. Davies, The physics of low-dimensional semiconductors, Cambridge university press, 1998.