Simulation of Layout-Dependent STI Stress and Its Impact on Circuit Performance

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***Abstract*—The impact of STI stress with layout dependency on circuit performance is investigated. A 3D stress simulator has been developed using finite element method, which considers both the layout design and process information (PDK). The mobility change due to stress is included in the transistor modeling for circuit simulation. The circuit performance can thus be analyzed with nonlocal stress. As a test case, a buffered SR flip-flop was simulated with and without STI stress considered. It can be seen that STI stress has non-negligible influence on the circuit performance.**

I. Introduction

Various stress engineering techniques have been introduced to improve the device performance as the scaling down of CMOS devices continues. However, stresses can also generate in the device channels during the fabrication process. Shallow trench isolation (STI) is one of the major sources of such stress-inducing mechanisms, the magnitude of STI stress depends on the layout pattern [1]. The performance of a transistor is therefor related to its surrounding layout, and is the performance of an entire circuit.

Efforts have been made to model the layout-dependent stress and to exploit the possibility of managing it as a performance enhancing technique [2]–[5]. Almost all these works were based on 1D layout parameters or pseudo-2D, "ideal" MOSFETs with rectangular or piecewise-rectangular active regions were assumed in these studies. The effects of neighboring devices were also not fully incorporated. However, such simplified model is different from the practical situations. As shown in Fig.4, even the layout of a simple standard cell contains complex neighboring polygon regions. As the layout is essentially two-dimensional, detailed analysis of STI stress should take into account 2D in-plane effects rather than 1D effects only. Therefore, taking into account the thickness direction, three-dimensional simulations must be conducted to show the stress distribution correctly in numerical analysis. Elaborated TCAD simulators have been developed to perform the simulations for stress introduced by different technology processes. Unfortunately, as limited by the amount of memory and computational power available, currently such TCAD tools can only be applied directly in the simulations for layouts containing no more than a couple of transistors. To perform numerical simulations for the stress profiles of larger cells, certain simplification together with appropriate methodology must be introduced to accelerate the simulation process. New simulation tools should be developed to enable the simulation of larger scale circuits.

In this work, a 3D parallel finite element simulator capable of the simulations of larger circuits containing dozens of transistors was developed to evaluate the layout-dependent stress. Comparisons between simulated result obtained from our program and experimental measurement were made. The effects of layout-dependent stress on the performance of an SR flip-flop standard cell are analyzed as an example. Circuit simulations were performed with or without the layout-dependent stress effect for circuit parameters to investigate the impact of STI stress.

II. Simulation Approach

For the STI process, the major stress sources and effects include thermal mismatch, intrinsic stress, growth of materials and viscoelasticity. The thermal mismatch stress is resulted from the difference of thermal expansion properties between different materials such as silicon and silicon dioxide, it can be calculated from the temperature change and thermal expansion coefficients; Thin films such as nitride film are generally highly stressed and thus have important effect on the overall stress distribution, an initial stress is included to model this effect; Volume expands during the oxidation process for oxide liner in the STI process, thus additional mechanical stress accumulates. This effect also contributes its part to the initial strain of the liner layer; Some materials, for example, nitride and silicon dioxide as concerned in our study, exhibits noticeable viscoelasticity at higher temperature and can not be neglected, a relaxation process is applied in reference to temperature change for simplification. Beside all these stress-inducing mechanisms, an additional initial stress is also introduced as calibration to model a practical fabrication technology.

The stress profile is solved using finite element method (FEM). As the direct solution of the whole system is inapplicable due to the large size of mesh, the problem is partitioned into smaller sub-regions and solved iteratively, which naturally enables parallel computing.

Piezoresistance model was employed to calculate the influence of stress on mobility since it is effective for small stress and can give the enhancement factor directly [6]. Model

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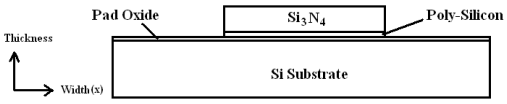

Fig. 1. Schematical structure of the test sample [8]. Width of the nitride/poly-Si is 9.4μm.

parameters presented in [7] were used. The mobility value for every transistor is then calculated from stress tensors and passed to a circuit simulator, then the circuit performance can be obtained from circuit simulations.

III. Results and Discussions

A simulation program was developed to implement the approach introduced previously. The simulation program consists of two components: the layout analyzer and the finite element simulator. In the layout analyzer, a modified scanning line algorithm was employed to process the layout geometries and extract the gate region for each transistor, then the whole layout was partitioned into smaller "effective regions" for FEM analysis. In the finite element simulator, first order Manhattan bricks were used for 3D meshing. The distribution and size of the elements were controlled along different directions separately to generate high quality meshes. In the solving phase, the resulting linear equations were solved using Generalized Minimal Residual Method (GMRES).

As a validation of our simulation approach, A test structure was simulated first to give a comparison between the simulation result of our program and experimental measurement. After the comparison, a buffered SR flip-flop standard cell was simulated to evaluate the impact of STI stress on the performance of practical circuits.

A. Comparisons

Micro-Raman spectroscopy was applied to determine mechanical stress in devices and structures used in microelectronics in [8]. One of the samples measured was shown in Fig.1. A 10-nm-thick pad oxide is grown on (001) silicon wafers by dry oxidation at 900°C. This is followed by deposition of 50 nm poly-amorphous silicon with intrinsic stress of -0.3GPa. Next a low-pressure chemical vapor deposition (LPCVD) silicon nitride film with intrinsic stress of 1.2GPa is deposited and photolithographically patterned into long [-110]-oriented nitride/poly-Si lines. The thickness of the nitride film is 240 nm. The width of the nitride/poly-Si is 9.4μm.

The same structure was simulated using our program and the stress profile was obtained. Fig.2 shows the stress component σ_{xx} in silicon near and beneath the upper silicon surface obtained from the simulation, together with the experimental measurements reported in [8]. Although slight differences are shown near the boundaries of the nitride/poly-Si line, good overall agreement is shown between the simulation result and the measurement result.

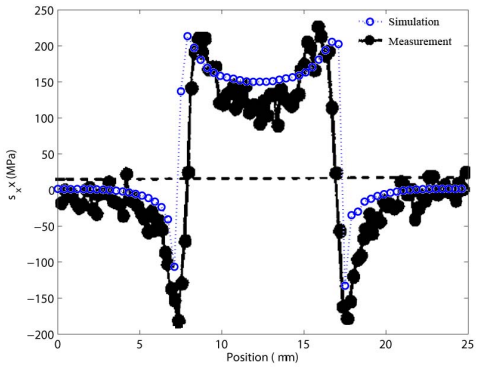

Fig. 2. Comparison between experimental measurements result from [8] and simulation results of σ_{xx} using our program for the same structure shown in Fig.1.

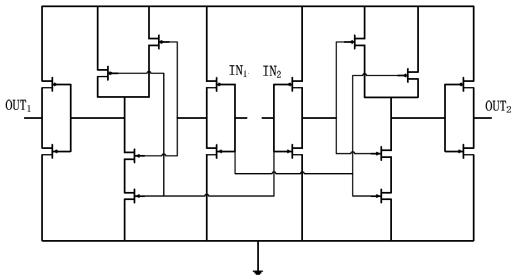

Fig. 3. Schematic of the buffered SR flip-flop.

B. Simulation Results

To apply our simulation approach to practical circuit, a 0.18μm buffered SR flip-flop standard cell with minimum size was simulated. The schematic of the circuit is shown in Fig.3. Its layout is given in Fig.4 with only some layers shown. The stress simulation was performed first to obtain the layout-dependent stress profile for each transistor. The corresponding degrees of freedom for the entire layout is 4,643,856. Fig.5 gives the in-plane result of stress tensor component σ_{xx} near the upper surface of silicon, across the

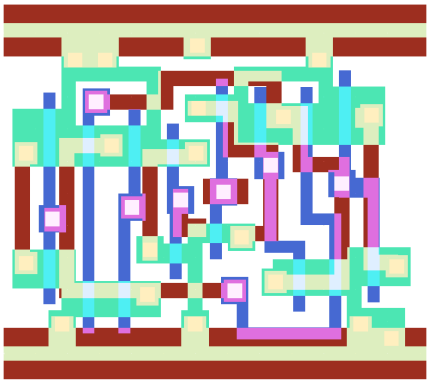

Fig. 4. Layout of the buffered SR flip-flop with active layer, poly-Si layer and one metal layer included.

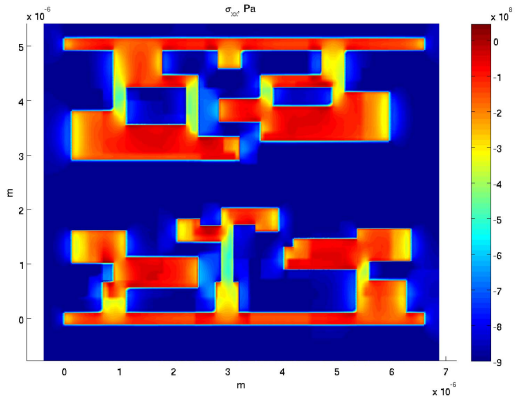

Fig. 5. In-plane Stress profile of σ_{xx} corresponding to the layout near the silicon surface.

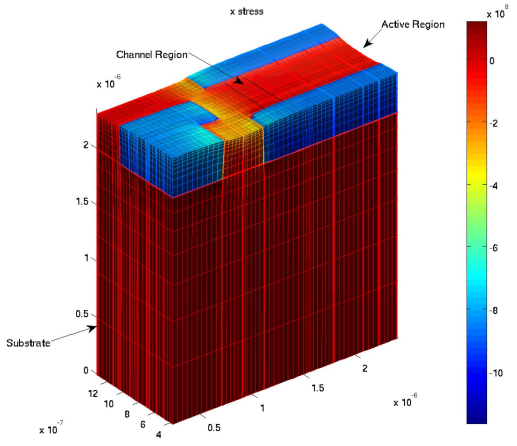

Fig. 6. 3-D stress profile of σ_{xx} for a sub-region of the whole circuit, with the nitride and oxide layer removed and meshes shown.

whole layout region. The magnitudes of σ_{xx} are depicted by different colors. The effects of different active region shapes on stress distribution can be seen in the visualization of stress distribution. It is shown obviously that narrower active regions result higher stress and wider active regions introduce smaller stress changes. Meanwhile, the stress profiles near corners of active region exhibit clear nonuniform 2D distributions, such distributions can not be predicted in 2D simulations.

Fig.6 illustrates the 3-D result of one sub region, surface colors correspond to the magnitudes of σ_{xx} as well. The meshes are deformed exaggeratedly in reference of the nodal displacements to give a better view. The transition of color on the top surface indicates obvious 2D in-plane variation of stress.

As the stress value differs along the width direction for each MOSFET, but only one scalar mobility value can be accepted by the device model, an integration operation was performed along the central line in width direction for each MOSFET to give the average stress values. This value was then passed to the piezoresistance mobility model and the mobility value was calculated for each transistor.

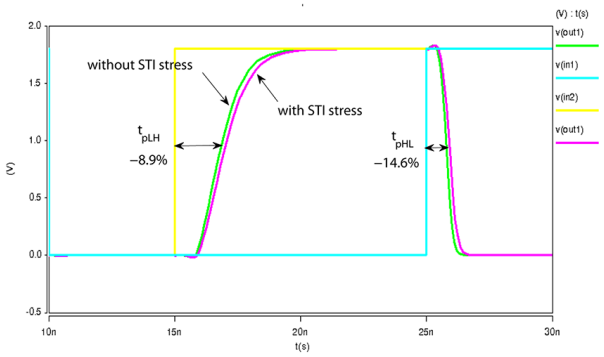

Fig. 7. Timing parameters of the SR flip-flop with or without STI stress effect.

With these new mobility values containing the influence of layout-dependent stress, circuit simulations can be performed to show the changes of circuit properties. The simulation tool HSPICE was used for these simulations. Performance parameters, including rise time t_r, fall time t_f and propagation delays t_{pHL}, t_{pLH} were obtained from the simulations. While the rise time t_r increased from 1.899ns without the layout-dependent stress effect to 2.069ns with the layout-dependent stress effect, fall time t_f increased from 0.483ns to 0.587ns. Parameters t_{pHL} and t_{pLH} are shown in Fig.7, with or without the STI stress. A 8.9% increase of t_{pLH} and a 14.6% increase of t_{pHL} were observed in circuit simulations due to the inclusion of STI stress, as shown in Fig.7. These simulation results indicate that the layout dependent stress has noticeable impacts on the device properties and thus the performance of the whole circuits.

IV. Conclusion

A numerical simulation program has been developed for 3D stress analysis. This program was applied in the analysis of practical devices. Comparisons between the simulation result and experimental measurement of stress distribution validated the accuracy of the simulation program. Simulation for the impact of layout-dependent stress on circuit performance was conducted using an SR flip-flop design. It is concluded that the global stress has non-negligible effects on circuit performance. Our program provides a good simulation tool for quantitative evaluation of the layout-dependent STI stress and its impact on circuit performance.

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