Simulation on NBTI degradation due to discrete interface traps considering local mobility model and its statistical effects

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***Abstract*—Mobility degradation due to the interface trap generated by the NBTI stress is simulated considering the discrete nature of the interface trap. We evaluate the relationship between threshold voltage shift (ΔV_{th}) and drain current degradation (ΔI_D) including the mobility degradation due to the traps. The results can be used, for example, to predict ΔV_{th} in the On-the-fly NBTI measurement. Moreover, the statistical modeling for the degradation of I_D due to the spatial distribution of the interface trap is investigated.**

***Index Terms*—Reliability modeling, NBTI, drain current degradation, mobility degradation, discrete trap**

I. Introduction

The measurement delay during the NBTI stress gives an unwanted recovery effect to make the interpretation of the results obscure. To overcome this recovery effect, the On-the-fly (OTF) measurement [1] has been proposed in which the gate stress is maintained while measuring I_D instead of sweeping the gate voltage to obtain ΔV_{th}. However, the OTF measurement has a disadvantage in which additional calculation is required to extract ΔV_{th} for the measured ΔI_D based on a MOSFET device model [2], [3].

In the OTF method, the incorporation of mobility degradation becomes an important issue in extracting correct ΔV_{th} [2], [3]. The measurement strategy proposed in [2] may results in wrong estimation of the mobility degradation since the discrepancy between devices for the mobility extraction measurement and OTF becomes larger as the device size shrinks due to the spatial distribution. In addition, the method using the BSIM model [3] cannot predict ΔI_D and ΔV_{th} deviation in a statistical manner.

In this paper, we propose an NBTI simulation strategy from generating the discrete interface charge to predicting the current degradation due to the mobility degradation in addition to the Poisson effect. We evaluate the mobility degradation due to the discrete interface traps using a local potential variation model [4], [5]. It will be shown that the modeling strategy gives not only a basis for correct interpretation of the OTF measurements but also the statistical distribution of ΔI_D and ΔV_{th} which becomes more important as the device size becomes smaller.

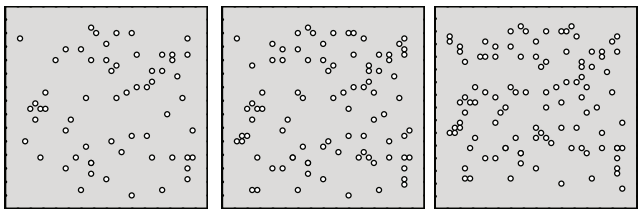

Fig. 1. Spatial distribution of interface trap under NBTI stress. Device size is 140nm × 140nm and the stress time is 11s, 50s and 150s from the left to right respectively.

II. Generation of discrete trap

The 2D profile of the discrete interface traps generated by the NBTI stress is extracted from the modifications of the triple well model (TWM) [6]. The TWM describes the energy distribution of discrete Si-H bonds which act as trap sites. With an input parameter N as the total number of Si-H bonds, 2D coordinate for each Si-H bond is given and placed a specific location at the interface. For each discrete Si-H bond, the well-to-well transition probabilities of a hydrogen particle during Δt are

$$k_{13} = \nu \exp(-1/k_{\mathrm{B}}T(V_2 - V_1 - \Delta_2))\Delta t \text{ (well 1 to 2)} \quad (1)$$

for a hydrogen particle in the well 1,

$$k_{31} = \nu \exp(-1/k_{\mathrm{B}}T(V_2 - V_3 - \Delta_2))\Delta t \text{ (well 2 to 1)} \quad (2)$$
$$k_{35} = \nu \exp(-1/k_{\mathrm{B}}T(V_4 - V_3 - \Delta_4))\Delta t \text{ (well 2 to 3)} \quad (3)$$

for a hydrogen particle in the well 2 and

$$k_{53} = \nu \exp(-1/k_{\mathrm{B}}T(V_4 - V_5 - \Delta_4))\Delta t \text{ (well 3 to 2)} \quad (4)$$

for a hydrogen particle in the well 3 where ν is a constant, V_1, V_2, V_3, V_4, V_5 represent the well energy configuration in [6]. V_1 represents an energy of well 1 (Si-H bonding state), V_3

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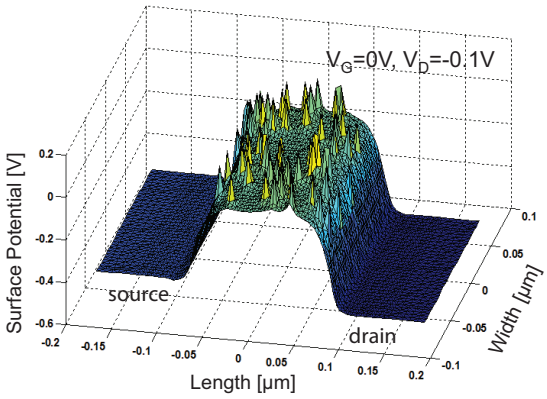

Fig. 2. 3D potential profile from the simulation. Potential barriers are created by the trap sites, which disturb the current path.

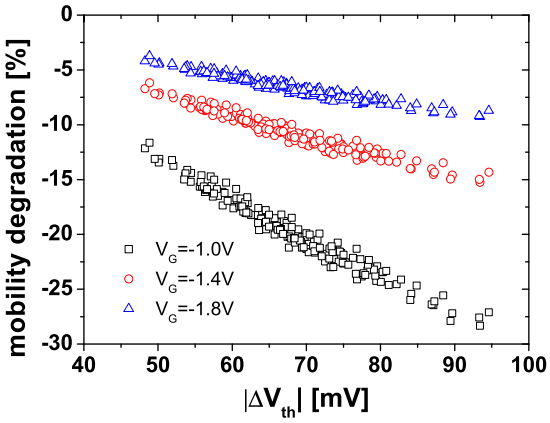

Fig. 3. Mobility degradation versus ΔV_{th} under NBTI stress. The mobility value is extracted for the gate biases of -1.0V, -1.4V and -1.8V.

and V_5 represent the energy of well 2 and well 3, respectively (electrically active trap state). V_2 is the energy barrier between well 1 and well 2 and V_4 is the energy barrier between well 2 and well 3. Δ_2 and Δ_4 represent the modifications of energy barrier heights reflecting the dissociation energy distribution due to the variation of physical parameters for Si-H bond. For each time interval, transition of the state of hydrogen particle is determined by the Monte-Carlo method with the transition probabilities in (1)-(4).

The 2D profile of the discrete trap distribution for a sample PMOSFET device generated after the NBTI stress is shown in Fig. 1, whose device structure and stress condition will be described in the following section.

III. Mobility Degradation and Estimation of Threshold Voltage Shift

In this work, the mobility degradation is calculated from the 2D profile of the interface traps generated by the TWM. To include the mobility degradation due to each discrete trap, we adopt the local mobility model [4], [5] as

$$\begin{aligned}\mu(r) &= q/m^*\Gamma(r) = q/m^*\left[\Gamma_0(r) + \delta\Gamma(r)\right] \\ &= \left[\mu_0^{-1}(r) + m^*\delta\Gamma(r)/q\right]^{-1} \\ &= \left[\mu_0^{-1}(r) + \beta\delta V(r)\right]^{-1}\end{aligned} \tag{5}$$

where $\mu(r)$ is the local mobility, q is the electronic charge, m^* is the effective mass of a carrier, $\Gamma(r)$ is the total scattering rate, $\delta V(r)$ is the potential variation due to a single trap and β is a constant fitting parameter which has been tuned to fit to the single RTS measurement [4]. With this mobility model, we simulate a device based on the 3D drift-diffusion (DD) framework to consider the spatial distribution of interface traps. Especially, as the device size scales down, the device-to-device variation of ΔV_{th} and ΔI_D due to traps become larger. ΔI_D variation is affected by two factors: one is the variation of the interface trap density and the other is the spatial distribution of the interface trap. Hence, we conduct the statistical simulation incorporating the two factors.

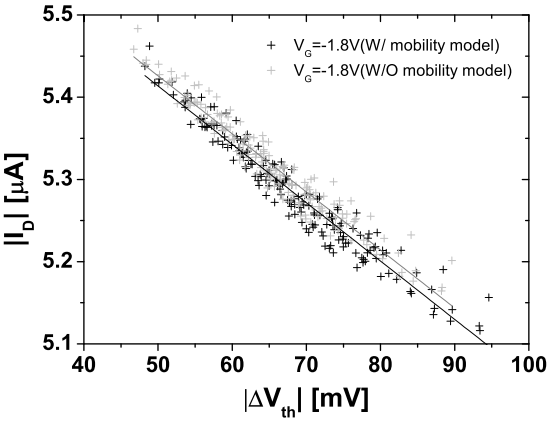

Fig. 4. I_D distribution vs. ΔV_{th} under NBTI stress with and without considering the mobility degradation. The solid line is added as the representative of the data.

IV. Statistical Simulation Results

The sample device is a planar PMOSFET whose size, oxide thickness and initial V_{th} are 140nm $\times$ 140nm, 2nm and -0.46V, respectively. V_{th} is determined at the gate voltage where the I_D is 1μA/μm^2. The drain voltage in calculating the drain current is -100mV. We simulate ΔV_{th} and ΔI_D with 35 identical samples under the NBTI stress ($V_{G,stress} = -1.8$V and $T = 400$K). The surface potential profile is shown in Fig. 2 with discrete interface traps. The potential barrier due to the trapped charge at the discrete trap interrupts the current path so that the drain current is reduced.

The mobility degradation vs. ΔV_{th} from the simulation is shown in Fig. 3 for three different gate bias conditions. Mobility decreases as ΔV_{th} increases due to the interface charge and the degradation is enhanced for smaller V_G (in magnitude) due to less screening effect. I_D degradation is extracted with and without the mobility model as shown in Fig. 4 and Fig. 5, which show an additional degradation in

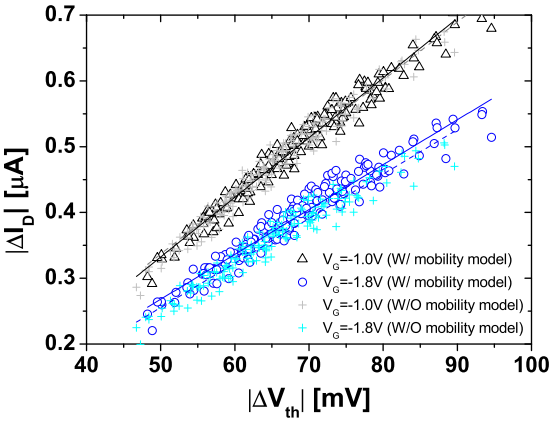

Fig. 5. ΔI_D vs. ΔV_{th} with and without inclusion of the mobility degradation model for two different gate bias conditions. The solid line are also added for the representative values of the data. Drain current degradation becomes larger when the mobility model is included.

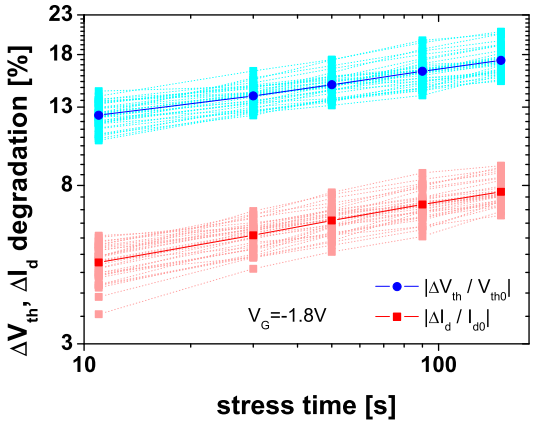

Fig. 7. ΔI_D and ΔV_{th} for 35 identical devices under NBTI stress. The gate voltage for stress is -1.8V and the drain voltage for calculating the drain current is -100mV. The thick solid lines represent the mean value of the scattered data.

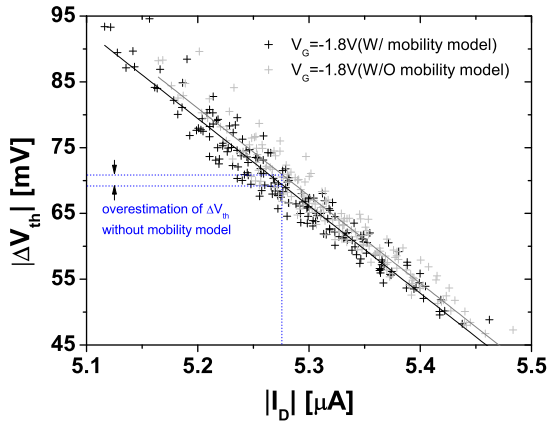

Fig. 6. ΔV_{th} as I_D under NBTI stress (inverse of Fig. 4). Without the mobility degradation, ΔV_{th} is underestimated for a given change in the drain current.

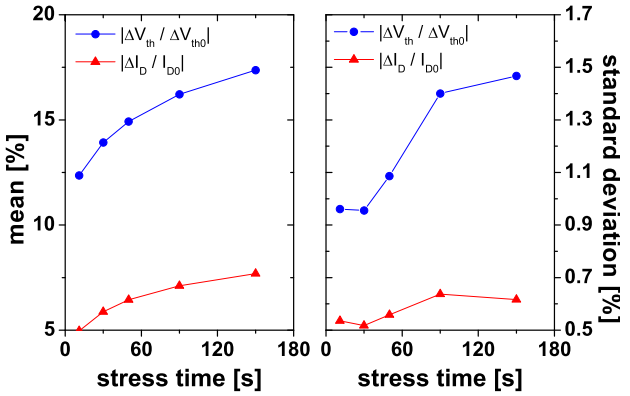

Fig. 8. Mean and standard deviation of $|\Delta I_D/I_{D0}|$ and $|\Delta V_{th}/V_{th0}|$ vs. stress time under $V_{G,stress} = -1.8$V.

current introduced by the mobility reduction as described in Fig. 3. Also a statistical distribution in the data can be observed due to the realistic interface trap profile. I_D vs. ΔV_{th} in Fig. 6 can be used for estimating ΔV_{th} from the measured I_D in the OTF measurements. One can see that ΔV_{th} is overestimated when the mobility degradation is not considered.

Changes of I_D and V_{th} vs. the NBTI stress time for 35 identical devices are shown in Fig. 7. The thick line represent the mean values of ΔI_D and ΔV_{th} and show a power-law dependence on the stress time, which is the characteristics of NBTI. The mean and the deviation of I_D and ΔV_{th} under NBTI stress are shown in Fig. 8 which shows an increase of the mean and the standard deviation as the stress time increases.

As the gate voltage increases, the mean and standard deviation of $\Delta I_D/I_{D0}$ reduce as shown in Fig. 9 which is consistent with experimental results in [7]. As the gate bias increases, increase in the screening effects reduces the effects of the trapped charges in the oxide so that both the mean and standard deviation of the $\Delta I_D/I_{D0}$ are reduced.

We study the relative contributions of the mobility and Poisson effect on $|I_D/I_{D0}|$ due to trapped charges as the gate bias increases. As shown in Fig. 10, both the mobility and Poisson effects on I_D degradation are reduced. The relative contribution of the mobility degradation to total I_D degradation and its standard deviation is calculated in Fig. 11. It is interesting to notice that the mobility portion is increased as the gate bias becomes higher while the portion is decreased as the NBTI stress time increases as shown in Fig. 12.

V. Conclusion

In this work, we extended the TWM model to obtain the 2D spatial profile of the interface trap generated by the NBTI stress and extracted ΔI_D considering the mobility degradation caused by the discrete interface traps in a 3D device simulation framework. From our simulation results, the relationship between ΔV_{th} and ΔI_D is evaluated which can

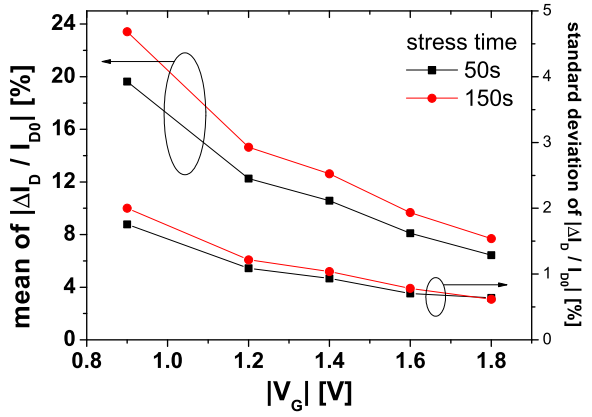

Fig. 9. Mean and standard deviation of $|\Delta I_D/I_{D0}|$ vs. gate bias in measurement for two different NBTI stress times; 50s (square) and 150s (circle).

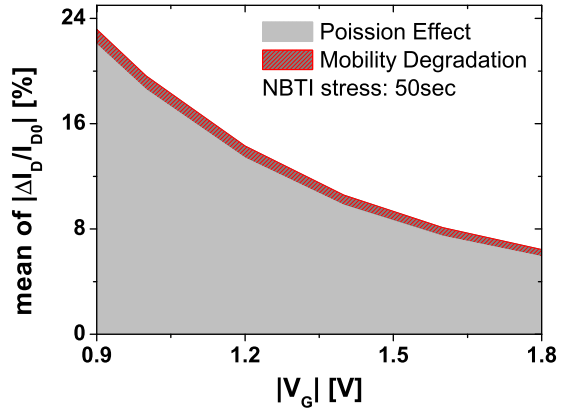

Fig. 10. Relative contribution of the Poisson effect and mobility degradation on $|\Delta I_D/I_{D0}|$ vs. gate voltage.

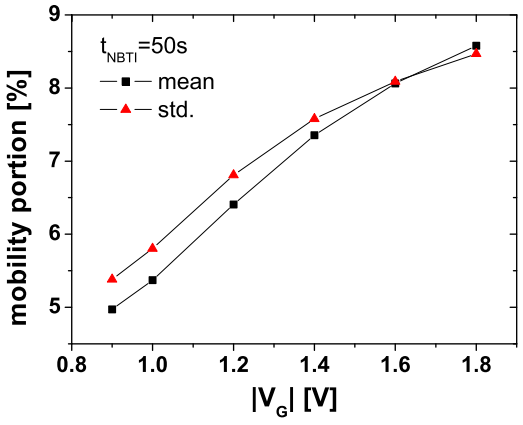

Fig. 11. Portion of mobility degradation effect on the mean and standard deviation of drain current degradation vs. gate voltage.

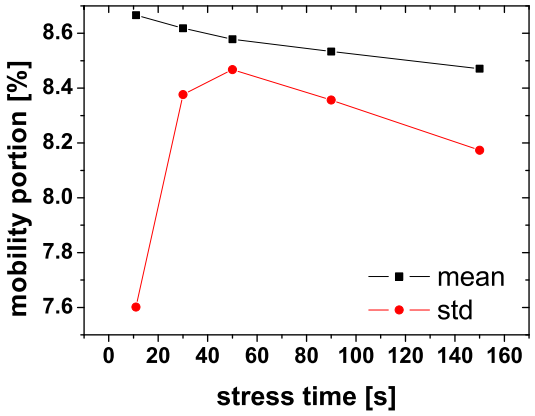

Fig. 12. Portion of mobility degradation effect on the mean and standard deviation of drain current degradation vs. NBTI stress time.

be used for correct analysis of the OTF measurement. The stress time and gate voltage dependence of contribution of the mobility degradation portion on total I_D degradation is also shown. From the simulation works, it has been shown that the incorporation of the mobility degradation caused by the discrete trap charges is important in predicting I_D degradation due to the NBTI stress.

Device-to-device variations in I_D due to the NBTI stress for the scaled devices have been analyzed. It has been shown that statistical analysis considering realistic trap distributions provide not only the statistical variations in the current degradation but a basis for correct data analysis of the NBTI stress measurements such as the OTF.

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