TCAD ANALYSIS OF A VERTICAL RF POWER TRANSISTOR

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***Abstract* — A detailed TCAD analysis of a low-C_{gd} high-power RF MOSFET incorporating a 0.25 μm sidewall gate is presented. A novel conductive plate is placed in the vicinity of the gate poly as well as underneath the gate interconnects to provide a complete shield of the gate from the influence of drain potential. The fabricated vertical DMOS device exhibits a $I_{d(sat)}$=750μA/μm and an extrinsic transconductance $g_{m(sat)}$=75μS/μm under saturation, and a BVDSS=110V. The simulated I-V and C-V characteristics match very well with the measured data. TCAD sheds light on the bias dependence of the capacitances. The penetration of potential contours near the n-drift drain recess is identified as the cause for a sharp drop in output capacitance against V_{ds}.**

Keywords - RF power; VDMOS; TCAD; output capacitance

I. INTRODUCTION

We have recently demonstrated a novel sidewall-gate, vertical power MOSFET with superior RF performances, including minimal parasitic capacitances, high power gain and extreme ruggedness against load mismatch [1-3]. Among the novelties of the HVVFET, a recess trench region is formed in the n-drift region, in which a silicided polysilicon layer residing on a thick oxide serves as a shield. The shape and physical location of the shield are chosen to allow for lower C_{gd} than any other power MOSFET technologies with similar voltage ranking. This paper reports TCAD analysis of device operation, including quasi-saturation, self-heating, and the influence of the JFET pinch region on output capacitance.

II. EXPERIMENTS

The starting material consisted of 10μm-thick n-type epilayer on a heavily As-doped Si substrate. A chain of low and high-energy phosphorus ion implantations was used to introduce extra dopants to further reduce R_{DSon}. The source and gate electrodes were contacted from the top surface to achieve minimal source inductance and maximal heat transfer capability, and the drain was contacted from the backside after wafer thinning.

As shown in Fig. 1, hexagon-shaped holes (with a typical "porosity" factor in the range of 30-50%) were etched using reactive ion etching within a sheet of dielectric stack. After the p-tub implantation which was self-aligned with respect to the edge of the hexagonal holes, a 200Å-thick gate oxide was formed at the exposed Si surface, followed by deposition of an in-situ doped poly both on the flat surface as well as along the vertical sidewall. The channel of the FET resided along the periphery of the hexagons with an estimated (electrical) gate length of about 0.25 μm.

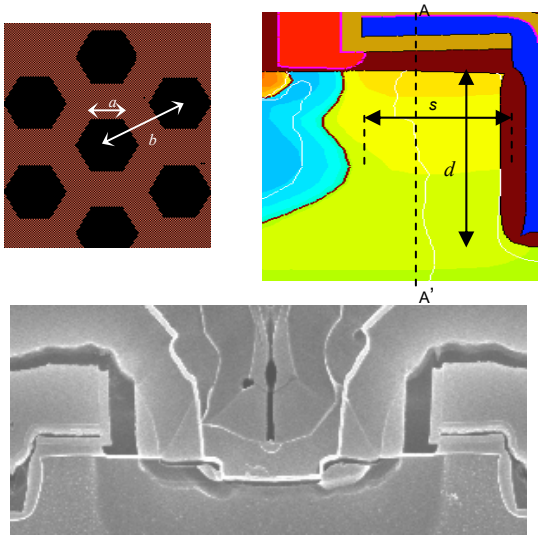

Figure 1 Hex-layout of HVVFET with side= *a* and pitch= *b*. Also shown are TCAD-generated cross-section and a SEM micrograph. Parameters *d* and *s* refer to the depth of the shallow trench and separation between the trench and dielectric sidewall, respectively. The vertical cutline A-A' is used in this paper for monitoring device internal operation.

Process and device simulations were performed using the Synopsys TCAD package. Philips mobility model was used owing to its accuracy in modeling velocity saturation, and doping and temperature dependencies of mobility [4]. The Lucent implementation of the Lombardi's formula was used to account for mobility degradation due to surface roughness and acoustic phonon scattering [5].

III. Results and Discussions

A. Current-Voltage Characteristics

Fig. 2 compares the measured (symbol) and simulated (line) I_d - V_{ds} curves for constant gate bias (V_{gs}) which steps from 1.6 to 3.4V at an ambient temperature (T_{amb}) of 300K. A good fit for the quasi-saturation results from accurate modeling of the field dependence of electron velocity. Appropriate thermal boundary conditions were chosen to simulate the self-heating-induced negative differential resistance effect.

Fig. 3 shows a good agreement between the measured and simulated 300K transfer curves at V_{ds} =0.1, 5V. Isothermal approximation was adopted, which can be justified by the negligible self-heating at low V_{ds}. The extrinsic peak transconductance (g_m) is found to be 3.5, 70, 75μS/μm at V_{ds}=0.1, 5, 10V, respectively. The values of both the extrinsic g_m and $R_{ds,\,on}$ are among the best of devices reported in the literature with similar voltage ranking; thus they are responsible for HVVFET's high frequency performance.

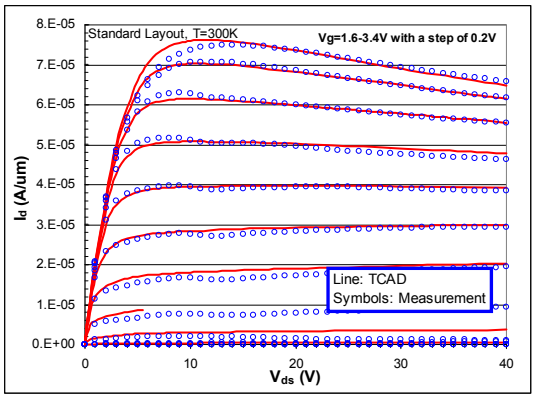

Figure 2 Measured (symbol) and simulated (line) I_d -V_{ds} family curves at ambient temperature (T_{amb}) of 300K. The total gate periphery (W_g) is 49.2 mm.

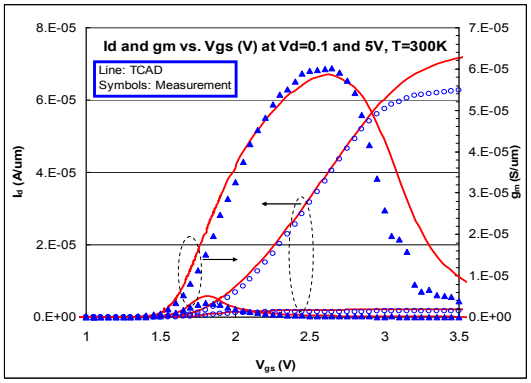

Figure 3 Measured (symbol) and simulated (line) 300K isothermal I_d – and g_m -V_{gs} characteristic with V_{ds}=0.1, 5V. This is the same part as shown in Fig. 2.

B. Capacitance-Voltage Characteristics

Figures 4 shows a good match between the measured and simulated C_{iss} versus V_{gs} characteristic of a typical packaged part; thus the measured capacitance includes the capacitive components inside the package.

Figure 5 plots the measured and simulated C_{oss} against V_{ds}. With gate grounded, C_{oss} for V_{ds} less than 4V is determined by the vertical doping profile in the upper portion of the n-drift region. On the other hand, C_{oss} at very large V_{ds} (namely >10V) is dominated by epilayer depletion. In between, there exists a transition region in which C_{oss} drops precipitously with V_{ds}, which will be discussed in more detail later. A recent report shows a 100V-breakdown VDMOS with a $C_{gd}|_{25V}$ of 8.6 X 10^{-18}F/um [6], which compares very favorably with 1.5X10^{-15} F/um obtained from an LDMOS biased at the same drain voltage [7]. HVVFET shows a C_{gd} of 1.6X10^{-18} and 1.2X10^{-18} F/um at 28V and 48V respectively, which is a further five-fold reduction as compared to the results in [6].

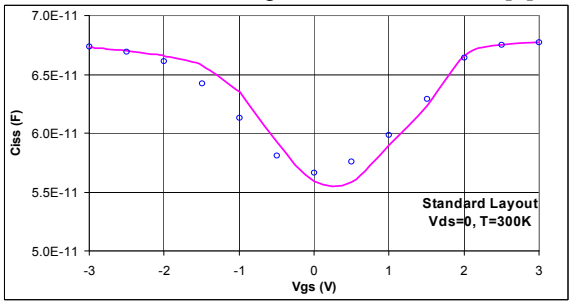

Figure 4 Measured (symbol) and simulated (line) C_{iss} vs. V_{gs} characteristics of a fully packaged part with W_g=49.2 mm. V_{ds}=0. Frequency=1MHz.

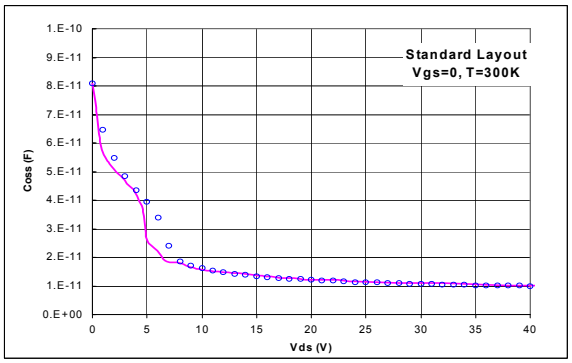

Figure 5 Measured (symbol) and simulated (line) C_{oss} vs. V_{ds} characteristics for the same part shown in Fig. 4. V_{gs}=0. Frequency=1MHz.

This region of abrupt drop of C_{oss} with V_{ds} has its origin in the lateral arrangement of HVVFET, which consists of a p-n junction on the left side and an MOS structure on the right side. As V_{ds} increases, the depletion regions associated with the p-n diode and with the MOS expand. Thus V_{tran} represents the onset of full depletion of the JFET region sandwiched between the two reverse-biased junctions. An analytical equation for V_{tran} has been derived from a simplified 1D formulation of electrostatics [8].

To elucidate the cause for the observed behavior of C_{oss} we plot in Fig. 6 the evolution of equal-potential lines for four different values of V_{ds}, with the depletion boundary shown as white lines in each plot. Deep in the Si, the equal-potential lines are parallel to the (100) surface, supporting the fact that

BVDSS of these devices is limited by the breakdown of the planar p-tub-to-epi junction. Comparing the equal-potential lines for the two lowest biases shown here, we find that at 3.75V, the JFET is not fully depleted. It becomes fully depleted only at V_{ds} greater than 7.5V. For intermediate values of V_{ds}, the propagation of depletion boundary is strongly influenced by the large doping gradient in the JFET region, resulting in a large dependence on V_{ds}.

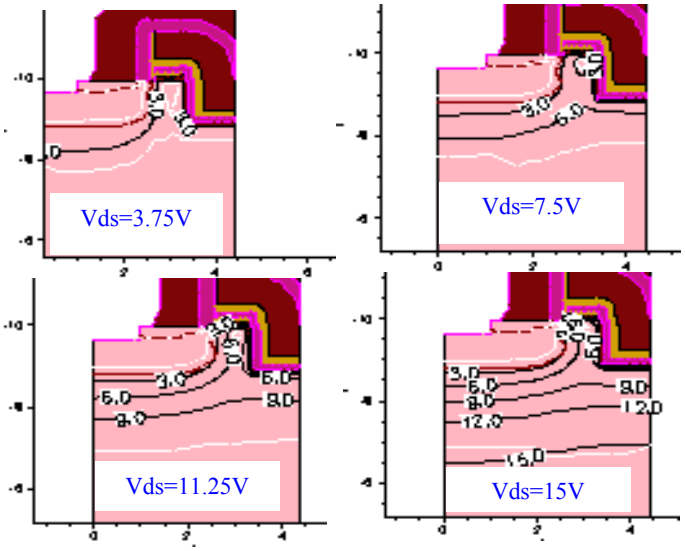

Figure 6 Simulated electrostatic potential for the standard layout at V_{gs}=0 and V_{ds}=3.75, 7.5, 11.25, 15V. The labels (from 0 to 15V in 3V step) on the lines refer to the values of the electrostatic potential. The white lines indicate the depletion boundaries.

To further confirm the mechanism responsible for the observed behavior of C_{oss}, a sensitivity study was performed using TCAD with regard to the layout parameter *s*, which was first introduced in Sec. II (Fig. 1). Fig. 7 demonstrates an upward shift in V_{pin} with *s*. As expected, independent of the value of *s*, the capacitances approach the same asymptotic limit for either $V_{ds}\rightarrow 0$ or $V_{ds}>20$V.

Figure 8(a) plots the y-coordinate dependence of the electrostatic potential under various V_{ds} along the A-A' cutline (Fig. 1). It is seen that between y= -9.97um and -9 um, the electrostatic potential is essentially pinned at ~8V. The pinning potential originates from solving the 2D nature of the device electrostatics. (It is critical to keep the pinning potential low in order to prevent surface breakdown from dominating over the planar junction breakdown.) Then, the potential starts to increase until it reaches at an inflection point. After passing the inflection point the potential curve mimics an inverted parabolic curve. Also, a 60V drain bias does not fully deplete the 10um n-epilayer, which is clearly seen in Fig. 8(b), which plots the electron density along the same cutline as in Fig. 8(a). As shown in Fig. 8(c), the peak electric field is situated at approximately y= -8um which is roughly bias independent. The shape of the field versus y-coordinate characteristic has a flat top, this field spreading is desirable for limiting the maxim field strength and for increasing BVDSS.

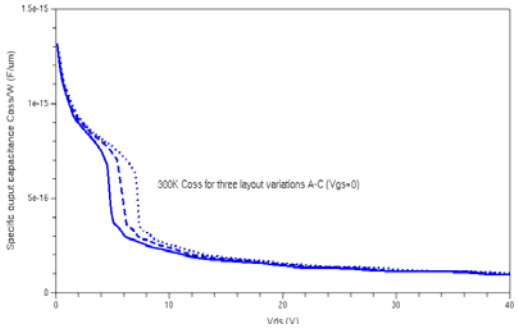

Figure 7 Simulated C_{oss}-V_{ds} characteristics at 1MHz with V_{gs} = 0V. The three curves correspond to *s*, as defined in Fig. 1, having values of Standard (solid line), Standard+0.1um (dashed line), and Standard+0.2um (dotted line).

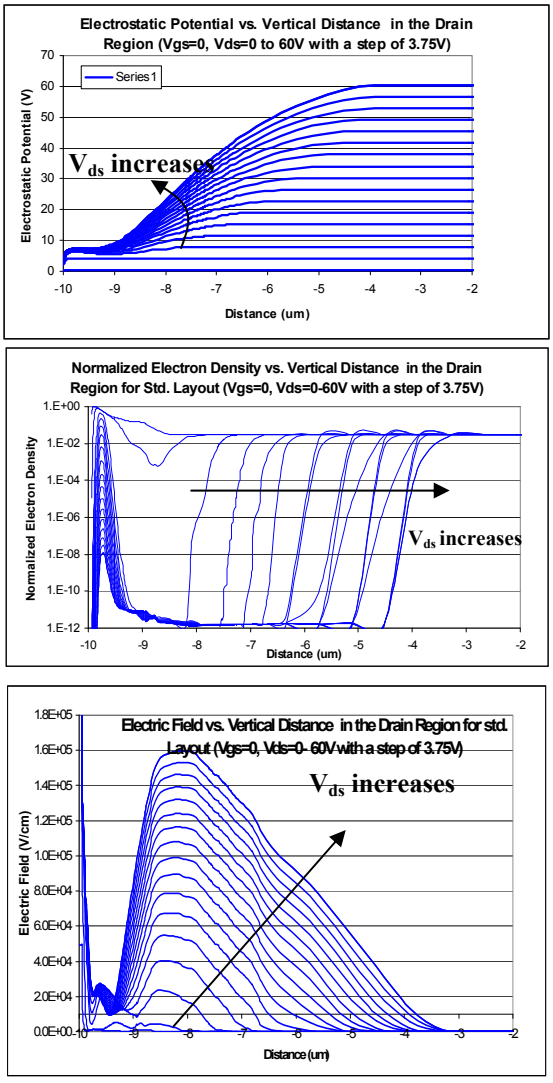

Fig. 8 (a) Electrostatic potential, (b) (normalized) electron density, (c) electrical field along the vertical cutline A-A' in the n-drift region for the standard layout. V_{ds} is a parameter stepping from 0 to 60V in 3.75V step.

V. CONCLUSIONS

We have demonstrated a novel vertical power MOSFET with a fully shielded gate. Very good matching of I-V and C-V curves is achieved between measurement and TCAD simulation. For off-state operation, the electrostatic potential is pinned to approximately 8V, independent of the external V_{ds}. This potential pinning helps prevent a premature junction and/or gate oxide breakdown at the surface. The cause for an abrupt drop in C_{oss} is identified to be the onset of full depletion of the JFET region.

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