Impact of Thickness and Deposition Temperature of Gate Dielectric on Valence Bands in Silicon Nanowires

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***Abstract*— The strain distribution and strained valence band structure in silicon nanowire with varied thicknesses and deposition temperatures of gate dielectric are discussed in detail in this work. Our calculation indicates that valence subbands are dependent on the structure and process parameters. Strain has little effects in (001) orientation. But in Si (110) nanowire, the valence subbands shift upper and warp remarkably as the gate dielectric becomes thicker. Taking thermal residual strain into consideration, the strained valence subbands go to higher energy positions compared to NW without the residual strain. The different deposition temperature by a certain process slightly influences the valence bands. Strain effects on densities of states and effective masses are also investigated.**

***Keywords*— strain tensor components; thermal residual strain; valence subbands**

Ⅰ. Introduction

During the past decades, Silicon nanowires (Si NW) have been attractive due to outstanding properties such as high carriers mobility, large ON-currents among nanoscale devices [1]. During all the building blocks for next generation electronics, Gate-all-around nanowire field effect transistors are considered as a very promising candidate following the reducing scale trend [2]. The tensile stress induced by thermal oxidation or uniaxial compressive strain from GeSi source and drain stressors can modulate channel valence band structure and hole transport performance significantly [3,4]. The device performance is structure-dependent owing to different strain effects. Indeed, strain engineering may play an important role in improving the nanoscale device performance. However, there is inevitable that lattice mismatch exists between the NW and gate dielectric layer. The corresponding misfit strain might influence the NW performance unclearly. In parallel, there are relatively few reports about the effect of gate dielectric to modulate the bands structure and of channel material as well as the device performance.

In this paper, we compute strain distribution in Si NW induced by varied thickness and deposition temperature (DT) of gate dielectric using finite element method. Then, different strain effects on Si NW property including valence structure, density of states and effective masses are investigated.

Ⅱ. Simulation Method

First, we use continuum elastic model to calculate the strain in Si NW with gate dielectric HfO_2 and SiO_2 [5]. We also assume that the nanowire is long enough in z orientation. Owing to the different growth orientation, we make a coordinate transformation from the coordinate where x=[1 0 0], y=[0 1 0] and z=[0 0 1] in Si (001) NW to a new coordinate where x= [1/2 1/2 -√2/2], y= [-1/2 1/2 -√2/2], z= [√2/2 √2/2 0] in Si (110) NW. During the process, the thermal expansion coefficient difference between the gate dielectric and silicon can induce a compressive or tensile residual strain to Si NW. We assume that thermal residual strain in the process is an integral of coefficient of thermal expansion α(T) [6,7]. Therefore, the total strain energy taking account of thermal residual strain effects can be calculated. The total strain has two parts: silicon core strain energy which can be found in ref.8 and the dielectric strain energy can be written as:

$$U_H = \frac{1}{2}\iint_H ds\{D_1^H(\varepsilon_{xx}'^2+\varepsilon_{yy}'^2)+D_2^H\varepsilon_{zz}'^2 + D_3^H\varepsilon_{xx}'\varepsilon_{yy}'+D_4^H(\varepsilon_{xx}'+\varepsilon_{yy}')\varepsilon_{zz}'+D_5^H\varepsilon_{xy}'^2\} \quad (1)$$

Where

$$D_1^H = D_2^H = \frac{E(1-v)}{(1+v)(1-2v)};$$
$$D_3^H = D_4^H = \frac{2Ev}{(1+v)(1-2v)};$$
$$D_5^H = \frac{E}{(1+v)}; \quad (2)$$
$$\varepsilon_{ii}' = \varepsilon_{ii} - \varepsilon_{ii}^H;$$
$$\varepsilon_{ii}^H = a_i^H / a_i^c - 1;$$
$$a_i^c = a_{si} + S_H - S_{si}$$

And the gate dielectric is an isotropic approximation, E is the Young's modulus and v is the Poisson's ratio[9，10]. Here, we also simplify that the gate dielectric such as HfO_2 or SiO_2 is crystal and its lattice constant is invariable. S_H and S_{si} are residual strains corresponding to gate dielectric and silicon

NW, respectively. a_i^c is the silicon lattice constant in consideration of the residual thermal strain. a_i^H is the lattice parameter of gate dielectrics. ε_{ii} is the strain tensor components in Si NW. ε_{ii}^H is the strain tensor components in surrounding gate dielectrics. The shear strain tensor ε_{xz} and ε_{yz} is zero owing to the long enough approximation.

Then, we calculate the strain energy minimum by finite element method and can calculate strain tensor components distribution. The strained valence band structures are calculated using 6×6 ***k·p*** Hamiltonian and a strain perturbation Hamiltonian with provision for a first order strain effect and the couplings between light holes, heavy holes and split-off holes [11]. And we use Bessel function as the corresponding basis functions along the z axis direction. In x-y plane, the basis function is still free plane-wave.

Ⅲ. Results and Discussion

Fig.1illustrates the strain energy distribution and strain tensor components in Si (110) NW with 3nm thick HfO_2 deposited at 473K in the process. The difference of the strain energy distribution in HfO_2 layer is large. However, the strain energy distribution in Si NW changes relatively small. There is an energy discrepancy between the Si NW and HfO_2 gate dielectric. At the same time, the strain tensor ε_{xx} and ε_{yy} are positive and ε_{xy} is negative in Si NW. From the x axis, the strain tensor ε_{xx} in gate dielectric is negative and ε_{xx} in Si NW is positive. Then, the dielectric can induce a compressive strain to Si NW. The other strain tensor components have similar effects.

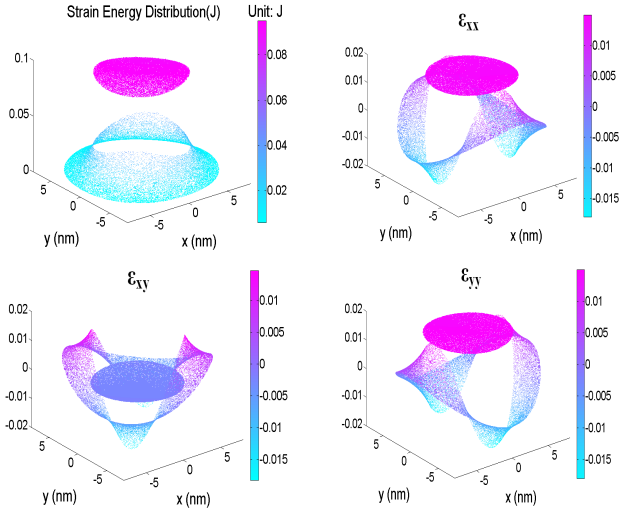

Fig.1 Strain energy distribution and strain tensor components ε_{xx}, ε_{xy}, ε_{yy} in Si (110) NW (R=5nm) and 3nm thick HfO_2 dielectric (deposition temperature: 473K)

Fig.2 shows valence band structures of Si (001) NW without dielectric (left), and with 3nm thick HfO_2 (middle), 3nm SiO_2 (right) gate dielectric, respectively. Our calculation indicates that HfO_2 and SiO_2 gate dielectrics have same effects on Si (001) NW. Compared to pure Si (001) NW, the top three valence subbands change very little. But there is a shape alteration from the 4th to 7th subband because of the gate dielectric modulation. The different temperature in NW with HfO_2 (SiO_2) insulator corresponds to the typical deposition temperature of the insulator by Atomic Layer Deposition (Thermal Oxidization Treatment).

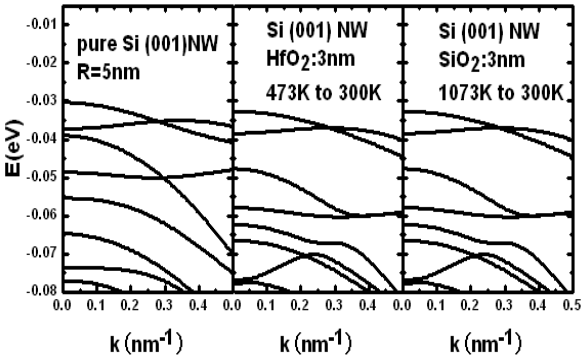

Fig.2 Valence band structures of pure Si (001) NW (left), and NW with 3nm HfO_2 (middle), SiO_2 (right) dielectric with 5nm radius

Valence band structures of Si (110) NW (left), and with 3nm, 4nm thick HfO_2 dielectric (DT=573K) are shown in Fig.3. In contrast with Si (001) NW, the valence subbands have great changes in (110) NW. Valence subband maximums all return to Γ-point by contrast to pure Si (110) NW. As increasing the HfO_2 thickness, subband maximums remarkably shift upwards. Taking the first top valence subband for example, the subband maximum is -0.02193eV at k=0 in pure Si (110) NW. Strain impact of HfO_2 gate dielectric push the first top subband to 0.2661eV (3nm HfO_2),0.28402eV(4nm HfO_2) at k=0, respectively. The rest of valence subbands have similar shifting tendency. Actually, the thermal residual strain in the above discussion has contributed to the crystal lattice dislocation and resulted in a larger strain effects. So the valence subbands shift larger than those without thermal residual strain.

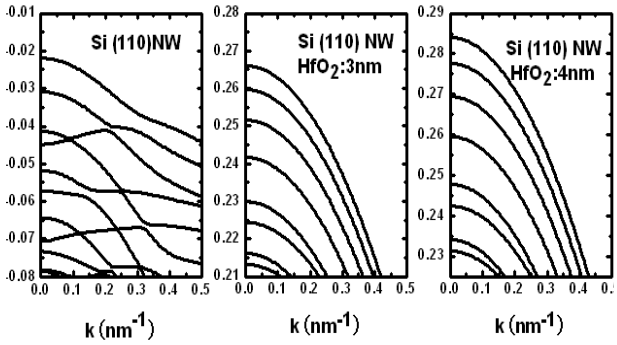

Fig.3 Valence band structures of Si (110) NW (R=5nm) with 0nm (left), 3nm (middle) and 4nm (right) HfO_2 dielectric (deposition temperature: 573K). Remarkably, valence band maximums shift upwards with HfO_2 dielectric.

Fig.4 plots valence band structures in Si (110) NW with HfO_2 (a), (b) or SiO_2 (c), (d) gate insulator at different DTs. Top valence subbands of NW with HfO_2 gate dielectric move upwards slightly at higher temperatures. The reason is that α(T) of HfO_2 is larger than silicon material and HfO_2 layer can result in a compressive strain. But valence subband variation modulated by SiO_2 gate dielectric is very tiny. The amplitude variation in temperature from 1073K to 1173K is relatively small and the corresponding residual strain

difference is negligible. The valence band structures with SiO_2 gate dielectric at 1073K and 1173K almost entirely match.

Fig.5 displays densities of states (DOS) of Si (110) NW versus thickness of HfO_2 gate dielectric. The DOS height is the effective mass within parabolic approximation. As HfO_2 dielectric thickness becomes larger, top valence subbands shift upper remarkably owing to larger strain effects.

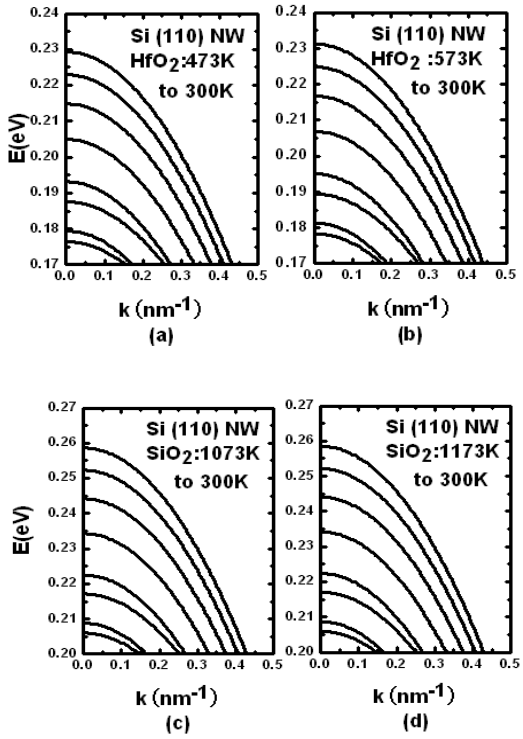

Fig.4 Valence band structures of Si (110) NW (R=5nm) with 2nm thick dielectric versus deposition temperature 473K(a), 573K(b), 1073K(c), 1173K(d)

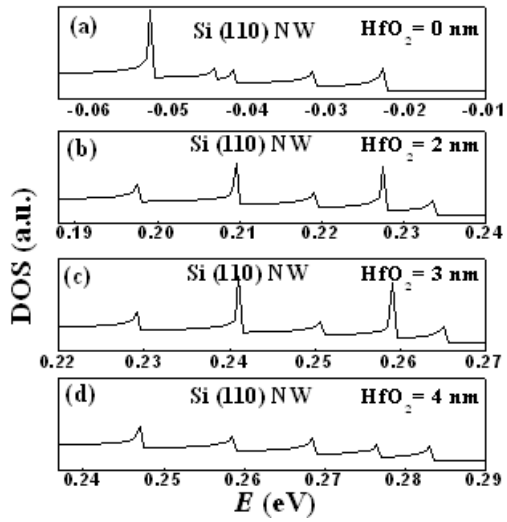

Fig.5 Densities of states of Si (110) NW (R=5nm) with HfO_2 gate dielectric versus thicknesses (deposition temperature: 573K)

Fig.6 plots DOS of NW with HfO_2 or SiO_2 dielectric at different DTs. As the DT increases in Si (110) NW with HfO_2 gate dielectric, the DOS peaks shift to higher energy positions. But the DOS peak values modulated by HfO_2 change very little. As the process temperature goes up in NW with SiO_2 dielectric, the DOS peaks in height or energy position change very tiny. This is in accordance with the valence band structures in NW with different deposition temperatures.

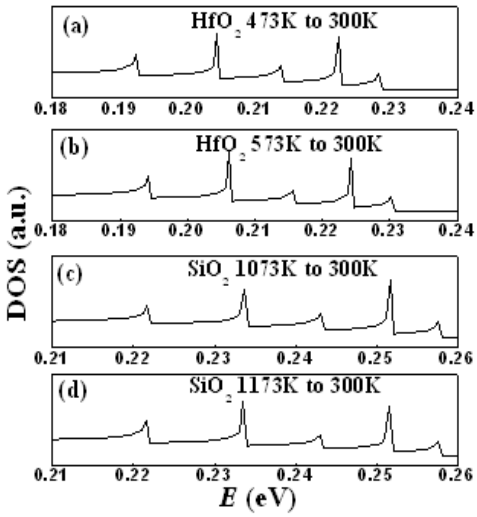

Fig.6 Densities of states of Si (110) NW versus different growth temperatures with HfO_2 (a), (b) or SiO_2 (c), (d), respectively

Fig.7 shows effective masses (|m*|) of top five subbands of Si (001) (a), (110) (b) NW and corresponding NW with 3nm thick HfO_2 (c), (d) using parabolic approximation, respectively. Effective masses of top five valence subbands in pure Si (001) NW is larger than that in pure Si (110) NW. Effective masses in Si (110) NW with 3nm thick HfO_2 dielectric are smaller than those in Si (001) NW with identical gate dielectric. The phenomenon indicates that the strain modulation by surrounding gate dielectric in Si (110) orientation is more valid than that in (001) NW.

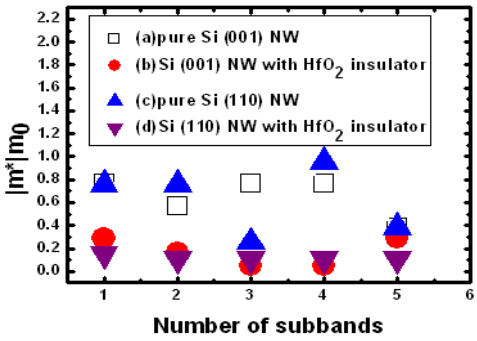

Fig.7 Effective masses of top five subbands of Si (001) (a), (110) (b) NW and corresponding NW with 3nm thick HfO_2 (c), (d)

At the same time, effective masses of the 2nd and 4th subbands in Si (001) NW with HfO_2 increases in contrast with pure (001) NW. Effective mass of the 3rd subband reduces while the others have no change. However, most effective

masses of top five subbands in Si (110) with HfO_2 have smaller values than those in pure (110) NW. The strain from gate dielectric in Si (110) is an important part in optimizing device performance.

Fig.8 plots effective masses |m*| versus thickness of HfO_2 dielectric in Si (110) NW. When HfO_2 dielectric strain effects are taken into consideration, strain effects can lower effective masses of the 1st, 2nd and 5th subbands while effective masses of the 3rd, 4th subbands increase compared to pure Si (110) NW. As the dielectric thickness increases, the effective mass has a fluctuation in top five subbands. Fig.9 describes effective masses |m*| of top five subbands versus deposition temperature for Si (110) NW (300K), with HfO_2 dielectric (473K), (573K) and SiO_2 dielectric (1073K), (1173K). NW with gate dielectric still has smaller effective masses than pure Si (110) NW. But as increasing the growth temperature, effective masses |m*| of the 1st and 2nd subbands in NW with HfO_2 have no changes while that of the 3rd subband reduces and the others increase. In Si (110) NW with SiO_2 dielectric, effective masses of the 4th and 5th subbands increase and the rest reduce. The effective mass variation in NW with different gate dielectric deposited at varied temperatures can provide a further direction to optimize the NW device performance.

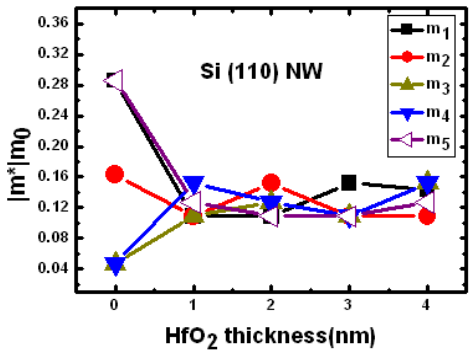

Fig.8 Effective masses of top five subbands of Si (110) NW versus different thick HfO_2 (process temperature: 573K)

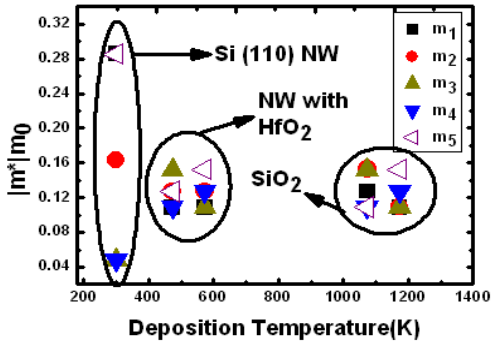

Fig.9 Effective masses versus process temperature for Si (110) NW (300K), with HfO_2 dielectric (473K, 573K) and SiO_2 dielectric (1073K, 1173K)

Ⅳ. Summary

We have calculated the impact of thickness and process temperature of gate dielectric on valence band structures in Si NW. Strain effects modulate valence bands in Si (110) NW remarkably than strain modulation in Si (001) NW. Valence subbands and hole effective masses are dependent on device structure such as axis orientation, the thickness of gate dielectric and process temperatures. Our simulation results reveal that as increasing the gate dielectric thickness, valence subbands shift upwards and warp remarkably. The thermal residual strain induced by the deposition temperature is helpful to pushing valence subbands upper. In Si (110) NW, effective masses are relatively smaller and more sensitive to the strain induced by gate dielectric. Our results are help to futher optimize Si NW based devices.

Acknowledgement

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References

[1]Y.Huang and C.M.Lieber. “Integrated nanoscale electronics and optoelectronics: Exploring nanoscale science and technology through semiconductor nanowires,” Pure and applied Chemistry, vol.76, no.12, pp.2051-2068, 2004.

[2]E. Gnani, S. Reggiani, M. Rudan, G. Baccarani. “Design Considerations and Comparative Investigation of Ultra-Thin SOI, Double-Gate and Cylindrical Nanowire FETs,” Proc. ESSDERC, pp.371-374, 2006.

[3] K. E. Moselund, P. Dobrosz, S. Olsen, V. Pott, L. De Michielis,D. Tsamados, D. Bouvet, A. O'Neill and A. M. Ionescu. “Bended Gate-All-Around Nanowire MOSFET: a device with enhanced carrier mobility due to oxidation-induced tensile stress,” IEDM, pp. 191-194, Dec 2007.

[4] T.Y. Liow,K.M.Tan, R.T.P.Lee, M.zhu, B.L.H Tan, N.Balasubramanian,Y.C.Yeo. “Germanium Source and Drain Stressors for Ultrathin-Body and Nanowire Field-Effect Transistors,” IEEE Electron Device Lett, vol.29, no.7, pp.808-810, July 2008.

[5]L. Landau and E. Lifshitz. Theory of elasticity, Butterworth- Heinmann, Oxford, 1986.

[6] Y.Okada and Y. Tokumaru. “Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 K,” J.Appl.Phys, vol.56, no.2, pp.314-320,July 1984.

[7] H. Holleck, “Material selection for hard coatings,” J. Vac. Sci. Technol. A, Vac. Surf. Films, vol. 4, pp. 2661–2669, 1986.

[8] Y. H, C. Fan; Y.Zhao, G.Du, X.Liu, R.Han. “Impact of inhomogeneous strain on the valence band structures of Ge-Si core-shell nanowires,” SISPAD, pp.121-124, Sept 2008.

[9]J. E. Jaffe, J. A. Snyder, Z. Lin, and A. C. Hess. “Low-temperature polymorphs of ZrO_2 and HfO_2: A density-functional theory study,” Phys. Rev. B, vol.72, pp. 144107, 2005.

[10]H.Ni, X.Li and H.Gao. “Elastic modulus of amorphous SiO_2 nanowires,” Appl.Phys.Lett, vol.88, pp.043108, Jan2006.

[11]T. Bahder. “Eight-band kp model of strained zinc-blende crystals,” Phys. Rev. B, vol.41, pp. 11992-12001, Jun1992.