TCAD investigation of abnormal degradation of inhibited cells in NAND Flash Structures

J. Postel-Pellerin, F. Lalande, P. Canet, R. Bouchakour
Aix-Marseille Université, IM2NP CNRS, Institut Matériaux Microélectronique et Nanosciences de Provence, UMR 6242, IMT Technopôle de Château-Gombert, 13451 Marseille, France
jeremy.postel-pellerin@im2np.fr

F. Jeuland, B. Bertello, B. Villard
ATMEL Corporation
Device Engineering
ZI de Rousset, 13106 Rousset, France

***Abstract*—In this paper, we propose to investigate the abnormal degradation on inhibited cells in NAND structures when cycling the addressed cell. The impact of the electric field is first explored and shows that the electric field isn't the main source of degradation. Then we try to identify the phenomenon occurring in the inhibition phase called "channel boosting". To visualize the potential in the channel area, a 2D TCAD simulation, emulating a 3D behavior by taking into account parasitic capacitances in the array, is developed and calibrated. We succeed in reproducing the bias conditions in the inhibited cell and to observe the emergence of a Source/Drain bias during the rising of potentials.**

Keywords-Reliability, Flash memory, oxide stress, TCAD Simulation, NAND architecture.

I. INTRODUCTION

In NAND strings the "selected" cell is the addressed cell, used in write, erase or read operation. While programming the selected cell, a high polarization is applied on Word Line (WL) so every cell sharing this WL would be programmed. To avoid this unwanted programming, these WL-neighbour cells of the selected cell must be inhibited, that's why they are called "inhibited" cells [1]. 100,000 Write/Erase cycles have been performed on selected and inhibited cells with the following bias conditions: 200µs at 17V on WL in programming and 1ms at 17V on substrate in erasing. The only difference between selected and inhibited cells is the bias applied on their Bit Line (BL) while programming, respectively 0V and V_{inh}≈3V. This polarisation V_{inh} induces a rise of the bias in the channel of the inhibited string up to about 6V, phenomenon called "channel boosting", decreasing field across tunnel oxide and avoiding programming [2-3]. Fig. 1 shows the variation of the median (on 7 dice) threshold voltage V_T during cycling for selected and inhibited cells. Selected cell shows the classical window closure and inhibited cell, which is expected to have no V_T shift, undergoes almost the same closure [4]. Several ways have been investigated to explain this degradation.

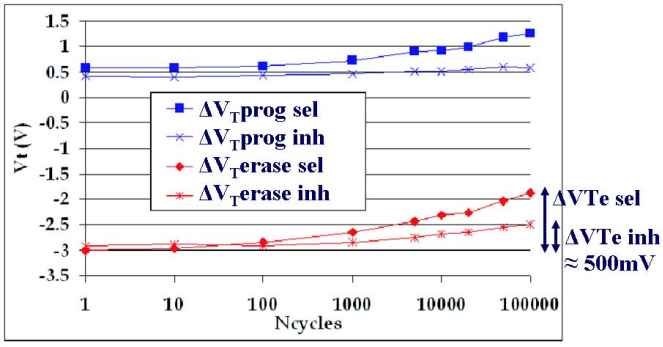

Figure 1. Programmed & Erased V_T as a function of Write/Erase cycles

II. LOW FIELD DEGRADATION INVESTIGATION

The first way which could explain the degradation of the inhibited cell is a low field degradation due to the 6.9 MV.cm^{-1} field across tunnel oxide. We looked for the bias condition to be applied on the WL, giving an equivalent field with 0V in the channel area. Fig. 2 shows the two equivalent bias conditions in term of electric field across tunnel oxide and the associated degradation levels. We can notice that although the electric field is the same, the degradation levels are very different. We have also increased the programming voltage to reach the same degradation levels which have been obtained with a 7.9 MV cm^{-1} field. A higher field is needed with 0V in the channel to have a similar stress on the inhibited cell as in the channel boosting phase. We can conclude from this that when inhibiting the cell, the low electric field induces degradation of this cell but an additional effect appears, due to the inhibition conditions. Some previous studies have shown that a V_{DS} potential can appear between source and drain contacts, causing a Gate Induced Drain Leakage current (GIDL). Some electrons are created at the source side and are accelerated to the drain by the V_{DS} bias, then being injected through tunnel oxide [5]. To explore this way, we have chosen to develop a TCAD simulation of the inhibition phase in our structure.

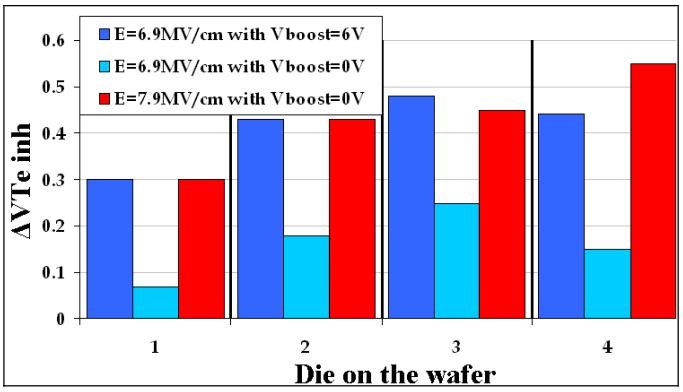

Figure 2. Threshold voltage shift of the erased state after 100,000 cycles

III. 3D EMULATED CELL SIMULATION

To visualize the phenomenon occurring in the inhibition phase, we developed a 2D TCAD process simulation taking into account parasitic capacitances extracted from a 3D simulation of a 3x3 cell array [6]. These capacitances have then been introduced by adding 4 additional contacts on the spacers of the 2D process structure, as shown in Fig. 3. This structure has been calibrated on threshold voltage measurements with a good agreement as shown in Fig. 4 and can be used to electrically simulate the inhibition conditions.

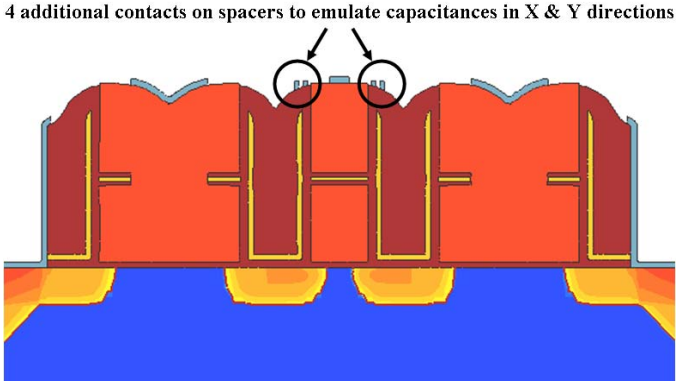

Figure 3. 2D TCAD Process structure, emulating 3D behavior thanks to parasitic capacitance consideration

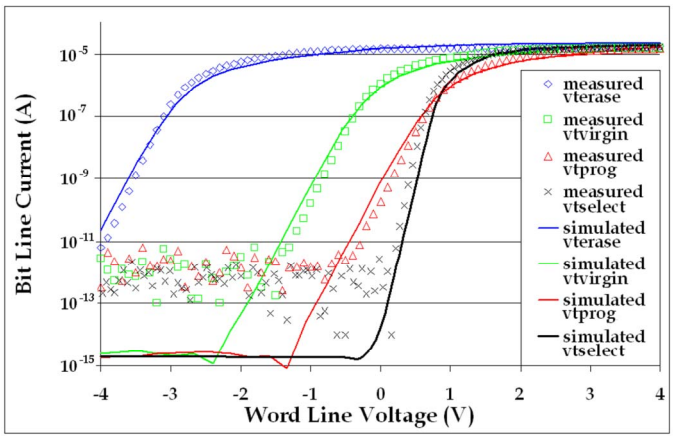

Figure 4. Calibration with I_{BL} vs. V_{WL} measurements on erased, virgin, programmed cells and on select transistors.

A. *Influence of the number of pulses in the programming phase*

To determine the involved phenomenon in the degradation of the inhibited cell, we have first search the influence of the number of programming pulses on the degradation level. We can notice in Fig. 5. that the degradation level increases logarithmically with the number of pulses used while programming the cell.

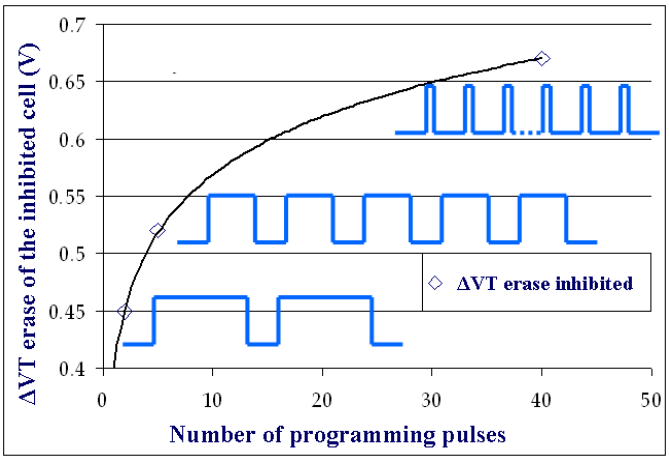

Figure 5. Logarithmic variation of the erased threshold voltage of the inhibited cell after 100,000 cycles as a function of the number of pulses used to reach the same programmed level

This shows that degradation occurs during the rising phase of inhibition polarizations. This transient phase can be simulated with our TCAD structure to identify the degradation mechanism.

B. *Electrical Simulation of the transient phase of channel boosting*

To explain this higher degradation level when increasing the number of programming pulses, we checked the uniformity of the channel boosting during the rise time. We plot in Fig. 6 the electrostatic potential simulated in the source/drain/channel area of the inhibited memory cell when reaching V_{prog}=12V and when reaching V_{prog}=17V. At V_{prog}=12V, the potential is uniform in the channel area but when the potential reaches V_{prog}=17V a Source/Drain (S/D) bias appears with a local fall in the Source area. It creates a local rise in the electric field at the corner of the Floating Gate (FG) and an electron injection, damaging the tunnel oxide.

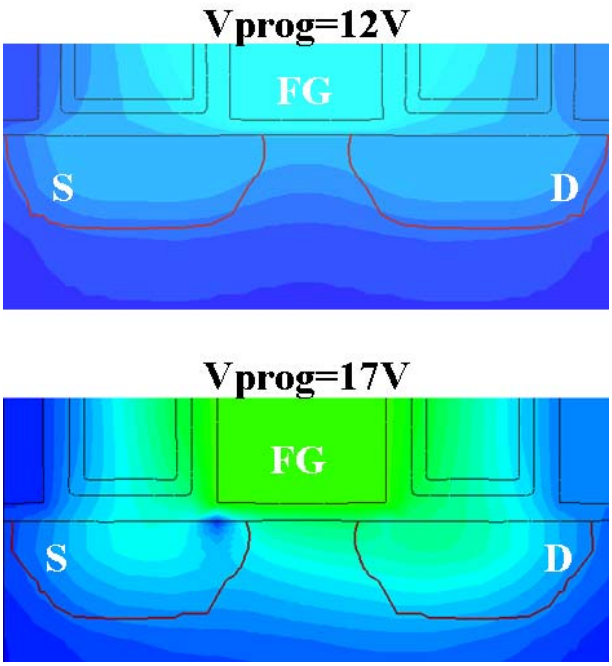

Figure 6. Electrical potential in the transient phase of channel boosting

IV. CONCLUSION

First, we present a major reliability issue in NAND Flash structures in which inhibited cells suffer degradation when cycling the addressed cell. We highlight the fact that the degradation isn't directly linked to the electric field but is mainly due to the inhibition conditions. We have also shown that the degradation level increases logarithmically with the number of pulses used while programming the cell. The phenomenon responsible for this degradation occurs in the transient phase of the inhibition that we simulated thanks to a developed 2D TCAD structure, emulating a 3D behavior by taking into account parasitic capacitances in X and Y directions, extracted on a 3D 3x3 cell array simulation. We observed the emergence of a Source/Drain bias, causing an electron injection in the Floating Gate, damaging the tunnel oxide.

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