An investigation on Effective Mobility in Nanowire FETs under Quasi-Ballistic Conditions

Elena Gnani, Antonio Gnudi, Susanna Reggiani, Giorgio Baccarani
ARCES and DEIS, University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy
Phone: +39 051 209 3773, Fax: +39 051 209 3779, E-mail: egnani@arces.unibo.it

***Abstract*—In this work we investigate the electron mobility in nanowire FETs operating under quasi-ballistic conditions. Starting from a general expression of the current-voltage characteristics worked out in a previous paper, we extract the drain current at vanishingly-low drain voltages and find the functional dependence of the effective mobility on the device length, the mean-free path and the barrier height. The resulting expression is nonlocal for short gate lengths, but may be useful for the interpretation of experimental measurements. The main result of this work is that the combined effect of acoustic-phonon and surface-roughness scattering leads to a nearly uniform mean-free path, at least for nanowire FETs with a diameter around 5 nm. Thus, mobility degradation at large gate voltages is predominantly due to carrier degeneracy, rather than an enhanced scattering rate.**

I. Introduction

Carrier mobility in silicon inversion layers has been traditionally measured in long-channel MOSFETs in order to ensure the accuracy and uniformity of the electric field and to reduce the effect of the parasitic source/drain resistance. More recently, new characterization methodologies exploiting high-frequency capacitance measurements [1] as well as the magnetoresistance technique [2] made it possible to carry out accurate mobility measurements in short-channel MOSFETs, showing that carrier mobility decreases as the channel length is reduced down to 30 nm and less [3].

Electron mobility is silicon nanowire (NW) FETs has been throughly investigated in Ref. [4]. The approach is based on the use of the Kubo-Greenwood formula and the self-consistent solution of the Schrödinger-Poisson equations within a gated nanowire and accounts for acoustic (AP) and optical phonons (OP), surface roughness (SR) and Coulomb scattering. This treatment, however, holds in the limit of infinitely-long devices and the computation is carried out numerically, so that the functional relationship which links the electron mobility with the carrier mean-free path, the gate length and the effective normal field is not made explicit.

In a recent paper [5], a rigorous analytical solution of the Boltzmann Transport Equation (BTE) in Si NW-FETs operating under quasi-ballistic conditions has been worked out under the assumption of dominant elastic collisions. From this solution, the device I-V characteristics have been determined and found to be in close agreement with a numerical solution of the BTE accounting for AP, OP and SR scattering [6].

The aim of this work is to extract from the above solution an *analytical* mobility model. As expected, this model is nonlocal and reflects the physical and geometrical features of the NW-FET via the device length and a statistically averaged momentum-relaxation length [5]. In any case, the present model may be useful for the interpretation of experimental data and for the extraction of physical parameters.

II. Mobility model

It has been shown in [5] that the current flowing within a single subband of a NW-FET can be expressed as

$$I_D = qN(x_m)\, R_t\, v_T\, \frac{\sqrt{\pi}\,\{\mathcal{F}_0(\eta_{ES}) - \mathcal{F}_0(\eta_{ED})\}}{\mathcal{F}_{-1/2}(\eta_{ES}) + R_t\,\mathcal{F}_{-1/2}(\eta_{ED})} \qquad (1)$$

where $N(x_m)$ is the electron concentration per unit length at the top of the barrier, often referred to as "virtual source"; $v_T = \sqrt{2k_BT/\pi m_x^*}$ is the thermionic velocity under nondegenerate conditions; $R_t = \lambda_p/(\lambda_p + L)$ is the transmission coefficient, λ_p and L being the momentum-relaxation length and the device length, respectively. Also, $\mathcal{F}_0$ and $\mathcal{F}_{-1/2}$ are the Fermi integrals of order 0 and $-1/2$, respectively; $\eta_{ES} = (E_{FS} - E_c(x_m))/k_BT$ and $\eta_{ED} = (E_{FD} - E_c(x_m))/k_BT$, where $E_c(x_m)$ is the subband energy at the virtual source; finally, E_{FS} and E_{FD} are the Fermi energies at the source and drain contacts, respectively. If more than one subband contributes to the current, a weighted average of terms like (1) ought to be considered, with the relative carrier populations as weighting factors.

At low V_{DS}, eq. (1) reduces to the following form

$$I_D = q\, N(x_m)\, v_T\, \frac{\lambda_p}{2\lambda_p + L}\, \frac{\sqrt{\pi}\, f_0(\eta_{ES})}{\mathcal{F}_{-1/2}(\eta_{ES})}\, \frac{qV_{DS}}{k_BT} \qquad (2)$$

where $f_0(\eta_{ES})$ is the Fermi function and the R_t expression has been made explicit. The effective carrier mobility within a NW-FET can be extracted from the equation

$$I_D = q\,\mu_{\rm eff}\, N(x_m)\, \frac{V_{DS}}{L_g} \qquad (3)$$

where L_g is the gate length. By comparing eqs. (2) and (3), it turns out that the effective mobility may be expressed as

$$\mu_{\rm eff} = \sqrt{\frac{2}{\pi}}\, \frac{q\lambda_p}{m_x^* v_{\rm th}}\, \frac{L_g}{2\lambda_p + L}\, \frac{\sqrt{\pi}\, f_0(\eta_{ES})}{\mathcal{F}_{-1/2}(\eta_{ES})} \qquad (4)$$

where $v_{\rm th} = \sqrt{k_BT/m_x^*}$ is the carrier thermal velocity for 1D structures.

The first term of eq. (4) is a pure mathematical factor close to 0.8; the second one is the standard expression of carrier

978-1-4244-3947-8/09/$25.00 ©2009 IEEE

mobility with the momentum-relaxation time $\tau_p = \lambda_p/v_{\rm th}$; the third term accounts for the gate-length dependence of the effective mobility; finally, the fourth term takes into account carrier degeneracy. Under nondegenerate conditions this term equals one, but plays a role at large gate voltages, where it is monotonically decreasing as the gate voltage is increased. The computation of this term requires the knowledge of η_{ES}, i.e. the numerical solution of the coupled Schrödinger-Poisson equations in the nanowire.

The third term in (4) represents the outcome of quasi-ballistic transport in NW-FETs and its value tends to zero in the limit of vanishing gate lengths. This result reflects the concept that the FET current is upper limited even if the gate length becomes vanishingly small, as opposed to eq. (3). Therefore, the effective mobility must go to zero in the same limit. A similar result has been obtained in Ref. [7] for nondegenerate conditions using McKelvey's flux model [8]. A further difference between the two models is that we keep distinct symbols for the device length L and the gate length L_g. The two quantities clearly differ for the extension of the source and drain regions.

We notice that, in the limit of pure ballistic transport, i.e. $L \ll \lambda_p$, eq. (4) tends to

$$\mu_{\rm bal} = \frac{1}{\sqrt{2\pi}} \frac{qL_g}{m_x^* v_{\rm th}} \frac{\sqrt{\pi}\, f_0(\eta_{ES})}{\mathcal{F}_{-1/2}(\eta_{ES})} \tag{5}$$

which, neglecting the degeneracy factor and accounting for the different definitions of the thermal velocity $v_{\rm th}$, perfectly agrees with a classical result by Shur for a 2D nondegenerate electron gas [9]. Next we observe that eq. (4) may be derived from the application of Matthiessen's rule, i.e.

$$\mu_{\rm eff}^{-1} = \mu_{\rm bal}^{-1} + \mu_{\rm sc}^{-1} \tag{6}$$

having defined the scattering-limited mobility $\mu_{\rm sc}$ as follows

$$\mu_{\rm sc} = \sqrt{\frac{2}{\pi}} \frac{q\lambda_p}{m_x^* v_{\rm th}} \frac{L_g}{L} \frac{\sqrt{\pi}\, f_0(\eta_{ES})}{\mathcal{F}_{-1/2}(\eta_{ES})} \ . \tag{7}$$

The thermionic process of carrier emission over the potential barrier at the device virtual source and the scattering process within the nanowire may thus be thought of as two limiting factors of carrier mobility acting in series. As opposed to [7], $\mu_{\rm sc}$ depends in this treatment on the ratio L_g/L, which may appreciably differ from one at the shorter gate lengths.

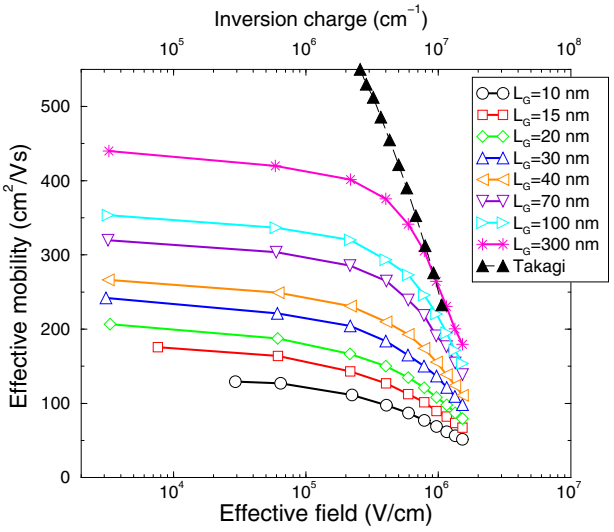

Fig. 1. Effective mobility of 5 nm diameter NW-FETs vs. effective field and inversion charge (upper scale) for different gate lengths. The computation accounts for AP and SR scattering. The gate voltage ranges from 0.5 to 1.4V in steps of 0.1V. Takagi's universal mobility curve [10] is reported for comparison with the theoretical mobility computed at the largest gate length $L_g = 850$ nm.

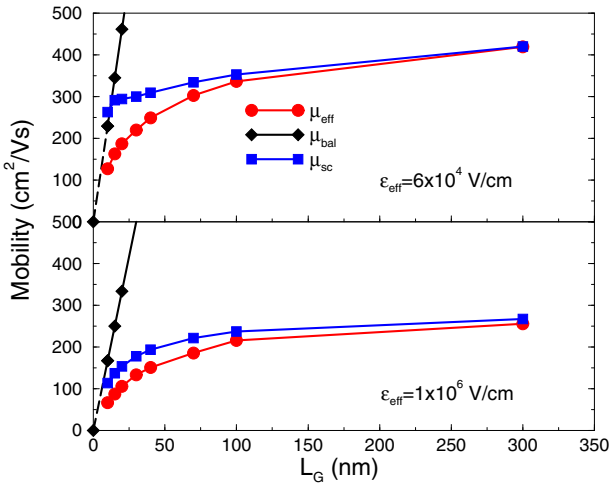

Fig. 2. Comparison of effective, ballistic, and scattering-limited mobilities vs. gate length for 5 nm NW-FETs. The effective normal fields $\mathcal{E}_{\rm eff} = 6 \times 10^4$ V/cm (top) and $\mathcal{E}_{\rm eff} = 10^6$ V/cm (bottom).

III. Results and Discussion

The mobility data presented in this section are based on self-consistent simulations of cylindrical NW-FETs with varying gate lengths, according to the procedure outlined in [5]. Therefore, no simplifying assumptions are taken in the computation of the barrier height at the device virtual source and multiple subbands are considered, as opposed to the treatment in the previous section which, for simplicity, refers to a single subband. The computations account for acoustic phonons (AP) and surface roughness (SR), but neglect Coulomb scattering, due to the assumption of an undoped nanowire within the channel. Unless otherwise specified, in our simulations the NW diameter is 5 nm, the source and drain regions are 10 nm long and the EOT equals 1 nm. Fig. 1 plots the effective mobility of electrons in NW-FETs with different gate lengths vs. the effective field. The reason for the flattening of the curves at low fields is due to the assumption of a negligible Coulomb scattering. The effective mobility decreases as the gate length is reduced according to the factor $L_g/(2\lambda_p + L)$. Instead, mobility decreases at high effective fields mainly due to carrier degeneracy. In the same figure, Takagi's universal mobility [10] is plotted for comparison. Fig. 2 represents $\mu_{\rm eff}$, $\mu_{\rm bal}$ and $\mu_{\rm sc}$ vs. gate lengths at the effective fields $\mathcal{E}_{\rm eff} = 6\times10^4$ V/cm (top) and $\mathcal{E}_{\rm eff} = 10^6$ V/cm (bottom).

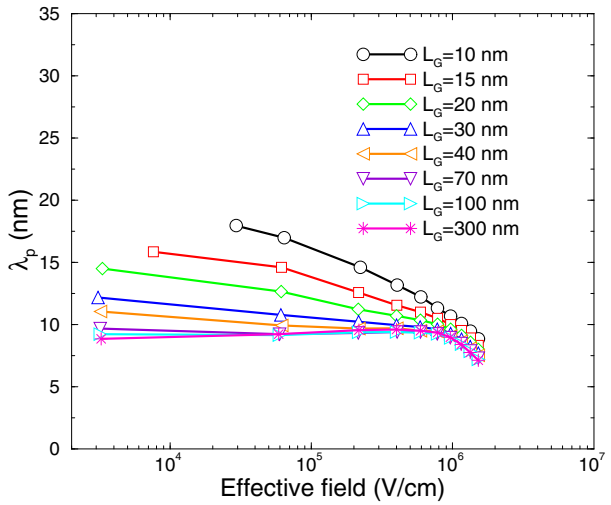

Fig. 3. Electron mean-free path vs. effective field for different gate lengths of 5 nm diameter nanowire FETs. The drop of the curves at the largest fields is due to the carrier repopulation of the primed ladder.

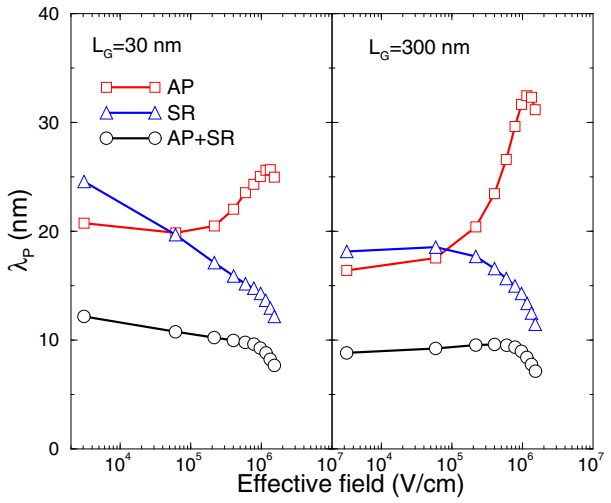

Fig. 5. AP, SR, and AP+SR mean-free paths vs. effective field for the gate lengths L_g = 30 (left) and L_g = 300 nm (right). The shorter gate lengths reduces the growth of the AP mean-free path.

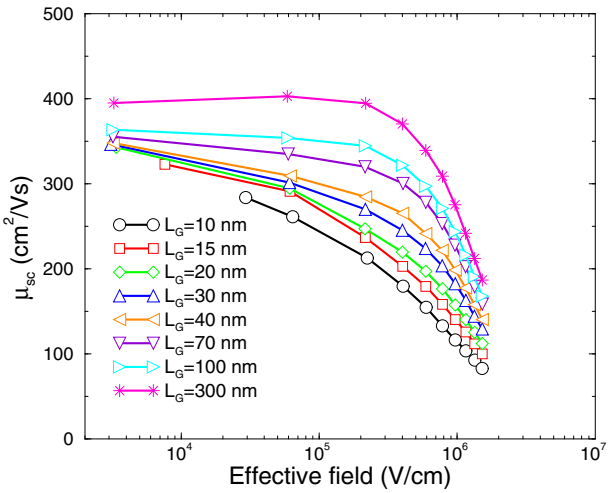

Fig. 4. Scattering-limited mobility vs. effective field for different values of the gate length. The ratio L_g/L in eq. (2) reverses the sequence of the curves with respect to that of the mean-free paths.

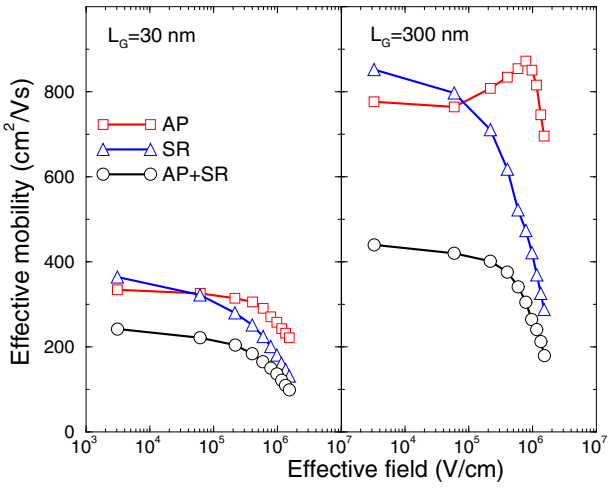

Fig. 6. AP, SR and AP+SR mobilities vs. effective fields for the gate lengths L_g = 30 nm (left) and L_g = 300 nm (right). The shorter gate length reduces the growth of the AP mobility.

$\mu_{\rm bal}$ is strictly proportional to the gate length; instead, $\mu_{\rm sc}$ is weakly varying at the lower field as L_g changes from 10 to 300 nm, despite its dependence on the ratio L_g/L which ranges from 0.33 to 0.94 in our simulations. The carrier mean-free path is plotted in fig. 3 vs. the effective field for different gate lengths. The sensitivity of λ_p with the gate length at low fields is due to the influence of the source and drain regions, where the scattering rate is lowered due to the higher kinetic energy and the reduced density of states. The drop at large fields is due instead to the repopulation of the primed subband ladder, which enhances the scattering rate via the larger transport and the smaller radial effective masses [5]. The moderate variation of λ_p across the explored range of gate voltages (from 0.5 to 1.4 V) indicates that the combined effect of AP and SR scattering is not overly sensitive to the effective normal field, and contradicts our perception of a more intense scattering rate intrinsically related with the high gate voltage. Therefore, the degradation of $\mu_{\rm eff}$ and $\mu_{\rm sc}$ visible in fig. 1 and in fig. 4, is mainly due to the effect of carrier degeneracy. In order to investigate this aspect further, we plot in fig. 5 the AP and SR mean-free paths vs. effective field for two gate lengths, namely 30 (left) and 300 nm (right). For both of them, we notice a growth of λ_p (AP) with the electric field due to the increased form factor, which reflects the widening of the electron distribution in the NW as the gate voltage is increased. For the same reason, the nearing of electrons to the interface lets λ_p (SR) monotonically decrease with the effective field. The partial compensation of the two effects makes the global mean-free path nearly uniform. The influence of the gate length on mobility is highlighted in fig. 6, where the

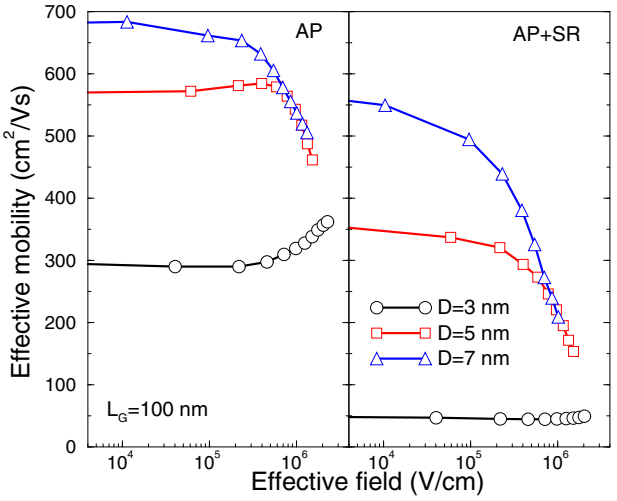

Fig. 7. AP (left) and AP+SR (right) mobilities for a 100nm long NW-FET vs. effective field for three different diameters of 3, 5, and 7 nm.

AP, SR and AP+SR mobilities are plotted for L_g = 30 nm (left) and L_g = 300 nm (right). The AP mobility of the longer device exhibits a growth due to the increase of the form factor with the effective field, until the degeneracy factor prevails forcing the curve to bend down. This effect, however, disappears at L_g = 30 nm due to the short-channel effect, which makes degeneracy stronger at smaller gate voltages. Fig. 7 shows the influence of the NW diameter on the AP (left) and AP+SR (right) mobilities for a gate length of 100 nm. For the larger diameter ($D = 7$ nm) the electron distribution is not confined at the center of the NW, and a thin inversion layer forms in the vicinity of the interface, similarly to the case of a 2D electron gas. Hence, the AP mobility does not exhibit a growth with the effective field, but shows instead a decreasing behavior. For the smaller diameter ($D = 3$ nm), the electron confinement is much stronger, and a larger field is required in order to enhance the form factor, so that the mobility growth is shifted to higher effective fields and prevails over the degeneracy factor despite its decrease from 1 to 0.53 for the first subband at the largest field. When the combined effect of AP and SR is accounted for, the two NWs with the largest diameter exhibit the standard decreasing behavior, while the NW with the smallest diameter shows a nearly flat, although much reduced, mobility.

IV. Conclusions

In this work, we have examined the behavior of carrier mobility in thin NW-FETs subject to quasi-ballistic transport. The mobility model is derived from a rigorous analytical solution of the BTE, and we find that the effective mobility at short gate lengths may be thought of as the Matthiessen's combination of the ballistic and a scattering-limited mobility which retains in its expression the ratio between the gate and the device lengths. The computations account for AP and SR scattering, as well as for multiple subbands in the nanowire FET via the numerical solution of the coupled Schorödinger-Poisson equations. Therefore, no major simplifying assumptions are taken. As opposed to the long-channel mobility, it is found that the effective mobility at short gate lengths has a nonlocal nature which makes it not useable for device simulation purposes. On the other hand, it corresponds to the experimental mobility determinations in short-channel FETs, and may thus be used for the interpretation of experimantal data and the extraction of physical parameters.

One of the main conclusions of this work is that the degradation effect which occurs at large gate fields is not so much due to an increased scattering rate but, rather, to carrier degeneracy, at least for nanowire diameters around 5 nm. This conclusion is supported by the relatively uniform carrier mean-free path against the effective field. This is due to a partial compensation of the separate effects of AP and SR scattering. The growth of the form factor with the effective field makes in fact the AP mean-free path increasing, thus balancing the growth of SR scattering. The electron mobility, however, is invariably decreasing with the gate voltage due to carrier degeneracy, which represents the main mobility degradation factor.

Acknowledgment

This work has been partially supported by the EU Network of Excellence NANOSIL via the IUNET Consortium.

References

[1] S. Severi, L. Pantisano, E. Augendre, E. S. Andres, P. Eyben, and K. De Meyer, "A Reliable Metric for Mobility Extraction of Short-Channel MOSFETs," *IEEE Trans. on Electron Devices*, vol. 54, no. 10, pp. 2690-2697, October 2007.

[2] Y. Meziani, J. Lusakowski, F. Teppe, N. Dyakonova, W. Knap, K. Romanjek, M. Ferrier, R. Clerc, G. Ghibaudo, F. Boeuf, and T. Skotnicki, "Magnetoresistance Mobility Measurements in sub 0.1 μm Si MOSFETs," in *Proc. of the 34th European Solid-State Device Research Conference (ESSDERC-2004)*, 2004, pp. 157-160.

[3] A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez, R. Gwoziecki, F. Boeuf, H. Brut, G. Ghibaudo and T. Skotnicki, "Unexpected mobility degradation for very short devices: A new challenge for CMOS scaling," *Proc. IEEE Int. Electron Devices Meeting (IEDM'06)*, San Francisco, CA, p. 663.

[4] S. Jin, M. V. Fischetti and T.-W. Tang, "Modeling of electron mobility in gated silicon nanowires at room temperature: Surface roughness scattering, dielectric screening and band nonparabolicity", *J. Appl. Phys.*, vol. 102, pp. 083715, 2007

[5] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Quasi-Ballistic Transport in Nanowire Field-Effect Transistors," *IEEE Trans. on Electron Devices*, vol. 55, no. 11, pp. 2918-2930, November 2008.

[6] M. Lenzi, P. Palestri, E. Gnani, S. Reggiani, A. Gnudi, D. Esseni, L. Selmi, and G. Baccarani, "Investigation of the Transport Properties of Silicon Nanowires Using Deterministic and Monte Carlo Approaches to the Solution of the Boltzmann Transport Equation," *IEEE Trans. on Electron Devices*, vol. 55, no. 8, pp. 2086-2096, August 2008.

[7] R. Wang, H. Liu, R. Huang, J. Zhuge, L. Zhang, D.-W. Kim, X. Zhang, D. Park and Y. Wang, "Experimental Investigations on Carrier Transport in Si Nanowire Transistors: Ballistic Efficiency and Apparent Mobility", *IEEE Trans. on Electron Devices*, vol. 55, no. 11, pp. 2960-2967, Nov. 2008.

[8] J. P. McKelvey, R. L. Longini and T. P. Brody, "Alternative approach to the solution of added carrier transport problems in semiconductors", *Phys. Rev.*, vol. 123, no. 1, pp. 51-57, Jan. 1961.

[9] M. Shur, "Low Ballistic Mobility in Submicron HEMTs," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 511-513, September 2002.

[10] S. Takagi, A. Turiumi, M. Iwase, and H. Tango, "On the Universality of Inversion Layer Mobility in si MOSFET's: Part I-Effects of Substrate Impurity Concentration," *IEEE Trans. on ED*, vol. 41, no. 12, pp. 2357-2362, Dec. 1994.