Effect of Impact-Ionization-Generated Holes on the Breakdown Mechanism in LDMOS Devices

T. Sakuda, N, Sadachika, Y. Oritsuki, M. Yokomichi, M. Miyake, T. Kajiwara, H. Kikuchihara
U. Feldmann, H. J. Mattausch and M. Miura-Mattausch

Graduate School of Advanced Sciences of Matter, Hiroshima University
1-3-1 Kagamiyama, Higashi-Hiroshima, Hiroshima Japan
sadatika@hiroshima-u.ac.jp

Abstract— **The breakdown mechanism in LDMOS devices with high resistive drift region sustaining high-voltage applications is analyzed and explained. Holes generated by the impact-ionization in the drift region are found to hinder the formation of the breakdown condition by increasing the potential underneath the gate-overlap region. This mechanism is modeled and implemented into the compact model HiSIM_HV for circuit simulation. Good agreement of simulated characteristics with 2D-device simulation results has been achieved.**

Keywords-Compact Modeling; High Voltage Transisters; LDMOS; Breakdown ; Impact Ionization

I. INTRODUCTION

The LDMOS (Laterally Diffused Metal Oxide Semiconductor) is an extension of MOSFETs for high voltage applications. By optimizing the resistive drift region at the drain side, it can be utilized for wide variety of bias conditions to be applied (see Fig. 1). However, the breakdown voltage V_{break} cannot be optimized in a simple way by reducing such as the impurity concentration in the drift region N_{drift}. Fig. 2a shows the *I-V* characteristics for different N_{drift} at the gate voltage V_{gs}=10V. By reducing N_{drift} it is expected that V_{break} increases. However, 2D-device simulation results show plateaus before the steep current increase of the breakdown condition. This step-like current increase in the drain current is called the expansion effect [1, 2].

It is our purpose to understand the reason for the expansion effect and to model the phenomenon to reflect device features for high performance circuit simulations. We demonstrate here that the high resistive drift region hinders the occurrence of the breakdown condition due to the potential change by the generated holes through the impact-ionization. The generated holes influence the whole potential distribution within the device, and not only the drain terminal current but also source terminal current is increased. These mechanism are modeled successfully by the hole storage within the drift region as well as the channel region, and the model is implemented into HiSIM_HV, a circuit simulation model based on the complete surface-potential-based description [3, 4, 5].

II. POTENTIAL DISTRIBUTION IN LDMOS

Fig. 2b shows the potential distributions along the device surface for three devices with different drift impurity concentrations of N_{drift}=5x10^{15}, 1x10^{16} and 5x10^{16} cm^{-3} at the bias conditions shown in Fig. 2a by circles. Most potential drop occurs within the drift region for the case, where N_{drift} is low i.e. high resistive case. On the other hand, with highly doped N_{drift}, applied voltage to the drain terminal is consumed mostly within the p-body / drift junction. It is also seen in Fig. 2c that the position where the impact-ionization occurs is moved to the drain contact for the case where N_{drift} is low and the expansion effect is observed in the I_d-V_{ds} characteristics.

III. MODELING OF THE IMPACT-IONIZATION UNDER THE EXPANSION PHENOMENON

Hereafter we focus on the case of N_{drift}=1x10^{16} cm^{-3}. Fig. 3a shows calculated I_b-V_{gs} characteristics by a 2D-device simulation where I_b is the bulk current detected on the bulk node. It is observed that I_b shows conventional bell-shaped characteristics for lower V_{gs} bias condition (V_{gs} < 7V), whereas exponential increase of I_b is observed for high V_{gs} bias condition. Different impact-ionization mechanisms for these two different characteristics are demonstrated in Fig. 3b. Contours of the generated hole concentration are compared for the gate biases of V_{gs}=4V and 10V. It is seen that the bulk current increase for high V_{gs} is due to the impact-ionization which occurs within the drift region near the drain terminal. Exactly under this high V_{gs} condition, the expansion effect is observed.

Fig. 4 shows the drain current I_d and the bulk current I_b simulated by a 2D-device simulator. Fig. 5 compares potential distribution along the LDMOS surface with and without impact-ionization for different drain voltages, starting from V_{ds}=20 upto 40V by fixing V_{gs} to 10V. As can be seen in Fig. 3a, negligible impact-ionization occurs within the drift region for V_{ds}=20V, and no difference between with and without is seen. Whereas the potential in the overlap region increases for V_{ds}=30 and 40V, due to the hole storage underneath the overlap region. This potential increase results in decrease of the potential drop in the drift region resulting in suppressed impact-ionization within the drift region.

The expansion effect caused by the impact-ionization in LDMOS is modeled using compact transistor model HiSIM_HV [6] by considering the potential increase in the overlap region caused by the generated holes. In HiSIM_HV, 3 surface potentials (potential at the source side, at the end of the channel and at the p-body / n-drift junction) are considered as shown in Fig. 6. These potential distributions are obtained by solving Poisson's equation and the resistance effect across the drift region. Using these calculated potential distributions, the bulk current I_b is written as

$$I_b = I_{ds} \cdot \mathbf{SUBLD1} \cdot E_{y,max} \cdot \exp\left\{-\frac{\mathbf{SUBLD2}}{E_{y,max}}\right\} \quad (1)$$

where **SUBLD1** and **SUBLD2** are model parameters. The maximum electric field $E_{y,max}$ is written with the potential values as

$$E_{y,max} = \frac{Vds + Ps0 - Psdl}{L_{drift}} \quad (2)$$

To extend this model equation for the expansion effect, Eq. 2 is rewritten as

$$E_{y,max} = \frac{Vds + Ps0 - Psdl - \Delta V}{L_{drift}} \quad (3)$$

where ΔV is the potential increase by the generated holes underneath the overlap region, which is modeled as

$$\Delta V = \mathbf{SUBLD3} \cdot I_b (V_{ds} - \mathbf{VDSTH}) \quad (4)$$

where **VDSTH** and **SUBLD3** are parameters which describing the threshold drain voltage at which the generated holes starts to increase the potential and the magnitude of the influence of the generated hole on the potential modification, respectively. For the I_b calculation, we need iterative approach solving Eqs. 1, 3 and 4 consistently. To minimize the calculation cost we simplify the approach by approximating I_b for the ΔV calculation given in Eq. 1.

Calculation results for I_b and I_d are plotted in Fig. 7a and b respectively in comparison with 2D-device simulation results. Suppression of the I_b is modeled accurately. On the other hand, simple addition of the impact-ionization-generated bulk current to the drain current underestimates simulated I_d-V_{ds} characteristics as is observed in Fig. 7b. This is because the generated holes further flow into the channel and increase the potential within the channel. This results in the increase of the source current as can be seen in Fig. 8.

IV. Increase of the Drain Current

To model the reason for the source current increase in HiSIM_HV, 3 potential values within the LDMOS, potential at the corner of the gate-overlapped region, potential at the junction and potential in the p-body region (shown by A, B and C in the inset of Fig. 9, respectively) are simulated by a 2D-device simulator and the results are plotted in Fig. 9. It is seen that not only the potential at the overlap edge, but also the potential values at the drain junction as well as at the source junction increase by the generated holes. We confirmed that potential increase at the source/drain junction is responsible for the source current increase shown in Fig. 8. In HiSIM model, this is considered as a bulk bias increase as

$$I_{ds} = f(V_{gs}, V_{ds}, V_{bs} + \Delta V_{bs}) \quad (5)$$

$$\Delta V_{bs} = I_b \cdot \mathbf{IBPC1} \quad (6)$$

and this approach can also be employed here for LDMOS with inclusion of the potential increase at the drain junction as.

$$\Delta V_{bs} = \frac{\Delta V_{Body} + \Delta V_{Junction}}{2} \quad (7)$$

here ΔV_{Body} and $\Delta V_{Junction}$ are potential enhancement by the hole at the body and p-body / n-drift junction, respectively. Potential increase by the impact-ionization at the body region ΔV_{body} is plotted as a function of I_b in Fig. 10a. Liner dependence is observed and modeled in the same manner as Eq. 6 as

$$\Delta V_{Body} = I_b \cdot \mathbf{IBPC1} \quad (8)$$

The junction potential increase $\Delta V_{junction}$ (indicated by B in the inset of Fig. 9) is also plotted in Fig. 10b and is modeled in the similar manner,

$$\Delta V_{Junction} = I_b' \cdot \mathbf{IBPC3} \quad (9)$$

here I_b' is the saturating bulk current which can be calculated with Eqs. 1 to 4. Finally the calculated total I_d-V_{ds} characteristics are plotted in Fig. 11 including the expansion effect. It is seen that the developed model correctly captures all mechanism modifying the breakdown in LDMOS.

V. Conclusion

A model which reproduces breakdown behavior in LDMOS devices is developed based on the potential distribution within the drift region. It has become clear that in high resistive LDMOS devices, there is a remarkable current increase in the saturation region. This increasing current is stabilized by the impact-ionization-generated holes, expanding the device-operation region up to higher breakdown voltages.

Acknowledgement

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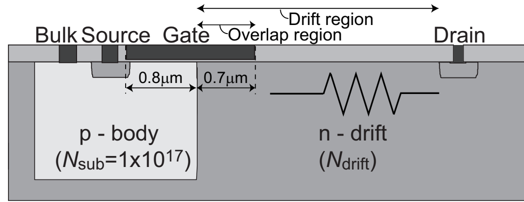
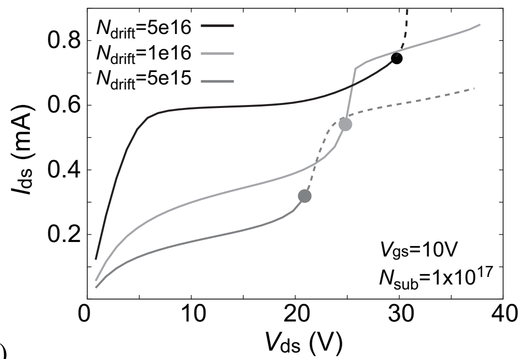
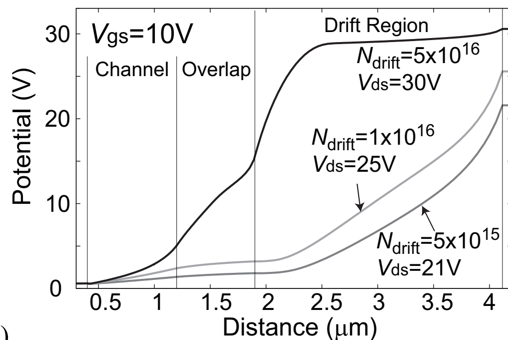


Figure 1. Schematic of the LDMOS for high voltage application. High resistive drift region and long overlapped region are specific in comparison to the conventional MOSFET for high voltage operation.



(a)



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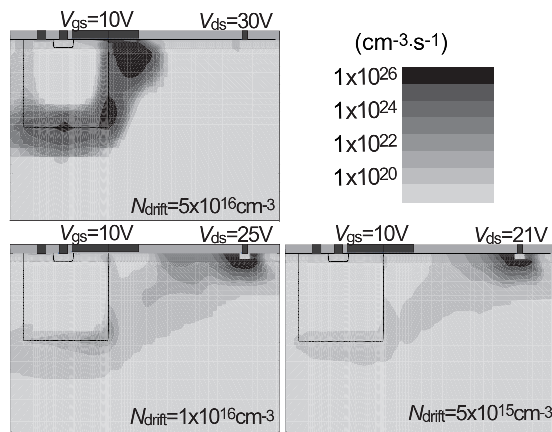
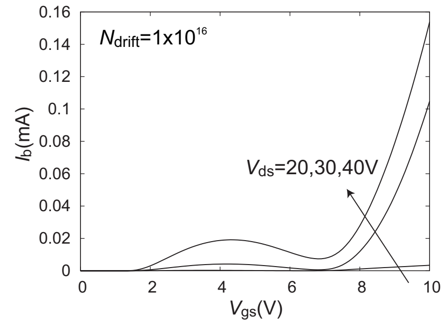


(c)

Figure 2. (a) Simulated I_d-V_{ds} characteristics with a 2D-device simlator for various impurity concentrations in the drift region; (b) Potential distribution alnog the surface; (c) Contour plot of the hole generation density.



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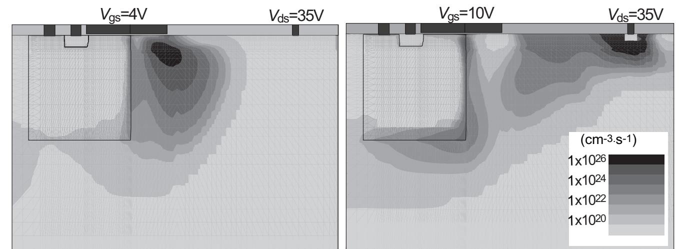


(b)

Figure 3. (a) Simulated I_b-V_{gs} characteristics for different V_{ds} values by a 2D-Device simulation; (b) Contour of the generated hole concentration at V_{ds}=35V for V_{gs}=4V (left) where bell-shaped I_b-V_{gs} is observedand and 10V (right) where monotornious increas of I_b-V_{gs} is observed.

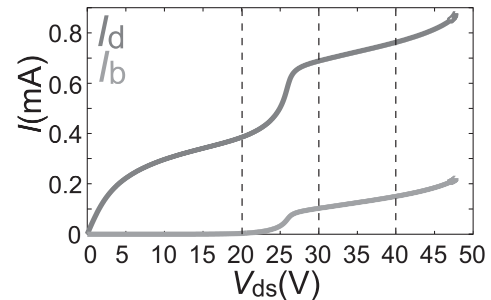


Figure 4. 2D-device simulation results of I_d, I_b and I_s -V_{ds} as a function of the drain voltage V_{ds} at applied gate bias V_{gs}=10V.

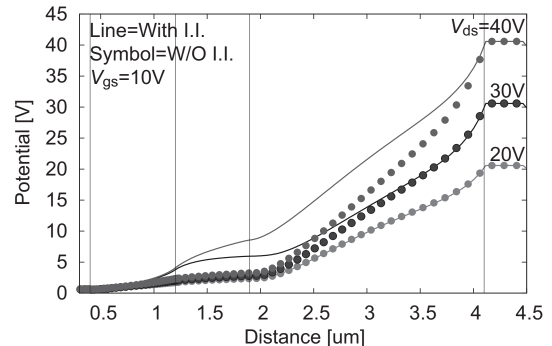


Figure 5. Simulated potential distribution along the LDMOS surface from source to drain electrode with / without impact-ionization consideration for different bias conditions by 2D-device simulation.

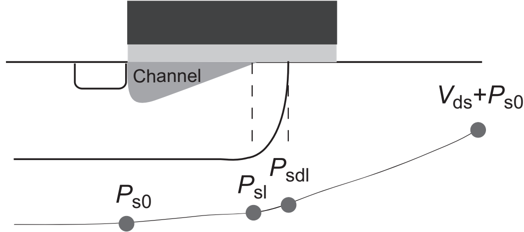
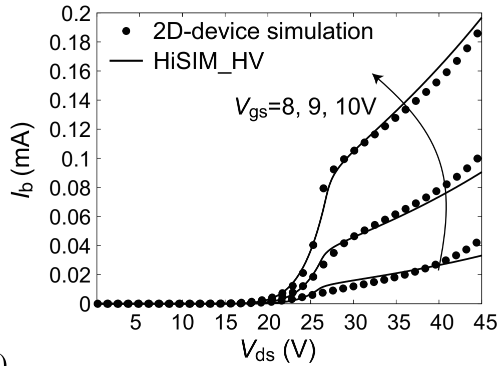
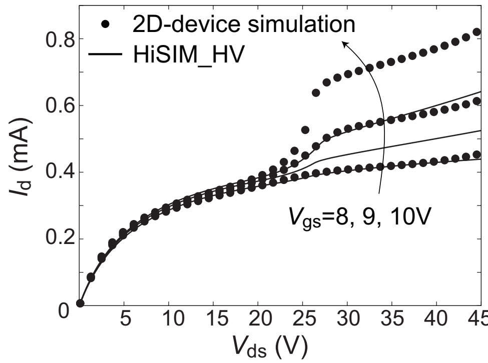


Figure 6. Potentials distribution calculated by HiSIM_HV.



(a)



(b)

Figure 7. Comparisons of HiSIM_HV results with the developed modle (a) I_b-V_{ds} and (b) I_d-V_{ds} For comparison, 2D-device simulation results are depicted.

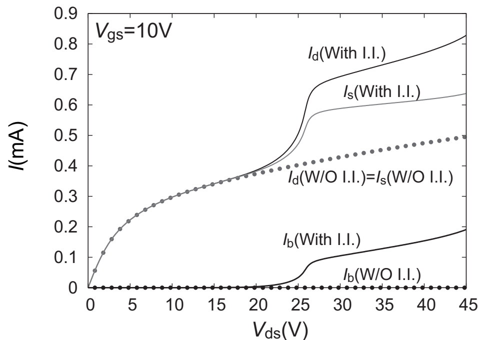


Figure 8. Separation of the simulated drain current by a 2D-device simulator into different components. Results with and without the impact ionization are compared.

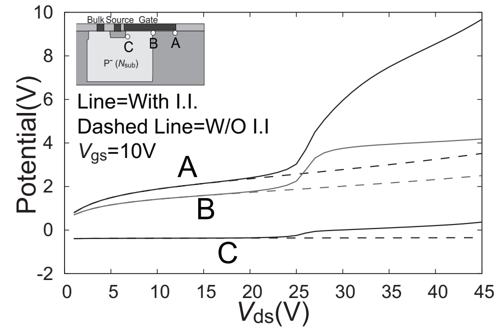


Figure 9. Simulated potential values by a 2D-device simulation at 3 different positions in the LDMOS shown in the inset plotted as a function of applied V_{ds} with / without impact-ionization conisderation.

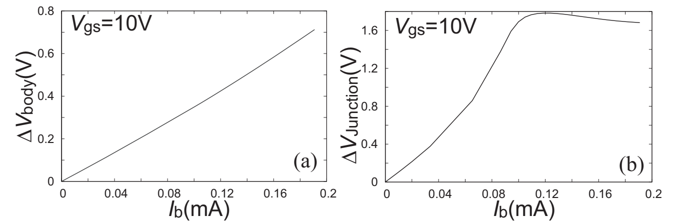


Figure 10. Simulation results of the potential increase by the impact-ionization as a function of bulk current I_b (a) at the body (position C in Fig. 9) and (b) at the p-body / n-drift junction (position B in Fig. 9).

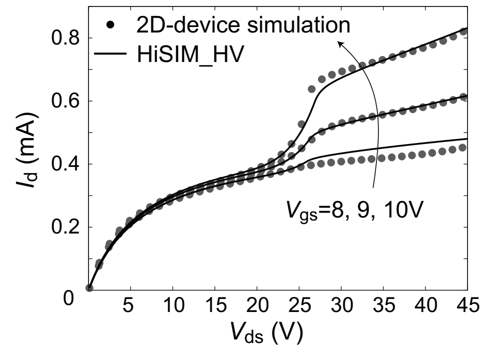


Figure 11. I_d-V_{ds} characteristics with the modeled expansion effect in comparison to 2D-device simulation result.