Study on Influence of Device Structure Dimensions and Profiles on Charge Collection Current Causing SET Pulse Leading to Soft Errors in Logic Circuits

Katsuhiko Tanaka, Hideyuki Nakamura, Taiki Uemura,
Kan Takeuchi, Toshikazu Fukuda, and Shigetaka Kumashiro
MIRAI-SELETE
Sagamihara Office, NEC Sagamihara Plant, 1120 Shimokuzawa, Sagamihara 229-1198, Japan
E-mail: tanaka.katsuhiko@selete.co.jp

***Abstract*—Current responses due to the strike of ionized particle onto nMOS transistor of 90nm and 55nm generation have been analyzed through 3D device simulations. From the current response, duration of charge collection (t_{cc}) is determined, which correlated strongly with the width of erroneous pulse (SET pulse). Causes of the difference between t_{cc} values of 90nm and 55nm generation MOSFETs have been investigated and it is found that the difference in STI depth and width of p-well contact line between these two generations influences t_{cc} mainly. This is because that the resistance below the p-well contact affects the ability to pull out the excess holes remaining in the channel region. It is also shown that there is room for reducing t_{cc} and hence SET pulse width by well profile engineering.**

I. Introduction

Neutron-induced soft error phenomena have received much attention since they are considered as one of the major obstacles to realize highly reliable LSIs. Although Single-Event-Upset observed in memory circuits such as SRAMs and flip-flops is still major concern, soft error phenomena occurring in combinational-logic circuits can be more serious in future technology node [1]. In the logic circuits, propagation of erroneous signal, called Single-Event-Transient (SET), occurs and the erroneous signal might be finally stored, for instance, in a flip-flop as illustrated in Fig. 1. The wider the SET pulse is, the more probably the erroneous signal is stored. Such a SET pulse is initially caused by collection of generated charge due to the impact of the ionized particle. In this paper, duration of charge collection is evaluated which is related to SET pulse width strongly, and its dependence on device structure dimensions and profiles is investigated.

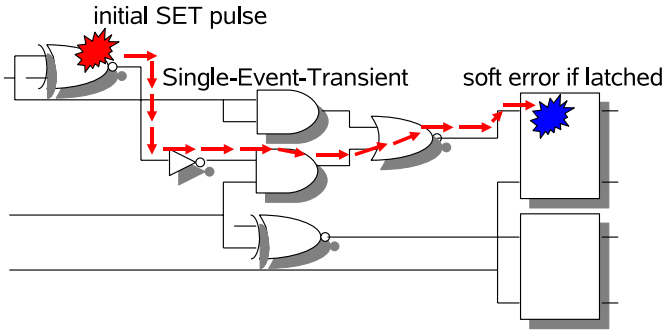
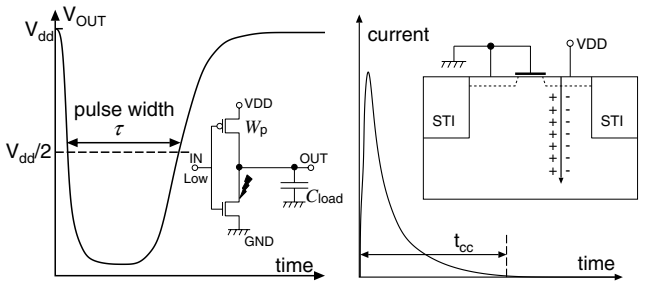


Fig. 1: Soft error in a logic circuit where Single-Event-Transient participates.



(a) (b)

Fig. 2: (a) SET pulse width and (b) duration of charge collection t_{cc}.

II. Evaluation of Duration of Charge Collection

SET pulse width is determined by the time during which the output voltage of the logic cell varies more than $V_{dd}/2$, as depicted in Fig. 2 (a). Although it is possible to evaluate the SET pulse width directly by, for instance, mixed-mode device simulation, we adopted simpler way to evaluate the significance of the SET pulse. In our method, the current response is calculated under the condition that the drain voltage is fixed. From this current waveform, the duration of charge collection, t_{cc} (Fig. 2 (b)), which is determined by the time until the charge collection current diminishes down to certain current level (e.g. 0.1mA in this work), is defined.

The duration of charge collection is evaluated using single nMOSFET structure as shown in Fig. 3. Since we focus on generation of the SET pulse in logic cells, well contacts span the whole structure, which is common in logic applications. For simplicity, pMOS transistor is omitted, although n-well layer is introduced. In most of our calculations, it is assumed that the ionized particle passes vertically through the nMOS drain layer, about 0.1μm away from the gate edge. For analyzing pulse responses, 3D device simulator (HyDeLEOS developed by SELETE [2]) is utilized.

Figure 4 (c) shows relations between t_{cc} and the SET pulse width calculated for the inverter cell by mixed-mode device simulation. Relations corresponding to two kinds of ion tracks are shown. One is the case that the ion passes through the center of the diffusion area (Fig. 4 (a)) and the other is the case that the ion passes 150nm away from the diffusion area (Fig. 4 (b)). In both cases, linear dependence of SET pulse

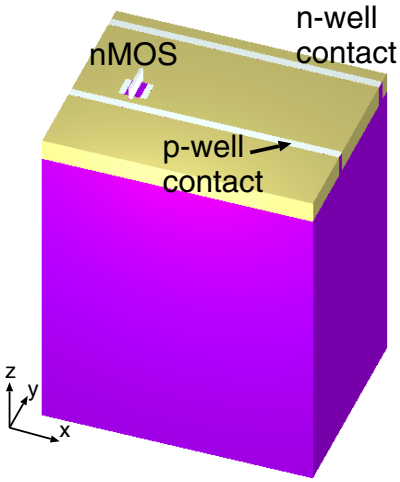
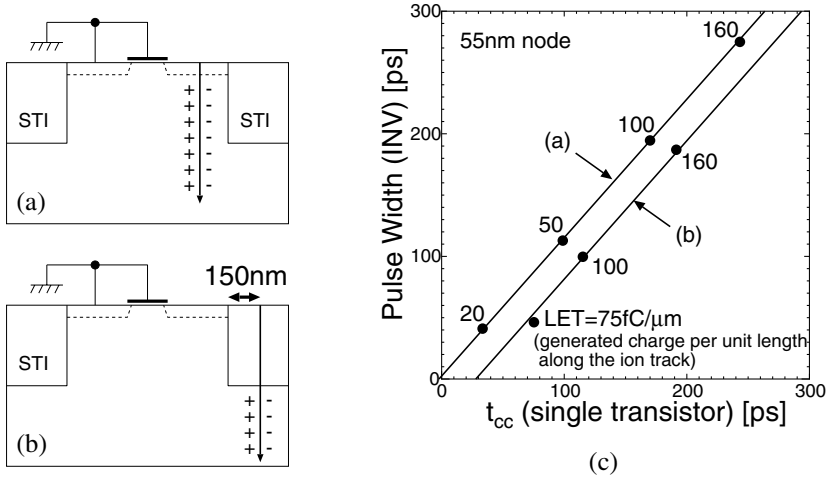


Fig. 3: 3D Device structure to calculate t_{cc}.



(c)

Fig. 4: (a) Ion track passing through the center of the drain. (b) Ion track passing 150nm away from the drain. (c) Relation between SET pulse width and t_{cc}.

width upon t_{cc} is observed. Since t_{cc} reflects ability to collect charge, it is natural that t_{cc} has close relation to the SET pulse width, and therefore, t_{cc} can be a good measure to evaluate the SET pulse.

III. Dependence of Duration of Charge Collection on Device Structure Dimensions and Profiles

In Fig. 5, current responses for 90nm and 55nm generation nMOSFETs are compared and large difference in t_{cc} is observed. It is predicted that soft error in logic circuits becomes significant mainly due to the increase in clock frequency because the probability of latching the erroneous signal increases. However, this result shows that SET pulse width can increase greatly as the transistor is scaled down, which makes soft error rate due to SET worse than previous prediction. Therefore, it is important to investigate this difference and find out the way to suppress increase in t_{cc}.

The current response for 55nm nMOSFET has longer tail, which implies that the excess holes in the channel that lower the potential barrier between the source and the drain, stay longer. In order to clarify the cause of this behavior, dependence of t_{cc} upon various device dimensions and profiles is investigated. The device structure of 55nm technology node is used as a reference, whose gate length is 50nm since the device is designed for low-power applications.

First, the dependence on gate length and channel profile is examined. An imaginary 90nm nMOS structure is generated from the 55nm nMOS structure by expanding gate length to 85nm and replacing the channel profile with that of 90nm generation nMOSFET. Since the gate length, which corresponds to the base width of the parasitic bipolar transistor, gets larger, reduction of t_{cc} is expected. Variation of t_{cc} due to this modification is about 7% as shown in Fig. 6

Figure 7 shows the dependence of t_{cc} on the area of the active region surrounded by STI. Area is changed by

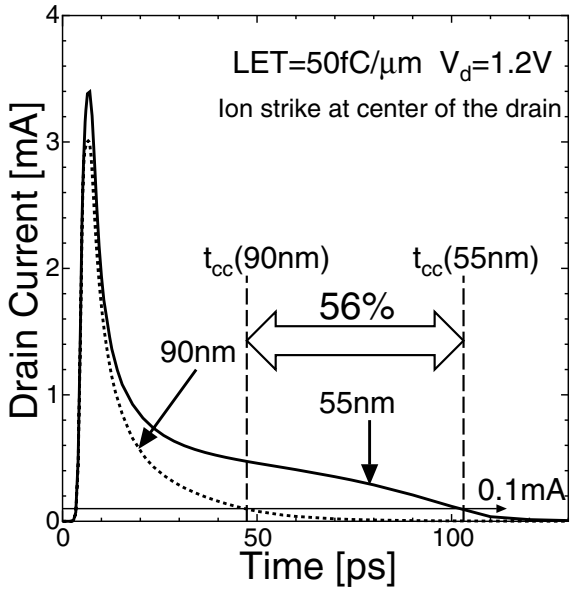


Fig. 5: Current responses for 90nm and 55nm generation nMOSFETs.

expanding/shrinking the active region in both x and y direction in the same ratio. Basically, t_{cc} slightly increases as area decreases since hole diffusion to substrate is inhibited due to the narrow active region. However, t_{cc} begins to decrease for further scaled-down active region, because the region where carriers are generated overlaps STI region and hence, effective generated charge decreases. In our calculation, distribution of generated charge around the ion track is Gaussian and the region within 2σ from the center (shown by dotted circle in the inset of Fig. 7) has almost the same width as that of drain diffusion area of 55nm technology node. As a whole, the dependence of t_{cc} on area of active region is not much remarkable. In case that the size of the active area is expanded

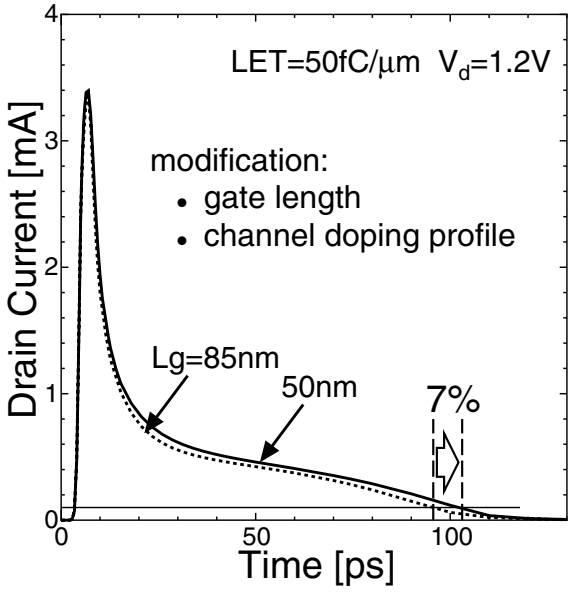


Fig. 6: Current responses for nMOS with different L_g.

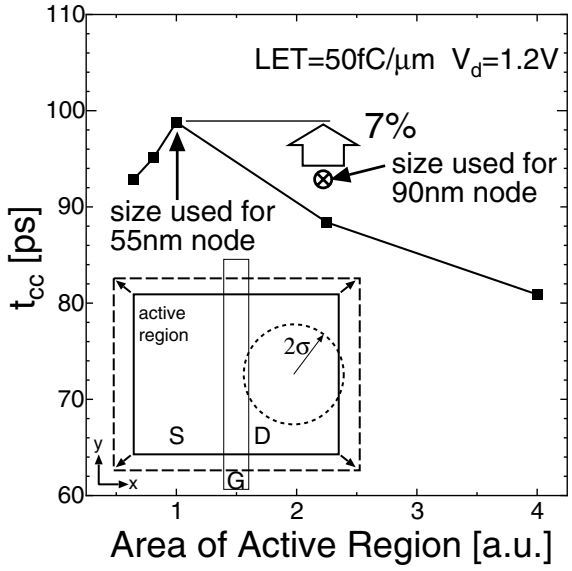


Fig. 7: Dependence of t_{cc} on the area of the active region.

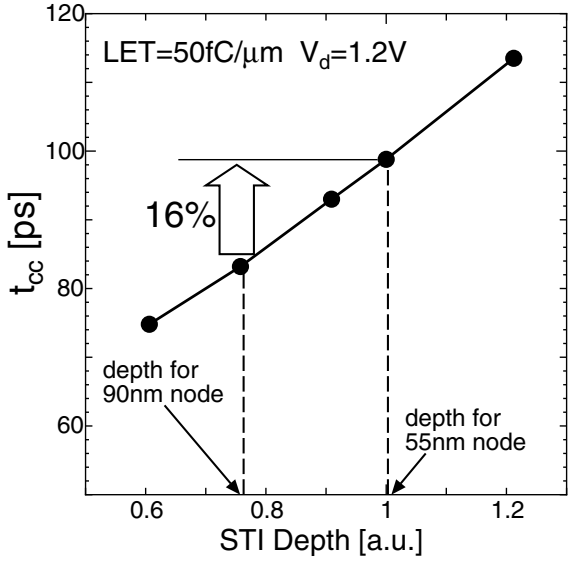


Fig. 8: Dependence of t_{cc} on STI depth.

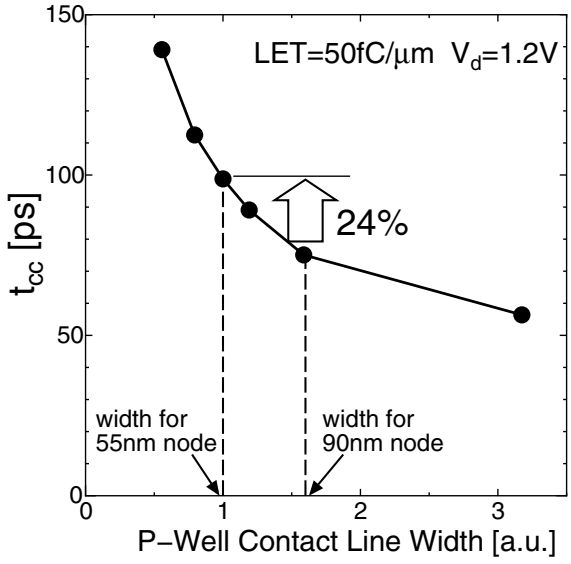


Fig. 9: Dependence of t_{cc} on the width of the p-well contact line.

to that of 90nm nMOSFET, t_{cc} is reduced by 7%.

Dependence of t_{cc} on STI depth is shown in Fig. 8. Since deep STI prevents hole from diffusing into the substrate and the p-well contact, large t_{cc} is expected for the structure with deep STI. By using STI depth of 90nm node, about 16% variation in t_{cc} is observed.

Figure 9 shows dependence on the width of the p-well contact line. Narrow contact increases the resistance between p-well and the contact, which degrades the ability to pull out holes from the channel. Use of contact width of 90nm node reduces t_{cc} by about 24% and t_{cc} is most sensitive to this factor.

Figure 10 summarizes the influence of device structure dimensions and profiles on the duration of charge collection. The difference between t_{cc} of 90nm node and 55nm node is mostly explained by the factors investigated so far. Apparently, width of the p-well contact line and STI depth affect t_{cc} strongly, which implies that increased resistivity between the channel and the p-well contact leads to larger t_{cc} in 55nm node. Since the shrink of device dimensions is a top priority, an approach to reduce t_{cc} other than relaxing device scaling is desired. Figure 11 shows the effect of introducing additional boron into two different regions. One is the region under the p-well contact (a), and the other is the region under the STI (b). The former case reduces t_{cc} more effectively, which shows that engineering of the well profile including the profile under

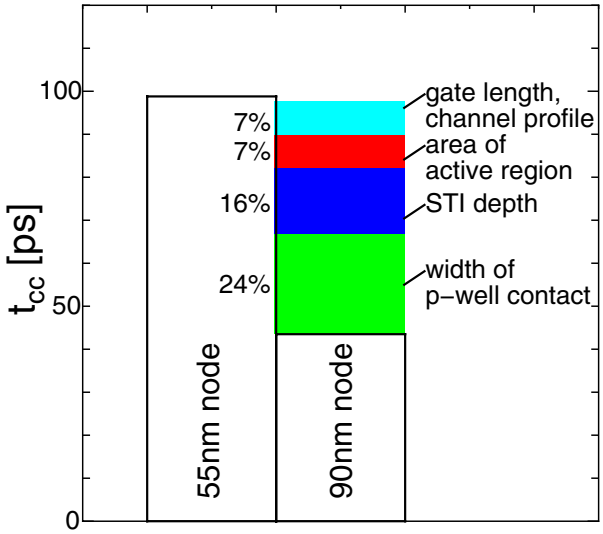


Fig. 10: Causes of the difference between t_{cc} of 55nm nMOSFET and that of 90nm nMOSFET.

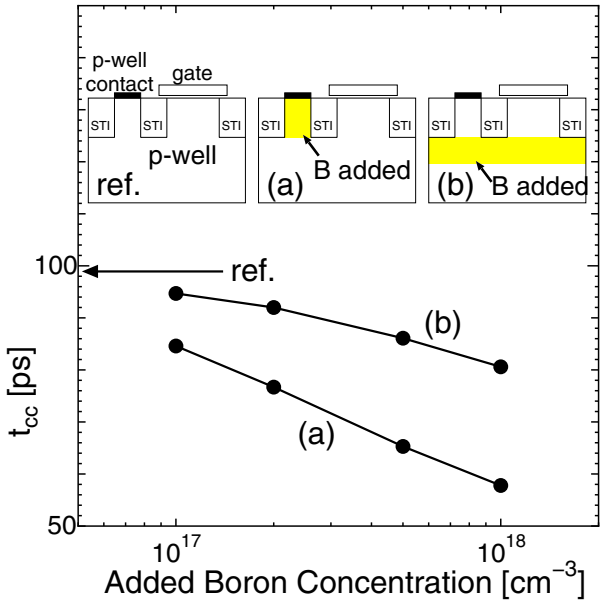


Fig. 11: Reduction of t_{cc} by introducing additional boron.

the well contact, can shorten the SET pulse width.

From the calculation of the current responses under the condition that the drain voltage is fixed, one can derive the useful information on SET pulse as discussed above. In addition, these current responses can be used to estimate the SET pulse width for various logic cells quickly, i.e. without performing mixed-mode device simulation. Utilizing the well-organized database of current responses of 55nm generation MOSFET, fast characterization tool (called TFIT [3]) of SET pulse width in cell level works well, where sampling of ion impact conditions for the database generation is carefully designed to reduce the error in compounding expected current response

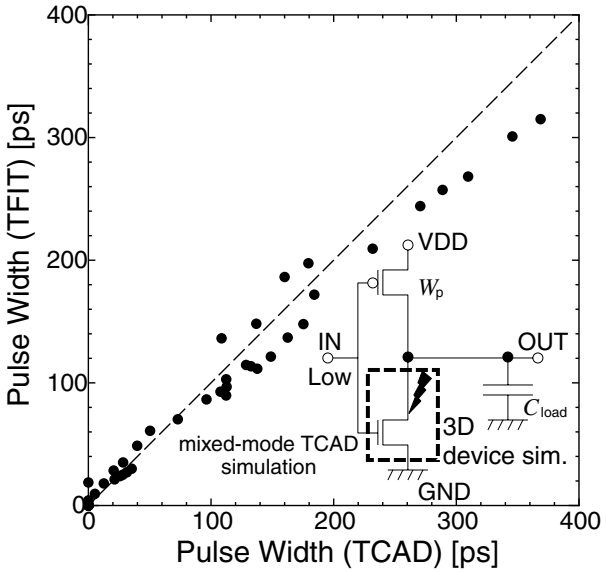


Fig. 12: Comparison between SET pulse width for 55nm inverter cell obtained by TFIT and that calculated by mixed-mode TCAD. Load capacitance, MOSFET channel width and LET are varied.

in the logic cells. As shown in Fig. 12, good agreement of estimated pulse width with that calculated by mixed-mode TCAD is obtained for the inverter cell. This makes the path to the chip-level soft error evaluation [4] available.

IV. Summary

Charge collection current due to the strike of ionized particle onto an nMOS transistor has been analyzed through 3D device simulations. Duration of charge collection, t_{cc}, which is found strongly correlated with the SET pulse width, is extracted from the current response. Through the investigation of the difference between t_{cc} of 90nm nMOSFET and 55nm nMOSFET, it is found that the difference in STI depth and width of p-well contact line between these two generations influences t_{cc} mainly, because t_{cc} is affected by the resistance between the channel and the p-well contact. It is also shown that there is room for reducing t_{cc} and hence SET pulse width by engineering of the well profile.

Acknowledgment

This work was supported by NEDO. The authors would like to thank people in iRoC technologies for valuable discussions and comments.

References

[1] P. Shivakumar et al., *Int. Conf. on Dependable Systems and Networks*, pp.389–398, 2002.
[2] http://www.selete.co.jp
[3] http://www.iRoCtech.com
[4] M. Hane et al., *2008 Int. Conf. on Simulation of Semiconductor Processes and Devices*, pp.365–368, 2008.