Transient 3D Simulation of Single Event Latchup in Deep Submicron CMOS-SRAMs

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***Abstract*—Using transient 3D simulations we investigated single event latchups in SRAMs caused by cosmic radiation. The device structure considered comprises n-well, p-substrate, and source regions of NMOS and PMOS transistors fabricated by means of an industrial 65nm technology. In particular, we analyzed the charge deposition and subsequent current flow initiated by impinging ions for varying impact energy, device temperature, supply voltage and location of the ion impact in order to reveal the details of the failure and eventual destruction mechanisms.**

I. Motivation

Soft errors and other failures caused by cosmic rays are a serious concern regarding the reliability of SRAMs. High energy cosmic rays interact with atoms from the atmosphere, creating a particle shower of muons, electrons, heavy ions, pions, protons, and neutrons [1]. It has been shown that neutrons are the primary source for upsets in electrical circuits, because, being uncharged particles, they can hardly be screened by the package and hindered from undergoing a nuclear reaction with a silicon nucleus in the device interior, leading to spallation products such as of heavy ions as a result. These ions loose their kinetic energy by generating a dense electron-hole plasma inside the device. Irradition experiments were performed at the LANSCE neutron beam facility, because the neutron energy spectrum available there conforms very well to the natural neutron energy spectrum observed at sea level. These experiments revealed a variety of failure processes occurring in SRAM cell arrays. Single event upsets as well as large error clusters were observed (Fig.1). These error clusters were accompanied by a rise in supply current, which is caused by triggering a parasitic thyristor in the SRAM cell array, known as "single event latchup" (SEL). The occurrence of SEL, as observed so far, is not destructive; however, a power down/up reset is required for its correction. But if SRAMs are part of a control unit, SEL threatens the overall system reliability dramatically. We performed transient 3D simulations for a detailed analysis of the complex SEL triggering process. This, in turn, enables the quantitative assessment of the robustness of the devices against SEL without (or at least with a reduced number) of expensive and time-consuming experiments. In this way, design rules can be derived to avoid SEL and, thus, to enhance robustness and reliability.

II. 3D Simulation

For realistic results 3D simulations are indispensable, because 2D simulations are inherently unable to provide a correct description of the real situation and, hence, yield qualitative results at most. Since in 2D a stripe-like geometry is implicitly assumed, the calculated charge generation and carrier concentration overestimates the deposited and injected charge. Furthermore, carrier diffusion is much more realistically modeled in 3D [2].

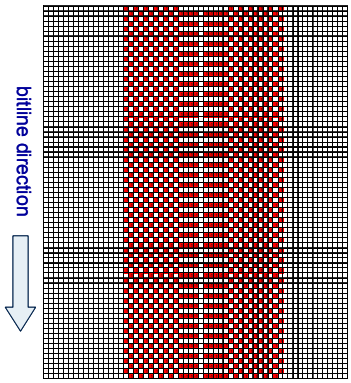

Figure 1. Error cluster caused by SEL as observed in experiments performed at the LANSCE neutron beam facility at elevated temperature.

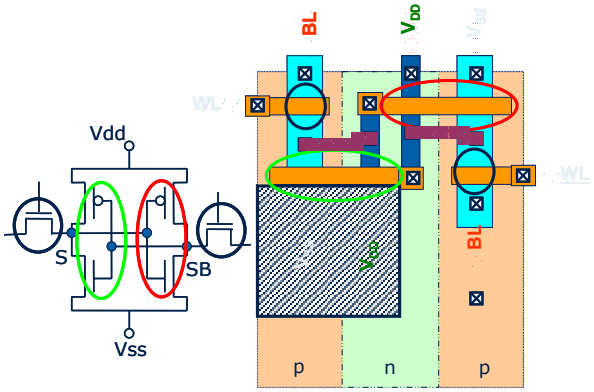

Figure 2. Left: Equivalent SRAM circuit. Right: Top view of a SRAM structure built by the use of an industrial 65nm technology. The black-framed square indicates the region considered in SEL simulation.

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Kreskovsky et al. [3] simulated charge collection of ion induced carriers in a simple pn-diode in 2D and 3D. Both simulations showed a similar qualitative behavior, but the duration of charge collection was significantly longer in the 2D case, while the field distortion was more severe than in 3D. Our simulated SRAMs are fabricated on the basis of an industrial 65nm CMOS process and consist of a periodically self-repeating structure forming the full cell array (Fig.2). A typical failure mechanism works in the way that one of the parasitic thyristors located between the source regions of adjacent NMOS and PMOS transistors is triggered during SEL (Fig.3 left). The simulated device region (Fig.2 right and Fig.3 right) contains all relevant parts of one of these thyristors, but is still small enough to keep 3D simulations within tolerable computation times. The charge injection into the device and the subsequent current flow through the device has been analyzed in detail using the simulation tool SDevice [4].

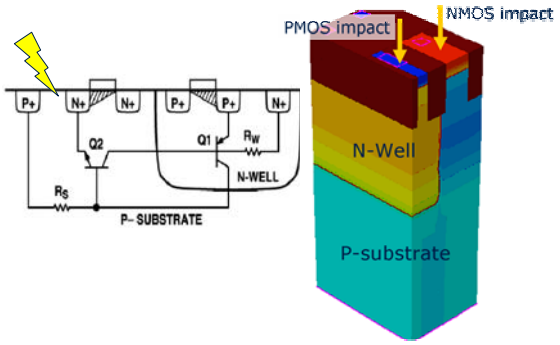

Figure 3. Left: Parasitic thyristor inherently present in a SRAM [8]. Right: Device region considered in SEL simulations.

In order to obtain accurate and realistic simulation results all physical models relevant to SEL have to be included. Since model complexity requires computational effort, we had to find a reasonable trade-off between physical sophistication and affordable computational expense. So mobility was modelled by including ionized impurity and phonon scattering, carrier-carrier scattering, and velocity saturation. For recombination, we referred to the doping-dependent Shockley-Read-Hall-model, Auger recombination and, most important, impact ionization. Furthermore, band gap narrowing for heavily doped regions was considered. The initial deposition rate of the electron-hole plasma G_{ion} caused by the spallation products was assumed as

$$G_{ion}(r,d,t) = G_{LET}(d)*G_t(t)*G_r(r) \qquad (1)$$

Here, $G_{LET}(d)$ denotes the energy loss per unit length at a distance d along the funnel axis, $G_t(t)$ describes the temporal evolution (assumed as Gaussian function), and $G_r(r)$ models the radial distribution of the electron-hole plasma perpendicular to the funnel axis (assumed as exponentially decaying within a characteristic distance of 0.1 µm). The realistic modelling of the initial carrier deposition is still the subject of controversial discussions, and its effect on the simulation results has been studied in other work [5, 6]. We also successfully investigated a similar device structure with the focus on charge retention. Transient 3D simulations of this kind aiming at the analysis of phenomena with steep spatial gradients, which rapidly move through the device, are quite a challenge considering the extremely high computational expense required. A carefully designed mesh is the essential prerequisite for convergence and ensures accuracy and numerical stability. For a satisfactory resolution of the carrier deposition and distribution and the subsequent filamentary current flow through the device, the path of the impinging ionizing particle as well as the neighboring region has to be discretized with a highly refined mesh. Prior to transient simulation, the quasi-stationary operating points of the I-V characteristics have been simulated to verify that the device models provide a realistic and accurate description of the high-resistive state. All these device simulations were supported by Monte-Carlo simulations using SRIM [7] in order to obtain accurate data of the energy loss function $G_{LET}(d)$ of the various spallation products generated by the nuclear reaction between the impinging cosmic neutron and a silicon nucleus of the device material. Employing the linear energy transfer approach (LET), the initial charge deposition of a SEL process was determined for all relevant neutron energies in the range of meV to GeV.

III. Results

The simulations reveal that and how SEL can occur in 65nm SRAMs. Our simulation approach proved to work properly and yielded an accurate time-dependent 3D visualization of this spectacular event (Fig.4). It showed that certain preconditions have to be met in order to trigger SEL: We identified the threshold LET, the threshold temperature, the supply voltage and the most sensitive location of neutron impact. The LET of the spallation products together with the length of the ion track determines the total electron-hole plasma charge deposited in the device.

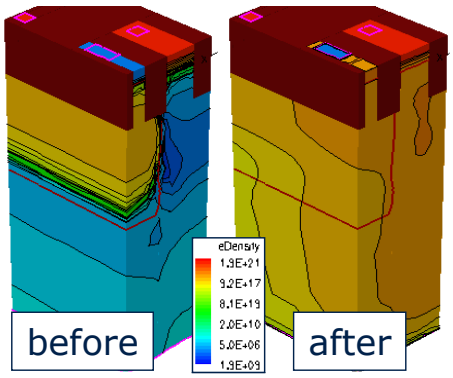

Figure 4. 3D Simulation: Electron density before current injection and after SEL triggering.

Above a certain threshold LET, the current induced by this charge becomes large enough to trigger the SEL process (Fig.5). For ions whose LET lies below this threshold the device returns into its original high resistive state. A decisive parameter is the lattice temperature, considering that SRAMs are also employed in control units that are operated in high-temperature environments. Various isothermal simulations have been performed with temperatures ranging from 300 *K* to 450 *K*. We observed a strong temperature-dependence of SEL, even if the LET is kept constant (Fig.6). Our finding is that with rising temperature the threshold LET decreases. Since the origin of SEL is a ignited parasitic thyristor, the saturation current increases with rising temperature, conforming with our

simulations. Since the experiments for model validation were carried out at room temperature, we paid special attention to this situation. We considered the maximum LET possible in silicon and found that, at room temperature, no SEL can occur in this type of SRAMs (Fig.7).

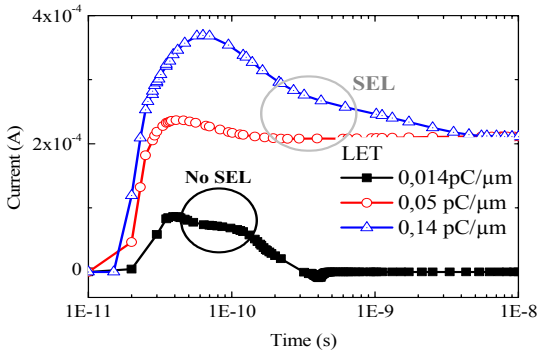

Figure 5. Transient currents through the source of the PMOS transistor after neutron impact for varying LET at 330K.

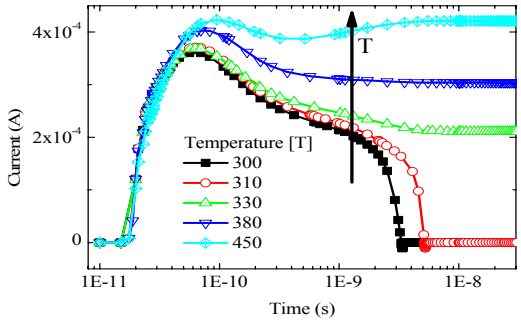

Figure 6. Sensitivity of SELwith respect to varying device temperature at constant LET.

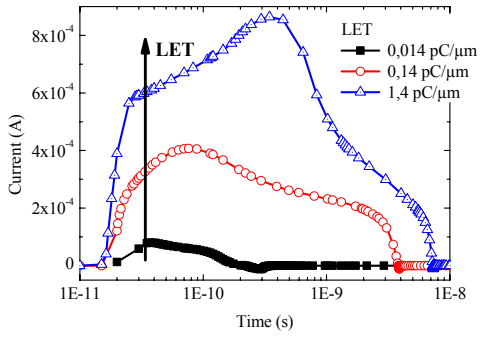

Figure 7. Transient PMOS source current at room temperature for varying LET: No SEL observed!

Increasing the LET alone causes a longer duration of the high current phase. This conforms with our experimental findings at LANSCE. Also the level of the supply voltage has a significant impact on the occurrence of SEL. Only if the voltage applied to PMOS and n-well exceeds the thyristor´s holding voltage, the current will continue to stay at a high level after latchup triggering, otherwise the device structure will return to its high resistive state. LET and device temperature were kept constant for these investigations, while the voltage was varied from 0.8 V to 1.4 V, corresponding to the minimum and the maximum voltage applied to this type of SRAM.

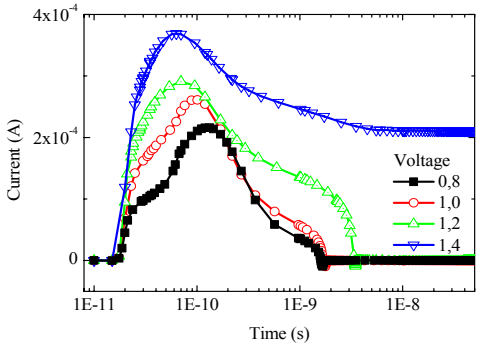

Figure 8. Transient PMOS source current for varying supply voltage. For small voltages below the holding voltage no SEL occurs at 330K.

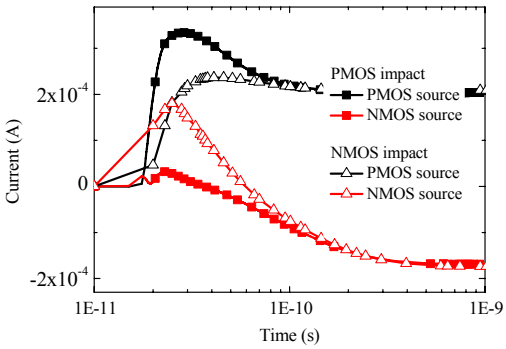

Figure 9. Transient current through the sources of PMOS and NMOS transistors at 330K for varying location of the neutron impact.

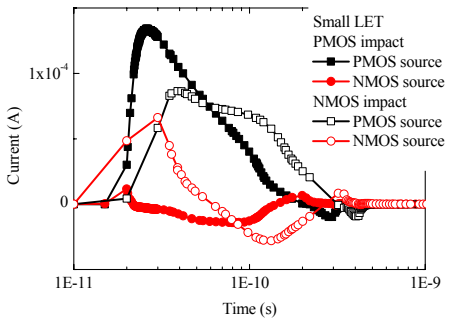

Figure 10. Transient current through the sources of PMOS and NMOS transistors at 330K for varying location of the neutron impact in the sub-threshold LET regime.

At 330K only a supply voltage above 1.4 V was able to sustain SEL (Fig.8). For smaller voltages the device returned into its overall high resistive state. Also simulation with temperatures as high as 450K did not show latchup for small voltages; SEL was only observed above a threshold of 1.2 V. Hence, we conclude that SRAMs in low power operating mode (retention) are not endangered by SEL even at higher temperatures, while at normal operating mode, when the supply voltage is higher, the SRAM is indeed threatened by SEL. The location of the impact of the neutron is also of major importance. It showed that in each of the two parasitic bipolar transistors SEL can be triggered for the same LET (Fig.9). However, the details of charge collection process look different, which indicates that the threshold LET in the PMOS and in the NMOS transistor are different. Analyzing subthreshold LET in both the PMOS and the NMOS transistor reveals large differences in the charge collection (Fig.10). If the neutron impact occurs in the PMOS, the device quickly returns to its high resistive state after charge collection is finished. If the impact happens in the NMOS, both parasitic bipolar transistors are partially switched on, but they do not attain the ignition treshold of the parasitic thyristor structure. In order to explore the radiation sensitivity of all individual parts of the device, a multitude of simulations were performed with varying tracks of the impinging neutron parallel to the device surface and varying penetration depth. (Fig.11).

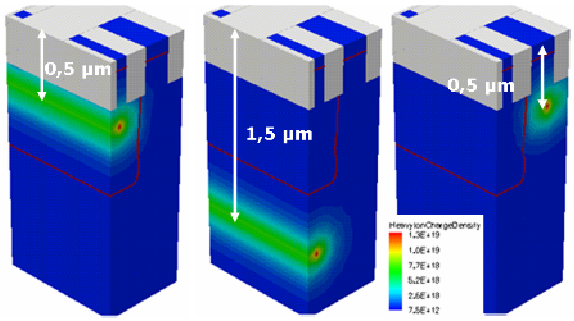

Figure 11. Ion impact parallel to the surface. Injection beneath the PMOS source at 0.5µm and 1.5µm and beneath the NMOS source at 0.5µm.

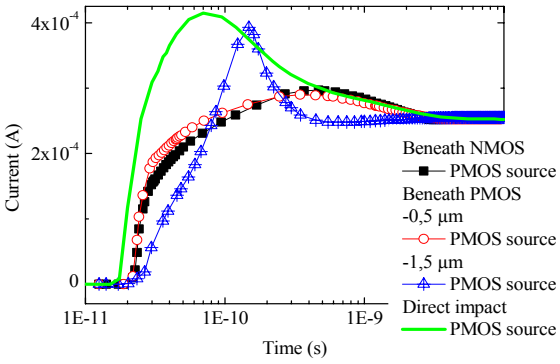

Figure 12. Ion impact parallel to the surface at 330K, beneath NMOS source at 0.5µm depth and beneath PMOS source at 0.5µm depth and 1.5µm depth.

This included simulations with ion impact at 0.5 µm beneath the surface of the NMOS source and the PMOS source, respectively, as well as ion impact at 1.5 µm beneath the PMOS source to study the influence of impact depth. Comparing "shallow impact" in the depleted regions around the sources of NMOS and PMOS with impact deeply underneath the sources, it shows that charge collection is significantly slower in the latter case, because charge is primarily conveyed by the action of diffusion, whereas it is drift in the electric field in the depleted regions that drives current flow in the case of shallow impact (Fig.12) [9]. The current peak originating from a "deep impact" in 1.5µm depth is significantly delayed, because the charge carriers are deposited farther away from the contact and, hence, need a longer time to diffuse to the contact. If the injected charge is not large enough to trigger SEL, the structure returns to its high-resistive state as it is the case for "shallow impact".

IV. Conclusion

We demonstrated that single event latchup in deep sub-micron CMOS-SRAMs can be realistically reproduced by virtual experiments using computer simulation. Comprehensive investigations were made for analyzing the effect of varying LET, temperature, bias voltage, and impact location on the SEL mechanism, with emphasis on effects. Considering that future computer technologies will reduce the currently still excessive computational expense, “virtual sensitivity tests” are likely to become a routine activity in the development of future CMOS technologies.

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