CAD based Interconnect Analysis

J. G. Rollins
Implementation Group, Synopsys
700 E. Middlefield Rd, Mountain View, CA 94043

***Abstract*—This paper provides an introduction and overview of interconnect modeling in integrated circuits. Resistance, capacitance, inductance and mechanical analysis are discussed.**

Keywords-Inteconnect, capacitance, resistance, inductance, parasitics

I. TECHNOLOGY ISSUES

Figure 1 shows a simplified cross section of interconnect in a 45 or 30nm process. Chips can have 10 layers of metal and more than 30 nearly planar dielectric layers. From 20% to 40% by volume of dielectric is made up of "low-k" material. Low-k meaning that $\varepsilon \sim 2.5$. The lower metal layers are thinner than the upper layers and the percentage of low-k is also lower. Metal regions have a slight taper typically less than 10 degrees. The etch stop regions have $\varepsilon \sim 5$

Some damage occurs to the low k material when the metal regions are inserted. This damage creates a small region with increased ε around the metal. Variations in metal density cause different etching rates during CMP (chemical-mechanical-polishing) and as a result the overall thickness of the metal and surrounding dielectric varies as the metal density changes.

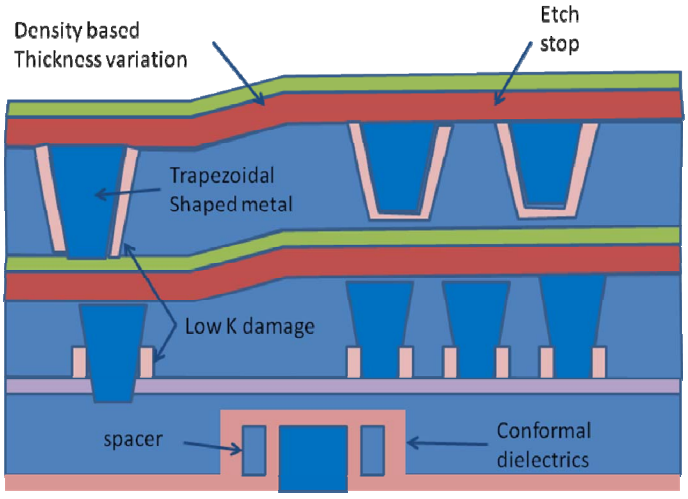

Figure 1. Technology cross-section showing dielectric.

CMP processing causes the tops of the metal to be aligned with the dielectric interfaces, however the position of the bottom of the metal can change relative to the dielectric interfaces. The bottom depth therefore becomes a function of the conductor width. These features are exaggerated in Figure 1 for emphasis. The damage regions typically are 10nm thick, the layer thickness variation less than 20% and the metal taper is less than 10 degrees.

Photolithography limitations now require that layouts use rectilinear geometries. This actually simplifies the analysis problem, particularly for capacitance analysis. Since layouts are made up of many rectangular conductors, a good way to characterize the size of a layout is in terms of the number of rectangles or "boxes" that it contains.

Copper is now used for most interconnects. Since Copper can migrate and contaminate the silicon the copper is encased within a barrier layer of Ti or Ta. At 22nm the metal width and height are expected to be 35nm and 70nm respectively.

II. THREE SIMULATION PHASES

In the IC design process, three phases can be identified where simulation can be of value. These are process development, cell level analysis and final verification.

The goal during process development is to develop the actual silicon processing steps. Attention is focused on reliability, maximizing yield and performance. Design rules are also developed at this stage. Very detailed TCAD simulations are performed on individual transistors. In the interconnect small sections or even just 2D cross sections are simulated to characterize the interconnect in terms of capacitance per unit length or resistance as a function of conductor width. Studies on electromigration and dielectric breakdown would be conducted at this point. Measurements are performed on test chips containing arrays of parallel metal lines for capacitance, strings of vias for resistance or ring oscillators or small cells to measure delays.

The purpose of cell level analysis is to develop accurate models of electrical blocks that will be used repeatedly in a chip. Cells can vary in size from a few transistors, for example a bit cell in an SRAM with 6 transistors, to a small memory containing several hundred thousand transistors. Since cells are fairly small and they will be used many times in the life of a technology, it is easier and more worthwhile to analyze them in high detail. Cell designers may therefore wish to extract the capacitance of all the nets in the cell with a field solver. Certain blocks like IO cells may get special analysis like ESD. Analysis using the optical image is also possible (see section

VII). Circuit simulations would most likely be performed using full SPICE accuracy.

Verification is done to make sure that everything will work when all the pieces are connected together. The design size during verification is the largest (millions of transistors). It is no longer possible to extract the capacitance all of the nets using a field solver, but a few critical nets may still be extracted with a random walk solver. The design will now contain longer busses and inductance and resistance may be important issues. A fast-SPICE simulator will probably be used for the circuit analysis.

III. CAPACITANCE EXTRACTION

The purpose of capacitance extraction is to calculate the parasitic capacitances that are always present. For integrated circuit analysis simple linear static capacitance is all that is required. The LaPlace equation is solved for the electric potential:

$$\nabla \bullet \varepsilon \nabla V = 0; \quad D = -\varepsilon \nabla V; \quad Q = \oiint D; \quad Q = CV \quad [1]$$

Dirchlet boundary conditions are used on metal regions and Neuman or Dirchlet boundary conditions are used on outside surfaces. For bit cells Neuman boundaries may be placed along the edges of the cell and used to simulate a cell in an array environment. For most other applications the boundaries are placed far enough from the conductors so as not to have any effect. Usually 10 microns is "far enough" for modern technologies. After the potential distribution has been calculated the electric flux vector D is integrated on or around the surface of conductors to obtain the charge. Since capacitance is linear, the capacitance is equal to the charge.

The permittivity for commonly used material ranges from 2.0 (low-k) up to 7.5 (SiN) although air gaps can be used and high capacitance films with ε up to 40 can be used in memory applications. For the BEM and Random Walk solvers, complex dielectric structures create more difficulties than complex metal regions.

All field solvers extract a single row of the capacitance matrix at a time. Therefore the extraction effort is proportional to the number of electrodes (or nets) to be extracted.

Floating metal "fill" is commonly used in modern processes to insure the planarity of the metal layers. Some regions of the chip may contain more fill boxes than actual conductors. The capacitance extraction algorithm therefore needs to be able to handle large numbers of pieces of floating metal efficiently.

The fundamental problem being solved has not really changed over the past 20 years. However with increasing chip complexity greater accuracy is needed. In addition, interconnect has a greater impact on over performance than before so capacitances need to be extracted with greater accuracy. Customers have high expectations on accuracy. Pattern based LPE extractors claim to offer accuracy of 5% or better so a field solver needs to give accuracy of 1% or better to be useful.

A. Volumetric methods

The volumetric methods include finite difference, finite volume and finite element. All require that a suitable volume filling mesh be constructed. The discretization is straight forward and a banded sparse symmetric positive definite system results. For 3D simulation an iterative linear solver similar to ICCG must be used.

Floating electrodes can be addressed by adding an additional unknown potential and equation to the system for each floating electrode. The new potential represents the voltage on the floating electrode (all nodes within the floating electrode are set equal to this potential). The new equation represents the sum of charge on the floating electrode which is set to zero.

The most difficult part of the analysis is mesh construction. Fortunately due to the rectilinear nature of most interconnect structures simple tensor product meshes are quite successful. Tensor product meshes require very little data storage and can be generated in a fraction of a second making it possible to simulate 50e6 mesh points on an Intel work station. The Raphael program uses this method and has been in use for almost 20 years.

For non rectilinear geometries a tetrahedral mesh offers greater accuracy and the possibility of reduced mesh counts. However the mesh generation time often greatly exceeds the solve time and the data requirements during mesh generation limit the mesh to 5e6 points.

The "bottom line" is that for the target accuracy of 1%, with modern work stations analysis using volumetric methods is limited to about 100 boxes so the technique is only useful for test structures or characterization during process design.

B. BEM (Boundary Element Methods)

Boundary element methods only require that mesh be generated on the surfaces of conductors and surfaces on non-planar dielectric interfaces. Typically these surfaces are divided into little rectangular or triangular patches called panels. The number of panels used controls the accuracy. To obtain accuracy in the 1-2% range around 100 panels are needed for each conductor "box".

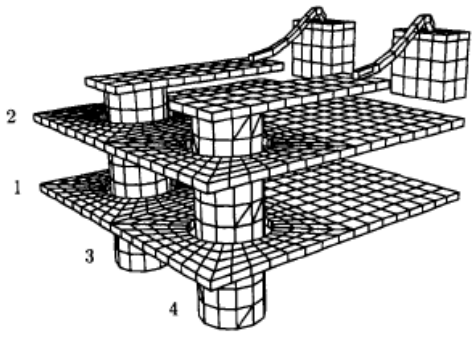

Figure 2: Panels used in BEM. Fig from [1]

The following equation is the basis of the BEM. Ψ(r) is the known potential on the surface of the conductors. σ(r) is the charge density that we are solving for. G(r,r') is the

Green's function which relates the potential at a point to the charge on the surrounding points.

$$\Psi(r) = \int \sigma(r')G(r,r')da \; ; \quad G(r,r') = \frac{1}{4\pi\varepsilon \, \| r - r' \|} \; [2]$$

Each panel has its own value of σ and likewise the integration is performed over each panel. Therefore each panel results in one unknown charge value and one equation which must be solved in linear system (higher order integration methods can also be used). Once that all the σ values have been determined they are summed over the surfaces of the electrode giving the electrode charge and hence the capacitance.

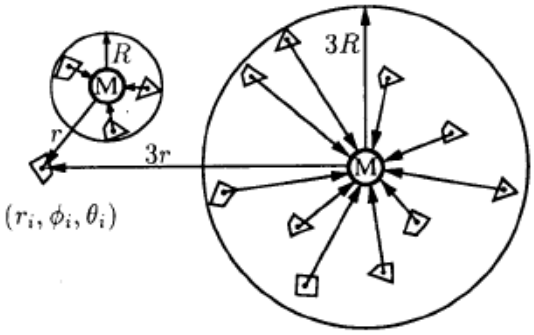

Figure 3. Multipole expansion. Fig from [1]

With the BEM method every panel is coupled to every other panel through the Greens Function. The resulting linear system has a dense matrix structure which is impractical to solve directly for any meaningful problems. Several methods have been developed to work around this limitation, the two best known are the multipole method used in FASTCAP [1] and hierarchical BEM [2]. These methods take advantage of the fact that panels at a distance can be grouped together as a set and treated together, effectively reducing the size of the problem. Memory requirements for the BEM are given as approximately 1Kb/box [3], so the BEM is limited to cell level analysis.

If the dielectric is non-uniform but consisting of planar "slabs" then the Greens function can be modified to include the effects of the dielectric (at additional computational cost). If the dielectric is nonplanar, then the dielectric interface must be discretized into panels and additional equations and unknowns added to the linear system.

C. Random Walk Method

The random walk method calculates capacitance using recursive application of a Greens function first to find an unknown potential from known potentials and then to find the electric field from potential [4]. See Fig 4. A Gaussian surface (GS) is first built around the conductor of interest. Next a point is chosen on the GS and a walk weight is calculated based on the area of the GS, the distance from the point on the GS to the surface of the electrode (d1) and an electric field Greens function. A random walk, which consists of a sequence of hops is performed from the point. Each hop jumps from the center to the surface of the largest cube of homogenous material that can be constructed around the hop starting point. If the hop lands on a fixed voltage conductor the capacitance sum for the conductor is incremented and the walk is terminated. If a hop lands on a floating conductor, a new GS is generated around the floating conductor and the walk continues from that GS. If the hop lands in the dielectric then more hops are performed until a conductor is reached. Random walks are performed until the capacitance sums converge, millions of walks may be needed per net with an average of around 10 hops per walk.

Dielectric interfaces are handled in different ways by different software developers. It is possible to handle the dielectric interfaces exactly but in a modern chip with so many interfaces the analysis becomes too slow. Approximations can be introduced to speed up the analysis usually at the penalty of 1% or 2% loss in accuracy.

The random walk method has the lowest memory requirement, no meshes are generated, only the conductor and dielectric geometries need to be stored. Typically less than 50 bytes/box are all that is needed. The memory efficiency of the RW method makes it possible to analyze designs with 1e8 boxes or 1e6 nets on a workstation. Under "good conditions" RW solvers can extract 100,000 nets to 1% accuracy in less than 1 day. (Note that run time is proportional to 1/Accuracy^2). In addition the RW method is very easy to parallelize on multiple cores or over a network of work stations.

The main drawback of the RW method is that it is best at extracting total net capacitance. If a coupling capacitor which is a small part of the total net capacitance needs to be extracted with high accuracy, this capacitor will take a long time to converge. This may limit the usefulness of RW in certain analog applications. Customers also often find the statistical nature of the results confusing.

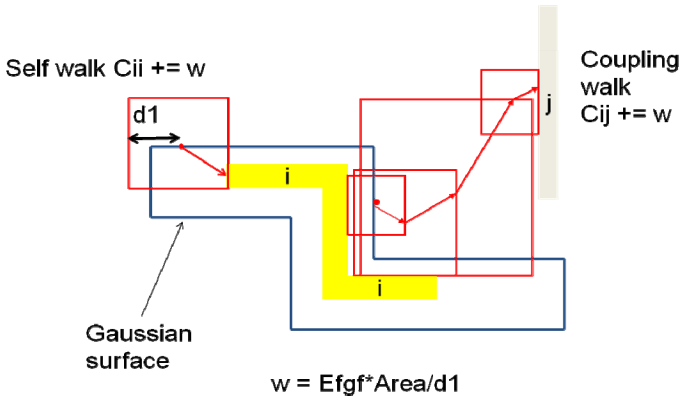

Figure 4. Random walk sequence.

D. Interactions with Device Models

Transistor level models (SPICE) contain voltage dependent capacitances between the gate, source, bulk and drain. However gate, source and drain are also capacitively coupled to conductors outside of the transistor so to completely model the interconnect the gate, source and drain must also be included when extracting interconnect capacitance. Some

interconnect capacitances overlap with the device capacitances (see Fig. 5) and "double counting" of capacitors could occur without careful modeling.

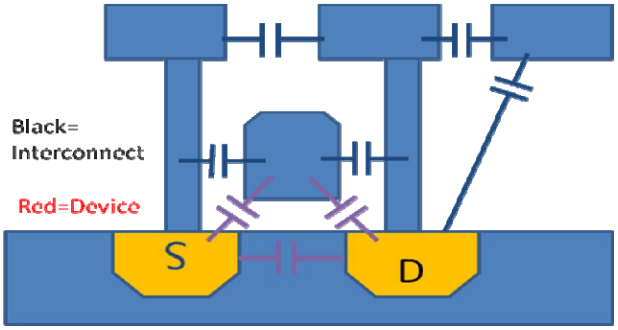

Figure 5. Cross section showing device and interconnect capacitances.

Software vendors have each developed their own method of "capacitance accounting" to handle this. Variations between the methods used cause differences when comparing LPE tools. New methods will need to be developed to support FINFET and pillar transistors.

IV. Resistance Extraction

The purpose of resistance extraction is to extract the parasitic resistance of the metal conductors. The system of equations is very similar to that for capacitance, the main difference is that the conductivity within the conductor is many orders of magnitude greater than within the insulator.

$$\nabla \bullet C_e \nabla V = 0; \quad J = -C_e \nabla V; \quad I = \oiint J; \quad RI = V \text{ [3]}$$

As a result conduction within the insulator regions can be ignored for all but a few special cases. Only the conductors need to be discretized. During process development a method like finite element can be used and the individual conductors can be solved in isolation. This analysis can be combined with mechanical analysis and reliability studies conducted (see section VI). As if this writing I am not aware of any commercial software tools specialized for resistance analysis during the process development phase. For cell level analysis and verification, since conductors tend to be long and thin, methods similar to square counting work well. Some LPE tools do create meshes of resistors to analyze square shaped regions like MOSFET source and drains.

In modern technologies as metal lines become thinner it is important to consider the effects of cladding layers and scattering that occurs at the surfaces of the conductance and at grain boundaries. The result of this is that the resistance per square becomes a strong function of the width of the conductor as shown in Figure 6 for Cu lines [5].

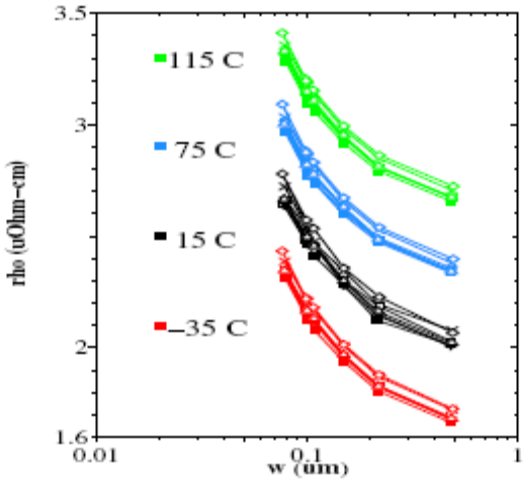

Figure 6. Resistivity of Cu lines as a function of width and temperature. Fig from [5].

Recently it has been found that self heating effects within conductors may be important. Joule heating caused by current flowing within the conductor causes its temperature to rise. The increased temperature causes the resistivity of the material to increase. Changes in resistivity up to 35% were seen [6].

V. Inductance

Inductance is always present as a parasitic. Inductance has the undesirable effects of introducing signal delays and noise. Parasitic inductance can interact with parasitic capacitance and cause "ringing" during signal transitions. Mutual inductance can create coupling between signal lines which can potentially cause false triggering. The skin effect can increase the effective resistance of conductors causing further delays. Inductance can be neglected for normal signal nets, however for signal busses and clock nets inductance can increase delays by 20% in modern 45 nm technologies.

For design of ICs outside of microwave applications inductance can be extracted independently of capacitance. We are not trying to create transmission line models. The inductance is a function only of the conductor geometry, dielectrics do not have an effect. The primary difficulty is that inductance calculation requires that current flow in a closed loop and when calculating the inductance for an individual conductor the return path is not known.

To solve the problem of the unknown return path, the concept of partial inductance was introduced by Rosa in 1908 [7] by assuming that the return path is infinitely far away. In 1972 Ruehli [8] created a method of analysis. The conductors are represented as rectangular boxes. Each box has a series inductive and resistive component. Analytic formulas are used to calculate the partial inductance between each pair of conductors. These formulas depend on the lengths and relative angle and distance between each pair of boxes. The skin effect can be modeled by discretizing each physical conductor

into multiple concentric parallel boxes see fig 7. Ground planes can be modeled using a rectangular grid of boxes.

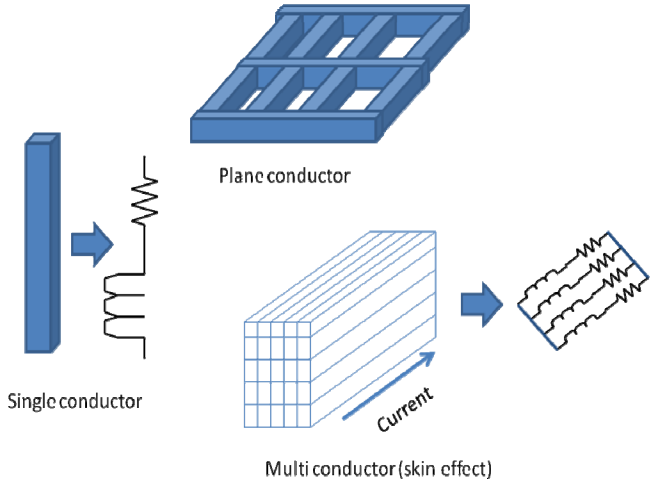

Figure 7. Representation of conductors for inductance extraction.

The network of resistors and conductors can now be combined with the other circuit elements (capacitors, transistors etc.) and analyzed using normal circuit simulation techniques. The problem is that every box element is inductively coupled to every other box element resulting in a dense circuit matrix. A circuit simulator like SPICE which is geared towards sparse problems will have unacceptable performance for any useful problems. Attempts to simplify the problem by eliminating numerically small elements from the L matrix can result in instability during circuit simulation.

In 2000 Devgan [9] introduced the "K-based" method or "reluctance". This method takes advantage of the fact that the K matrix, which is the inverse of L is "more sparse" than L, which means that when K is used, conductors that are farther away have less effect. The K matrix can be constructed by selecting only conductors close to the target conductor, calculating L and then inverting to find K. The K matrices from different sections of the conductor are then summed together to obtain a global K matrix with sparcity pastern similar to the capacitance matrix.. Circuit simulators have been developed (both time and frequency domain) which can accept the K matrix directly [10].

VI. Mechanical Analysis

Mechanical analysis is employed during process development and is usually concerned with the reliability of the interconnect. Interconnect systems are made up of materials with different thermal expansion coefficients. Since the materials are deposited at temperatures different from the operating temperature, mechanical stress is "built into" the system. If the stress becomes too high it can cause cracks to form. low-k material is more porous than traditional oxide and more susceptible to cracking.

Figure 8 shows calculated stress in low-k dielectric. A 3D finite element model was used. The Cu lines (white regions) are 140nm wide and 310 nm thick. The stress-free temperature is 250C. The stress is concentrated between the corners of the metal lines. The peak stress is about 140MPa [11].

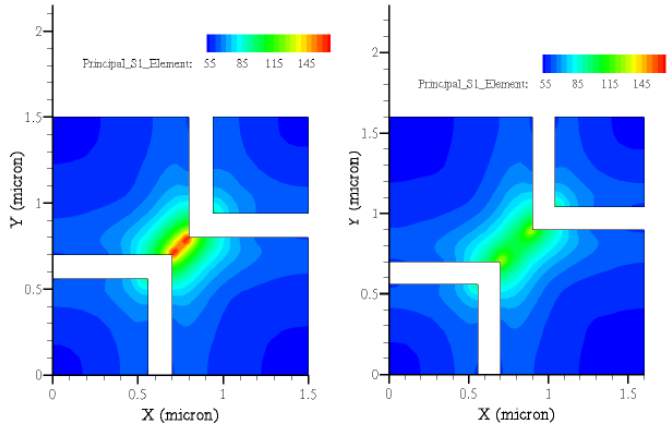

Figure 8, Stress in low-k dielectric due to CTE mismatch. Fig from 11.

Mechanical stress in conductors can cause material to migrate forming voids which cause electrical "opens". Electrical currents transfer momentum to atoms in conductors causing the atoms to move, again forming voids or else form extrusions which can cause shorts. Modern interconnects are more susceptible to these problems because the conductor size is smaller so there are fewer "grains" of material and also because the barrier layers which encase the copper create sites where voids can "nucleate" or begin forming. Finally the low-k dielectric offers more thermal resistance.

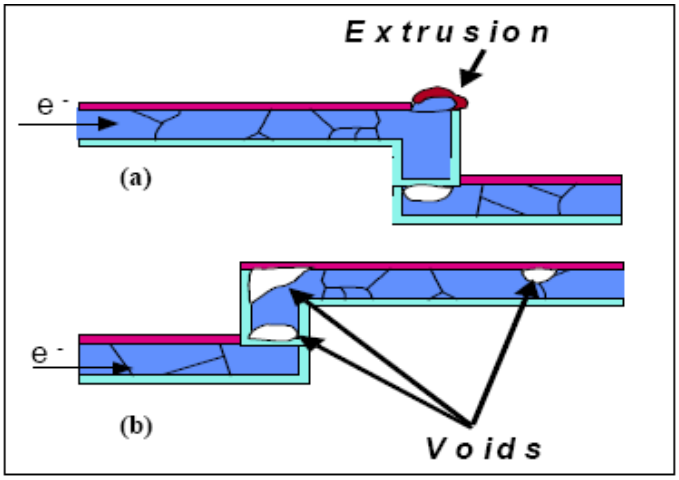

Figure 9. Voids and Extrusions. Fig from [9].

One method of analyzing void formation is to treat the concentration of material at a given location (or alternately vacancies) as a continuous variable N(x,y,z). N obeys a continuity equation:

$$\frac{\partial N}{\partial t} + \nabla(J_c + J_t + J_s + J_n) = 0 \qquad [4]$$

$$J_c \alpha\, N J_e; \quad J_t \,\alpha\, N\nabla T; \quad J_s \,\alpha\, N\nabla\sigma; \quad J_n \,\alpha - \nabla N$$

The four material flow (J) terms are Jc electrically driven term, driven by the electron current density Je, Jt driven by the temperature gradient, Js driven by the gradient in hydrostatic stress σ and Jn driven by the material gradient.

The electrical current density can be calculated by solving the current density equations [3] given earlier. The temperature distribution T can be found by solving the heat equation including Joule heating caused by currents in the conductors.

$$\nabla \bullet C_t \nabla V = J_e \bullet J_e / C_e \qquad [5]$$

Ct and Ce are the thermal and electrical conductivity of the materials. The hydrostatic (mechanical) stress can be calculated from the Navier equation (greatly simplified here)

$$\nabla\sigma \;=\; f(N)$$

$$\sigma_0 = C_{te} C_m\, (T - T_0) \qquad [6]$$

Cte is the coefficient of thermal expansion. Cm represents the elasticity of the material. To is the fabrication temperature. Therefore σo represents the stress that is "built into" the structure when it is fabricated. Function f(N) accounts for the fact that movement of the material along grain boundaries will change the stress distribution. This problem is very complex and several approaches have been developed over the last few years to treat it [12, 13]

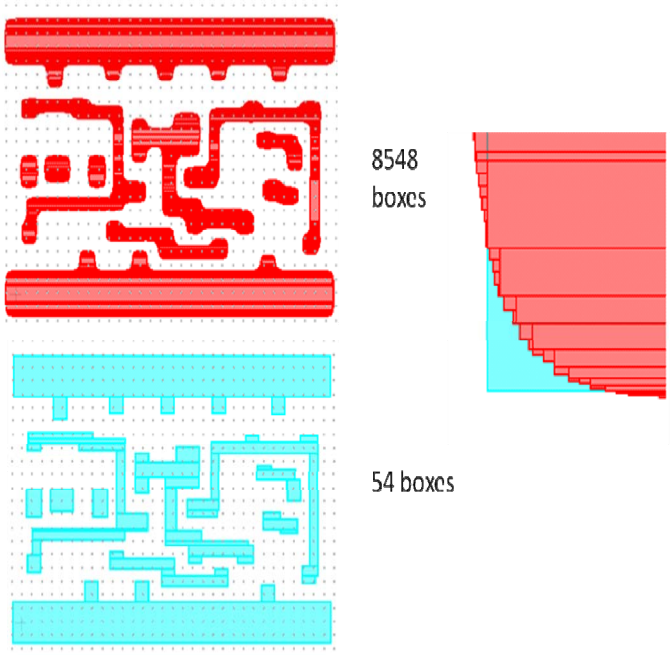

Figure 10, Original layout and layout with defocus.

VII. USING THE PRINTED IMAGE

Interconnect analysis is normally done using GDS as the input. Special "EVWS" (Etch –vs- width and spacing) are applied to compensate for photolithography and etching effects then the boxes are extruded to create 3D geometries. However the resulting geometries still use simple rectangles where as the actually printed patterns will have smoothly rounded corners.

An alternate approach is to use optical and etching models to generate 2D contours of the printed image can. (Defocus and optical proximity effects can be included). The 2D contours can then be extruded to create a 3D model and the resistance or capacitance of the model can be extracted.

This procedure was used on the layout shown in Figure 10. The procedure is computationally expensive, it takes 8548 rectangles to represent the smooth image but only 54 to represent the original. Run time using a random walk solver is about 10X longer for the smooth image. The average difference in total net capacitance between the two images was 5% with the largest difference being 13%.

This technique would not be practical during the verification phase but may be worthwhile for analysis at the cell level. Implications for resistance extraction are also important since "pinched" conductors with high resistance section have been observed in the optical image [14].

VIII. CONCLUSIONS

Interconnect analysis is a critical part of the IC design process. Electrical extraction techniques have kept pace with the complexity of the problem. Opportunities exist for analysis of interconnect reliability and most recent research has been in that area.

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