Modeling the Effect of Conduction Band Density of States on Interface Trap Occupation and its Influence on 4H-SiC MOSFET Performance

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***Abstract*— Interface traps play a crucial role in determining total mobile charge available for conduction and also in determining low field mobility in 4H-SiC MOSFETs. They are important in determining current and transconductance in these devices. Accurate calculation of the interface trap density is essential for characterization of transport in 4H-SiC MOS devices. Typical conduction band edge density of states for traps can reach values comparable to electron states in the conduction band. Therefore, it is necessary to include traps located in the conduction band while calculating occupied trap densities. Using DOS calculated by DFT method, we show that trap and electron DOS are comparable up to 200meV inside the conduction band, and use this to calculate occupied trap densities and currents for 4H-SiC MOSFETs. Validation of this occupation model is achieved by excellent comparison of simulated and measured current-voltage characteristics for MOSFETs with a wide range of channel doping values.**

Keywords-4H-SiC MOSFET; DFT-DOS; interface traps; current degradation;

I. INTRODUCTION

Silicon Carbide (SiC) has a wide bandgap, high breakdown field, good thermal conductivity, and a native oxide, making it very attractive for design of high power high temperature electronics. However, excessively large densities of interface traps distributed over the 4H-SiC bandgap pose a serious concern for reliable and reproducible designs of SiC MOS devices [1, 2]. Accurate evaluation of the density, location and energy-distribution of these interface traps is very important for designing complex circuits using SiC devices. The density of states for the traps near the edge of the conduction band is so large, that they become comparable to the conduction band density of states for electrons. This implies that a conduction

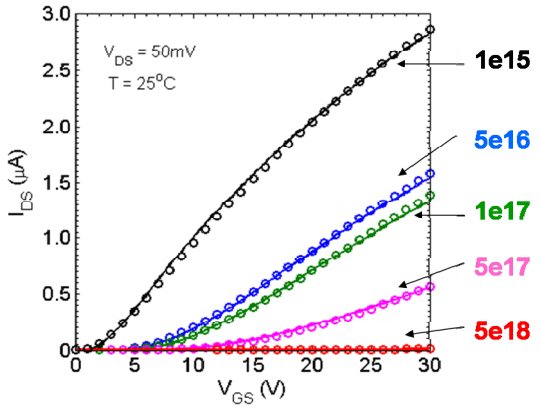

Fig. 1 (a) Simulated (circles) and measured (lines) linear I_D-V_{GS} characteristics of 4H-SiC MOSFETs with various channel doping values (10^{15} to 5×10^{18} cm^{-3})

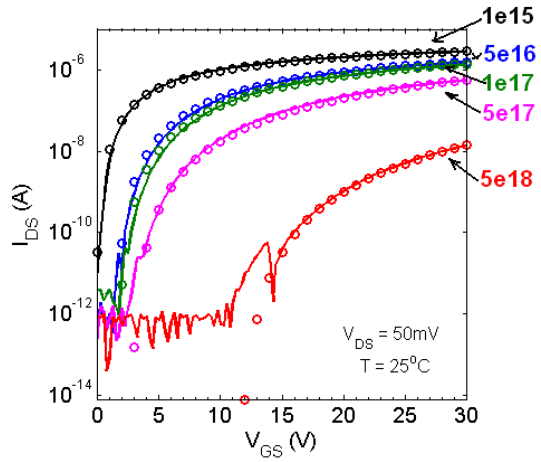

Fig. 1(b) Simulated (circles) and measured (lines) sub-threshold I_D-V_{GS} characteristics of 4H-SiC MOSFETs with various channel doping values (10^{15} to 5×10^{18} cm^{-3}). Simulated I-V data shows excellent agreement with experiment.

band electron will have similar probabilities of occupying a conduction band trap or a conduction band state. We investigate occupation of these band-edge trap states in 4H-SiC MOSFETs and analyze their effect on current-voltage characteristics using our novel device simulator, which is verified by experiments as shown in Fig. 1(a) and Fig. 1(b). We employ a combination of drift-diffusion based device modeling and DFT based MC calculations to calculate occupied trap density.

II. DFT Calculations for Conduction Band Density of States

The DFT-DOS based method for calculating electron and hole dispersion relations differs from other standard Monte Carlo (MC) techniques that employ the full 4*H*-SiC spectra that are calculated for example, using the tight-binding approach or the empirical pseudopotential method (EPM). Both these methods rely heavily on experiments for adaptive calibrations. For instance, while EPM is good at predicting band structure details at conduction and valence band edges, there is not enough experimental data to test its validity far from the bandgap. Experimental data are usually limited to band minima/maxima or curvatures of the conduction and valence band edges. It is especially difficult to obtain details of the energy-momentum relations for a wide range of energies, and for high kinetic energies that electrons and holes possess while undergoing impact ionizations. Additionally, it requires consideration of many non-isotropic (k_x, k_y, k_z dependent) conduction and valence bands for 4*H*- and 6*H*-SiC polytypes to obtain high field transport characteristics.

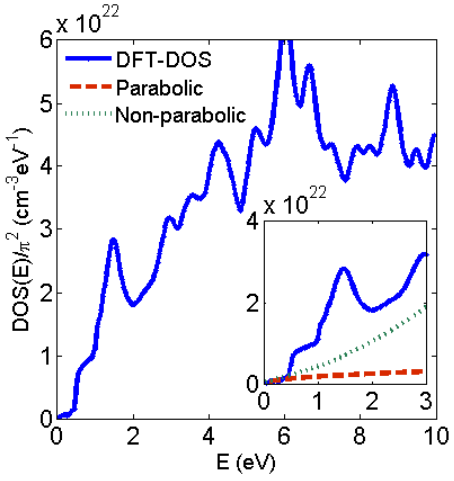

Fig. 2. 4H-SiC conduction band density of states calculated using DFT-DOS method.

The DOS curves are extracted from DFT calculations up to 16 eV above the conduction band and below the valence band. To obtain these curves, the DFT simulation is performed using the linear density approximation and the full-potential linearized augmented plane wave method [3]. To obtain an energy versus average momentum relation, we start with the three-dimensional DOS expression $k^2(dk/dE)=\mathrm{DOS}(E)$. Multiplying both sides by dE, and integrating the left and right hand sides in momentum and energy respectively, yield an average momentum for a given energy. This momentum is proportional to the integral of the DOS curve from the conduction band minimum to that energy E as

$$\left[\langle k\rangle = \left(\left|3\times\int_{E_{\min}}^{E} DOS\ (E)dE\right|\right)^{1/3}\right].$$

Fig. 2 shows the DFT-DOS curves we use along with the calculated electron energy spectra. For the conduction band, we also show DOS curves due to a one-band parabolic dispersion relation with $m^*=0.4\times m_0$, and a one-band non-parabolic dispersion relation with $m^*=0.4\times m_0$ and $\alpha=0.5$. Here the effective mass $m^*=0.4\times m_0$ is found by fitting the lower part of the energy-momentum DFT-DOS curve to a second degree polynomial.

III. Interface Trap Occupation Model

The occupied acceptor type interface trap density (N_{it}) depends on trap density of states (D_{it}) and the Fermi level at the interface. A typical D_{it} profile for 4H-SiC MOSFET is shown in Fig. 3.

The occupation probability is determined by the

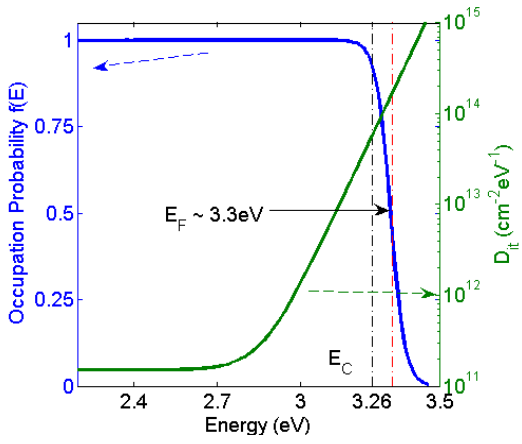

Fig. 3. Interface traps DOS and the occupation probability near the conduction band edge in a test 4H-SiC MOSFET.

electron concentration at the surface. Classical solution of the electron concentration in the SiC MOSFET gives the maximum at the interface leading to a large trap occupation. If quantum confinement is considered in the channel, then the peak of the electron concentration is away from the interface, which may lower the number of occupied traps [4].

If the conduction band density of states for electrons is significantly larger than the band-edge interface trap density of states, then the occupation of interface traps is calculated by integrating the product of the distribution function and the trap density of states from the neutrality point to the conduction band (CB) edge. This is the case for Silicon MOSFETs. But, in the case of 4H-SiC MOSFETs, the observed band-edge DOS for interface trap states is in the order of mid 10^{13} $cm^{-2}eV^{-1}$ levels. If the traps are distributed over a 1nm interface, the 3D density of states for the traps will be in the mid 10^{20} $cm^{-3}eV^{-1}$ level. As shown in Fig. 4, this is comparable to the conduction band electron DOS calculated using the density functional theory as well as single sub-band parabolic and non-parabolic dispersion curves [5]. In Fig. 4, interface trap density is shown up to 200 meV above the conduction band edge, as the extrapolation of the trap DOS into the CB differs from the exponential expression given in the figure at high energies.

As the calculated Fermi level in device simulations

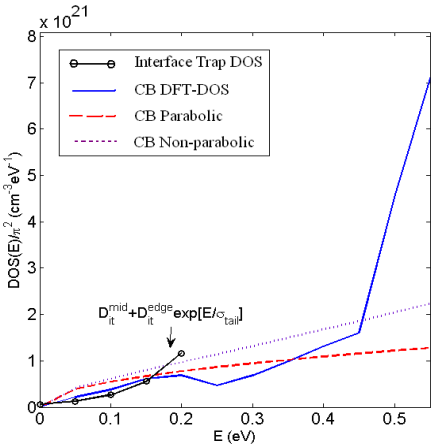

Fig. 4. Electron DOS in the conduction band (DFT, single sub-band parabolic and single sub-band non-parabolic) compared with interface trap densities of states shown using symbols.

are close to the CB minimum, in addition to integrating from the neutrality point to the edge of the conduction band, we need to consider the tail of the distribution function inside the conduction band itself while calculating the occupied trap density. The occupied trap density as calculated by this model is given in (1). Here, E_n is the neutrality point, E_C' is the energy level where conduction band DOS exceeds the interface trap DOS (typically about E_C+200meV), and $f(x, E)$ gives the trap occupation probability as a function of energy and position along the interface as defined by Fermi-Dirac statistics. The Fermi level at each point along the interface is calculated by using the electron concentration at the surface ($n(x, 0)$) and the average conduction band density of states (N_C) for 4H-SiC.

$$N_{it}(x) = \int_{E_n}^{E_C'} D_{it}(E) f(x,E) dE \quad (1)$$

$$E_F(x) = E_C - V_T \ln\left(\frac{n(x,0)}{N_C}\right) \quad (2)$$

The trap occupations for a number of 4H-SiC MOSFETs with different channel doping values are evaluated using this expression. Simulations of the current-voltage characteristics of these devices and comparison to experiment as shown in Fig. 1(a) and 1(b) are then used to extract channel mobility and interface trap density of states values.

IV. Results

A. Device Design and Measurement:

4H-SiC MOSFETs were fabricated at Cree Inc. on epitaxial layers doped to different levels. The oxide was thermally grown and then treated to NO+N_2O high temperature anneals to reduce interface trap densities. The channel doping for the different devices varied from $1\times10^{15}cm^{-3}$ to $5\times10^{18}cm^{-3}$. The MOSFETs were fabricated as 400µmx400µm test structures with an oxide thickness of about 48nm. The threshold voltage for the various devices varied significantly due to their different channel doping concentrations. The room temperature I_D-V_{GS} characteristics were measured and are shown in Fig. 1(a) and 1(b).

B. Calculated Occupied Traps and Inversion Charge:

Due to the very large interface trap DOS near the conduction band edge, conduction band electrons have a probability of occupying a trap that is comparable to the probability of occupying a conduction band state. Due to this effect, the occupied interface trap density does not saturate when the Fermi level is pushed a few tens of meV into the conduction band. On the contrary, with increase in gate bias, the occupied trap density shows an almost linear increase. Beyond inversion, the interface trapped charge and the inversion charge both increase monotonically with gate bias, leading to a

significant reduction in drain-source current in the device. Fig. 5(a) and Fig. 5(b) show the extracted occupied interface traps and the inversion charge density respectively, with increasing gate bias for 4H-SiC MOSFETs with different values of channel doping.

Due to the difference in threshold voltages resulting

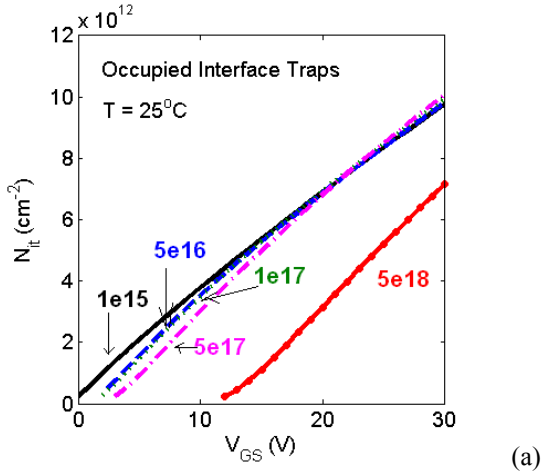

Fig. 5. (a) Extracted occupied interface trap density (N_{it}) and (b) inversion charge density (N_{inv}) in the sample 4H-SiC MOSFETs with different channel doping values from 10^{15} cm^{-3} to 5×10^{18} cm^{-3}. Due to occupation of interface traps spread a few meV inside the conduction band, the occupied interface trap density does not saturate at higher gate biases causing significant degradation in current and transconductance.

from the different channel dopings, the occupied trap density and inversion charge plots are shifted in gate bias. As is seen from equation (2), the occupation probability depends on the surface Fermi level, which in turn is dependent upon the depletion charge and thereby on the channel doping. This leads to the threshold voltage for the $5\times10^{18}cm^{-3}$ channel doping device to be significantly higher than the others, and thereby causing the interface trapped charge and inversion charge to start building up at higher gate biases.

C. Current Degradation Due to Trap Occupation:

The large number of occupied traps leads to a significantly lower value for the inversion charge. This leads to degradation in the current-voltage characteristics of the 4H-SiC MOSFET. Fig. 1(a) and 1(b) shows the simulated and experimentally measured I_{DS}-V_{GS} characteristics of several 4H-SiC MOSFETs. Negatively charged traps at the interface also contribute to Coulombic scattering of the inversion layer electrons, causing a further degradation in the transconductance and I_{DS}-V_{GS} characteristics. As can be seen from Fig 1(a) and 1(b), this interface trap occupation model is able to predict the measured current values very well, in the sub-threshold as well as linear regions, and for a wide range of channel doping values.

V. CONCLUSION

DFT based 4H-SiC DOS calculations and drift-diffusion modeling of 4H-SiC MOSFETs have suggested that the band-edge interface trap DOS in 4H-SiC MOSFETs are comparable to conduction band electron DOS. This leads to similar probabilities of an electron to occupy a conduction band electron state or a conduction band trap. Simulations of transport in 4H-SiC MOSFETs using this trap occupation model have shown an increase in occupied trap density with gate bias even in strong inversion when the Fermi level is pushed into the conduction band. It was possible to predict the behavior of 4H-SiC MOSFETs with different channel doping values over a wide range of gate bias using this model, and obtain excellent match between the simulated and experimentally measured I-V curves.

VI. REFERENCES

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