Impact Ionization and Freeze-Out Model for Simulation of Low Gate Bias Kink Effect in SOI-MOSFETs Operating at Liquid He Temperature

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Abstract— **A 0.4 μm p-channel silicon-on-insulator (SOI) metal-oxide-field-effect-transistor (MOSFET) is measured at 300 K and 4 K. Finite difference two dimensional numeric device simulations are performed at these temperatures to provide physical insight about the mechanisms that lead to the observed cryogenic effects at liquid Helium temperature. The MOSFET subthreshold slope is measured as 88 mv/dec at 300 K and is observed to have a drain bias dependence at 4 K ranging from 30 mv/dec at low source-to-drain (V_{SD}) voltage (0.05 V) to 10 mv/dec at high V_{SD} (3.3 V). A kink in the current is furthermore observed at low gate bias (1.35 V) and drain bias above 2 V. The numeric simulations indicate that incomplete ionization of dopants at cryogenic temperatures and impact ionization significantly affect the device behavior in the subthreshold region of operation at 4 K. Specifically, for a low source-to-gate (V_{SG}) bias (V_{SG} = 1.35 V, which is near subthreshold) the former affects the base current level, and the latter along with the incomplete ionization gives rise to a current kink for high drain biases (V_{SD} > 2 V). The simulation techniques to handle the numerical challenges related to device modeling at 4 K are also presented.**

Keywords: Cryogenic MOSFET simulation, MOSFET operation at 4 K, incomplete ionization, impact ionization at cryogenic temperatures.

I. INTRODUCTION

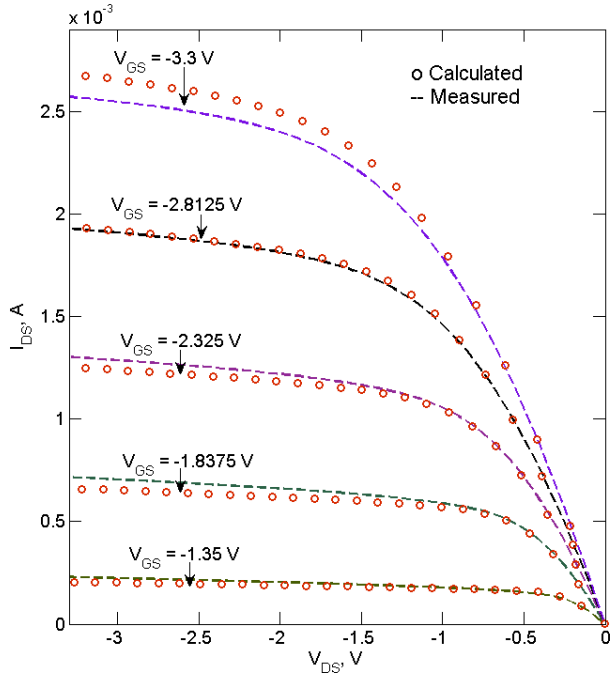
We report on experimentally and numerically obtained 4.2 K p-channel silicon-on-insulator (SOI) MOSFET operation. The two-dimensional numeric simulation reproduces the experimentally observed 4 K behavior only after impact ionization and incomplete thermal ionization of the substrate dopants are included. The p-MOSFET that we use is a 0.4 μm p-channel SOI-MOSFET fabricated in the Sandia National Laboratories 0.35 μm CMOS line.

Measurements of the pFET were done at room temperature and 4.2 K using a Lakeshore cryogenic probe station where the sample is thermally mounted to a copper chuck inside an evacuated test chamber and then cooled by continuous-transfer of liquid Helium. Two-terminal DC measurements of the source-drain current, I_{SD}, were measured as a function of source-drain (V_{SD}), -gate (V_{SG}) and, -body (V_{SB}) biases using an Agilent B1500 semiconductor device analyzer.

Room temperature performance is shown in Fig. 1. The best numeric simulated fit uses a background doping of 3.5×10^{17} cm^{-3} and assumes the nominal geometric dimensions (L = 0.4 μm, W = 10 μm and tox = 7 nm). The short channel structure is found to have a saturation current magnitude dominated by the saturation velocity.

At the nominal 4.2 K temperature, the device characteristics in linear operation resemble that of the room temperature, Fig. 2, but with a slightly higher transconductance due to increased carrier mobilities. The low field mobility is found to be roughly 2× greater. At low gate bias the drain voltage sweep deviates from the qualitative room temperature behavior and shows a current kink past 2 V. Furthermore, the subthreshold slope is observed to have a drain bias dependence at 4 K, and is measured to be 30 and 10 mV/dec at low (V_{SD} = 50 mV) and high V_{SD} (V_{SD} = 3.3 V), respectively. Also, the threshold voltage at 4.2 K is approximately 0.5 V higher than that at room temperature.

Relatively speaking, there has not been a significant effort to design electronics or model MOSFETs that operate reliably at cryogenic temperatures. Most of the electronics design software that has been developed typically is targeted at temperature conditions above approximately 200 K. Cryogenic device simulations have also been performed only down to liquid Nitrogen temperature. The physics of MOSFET operation at liquid Helium temperature simply has not been



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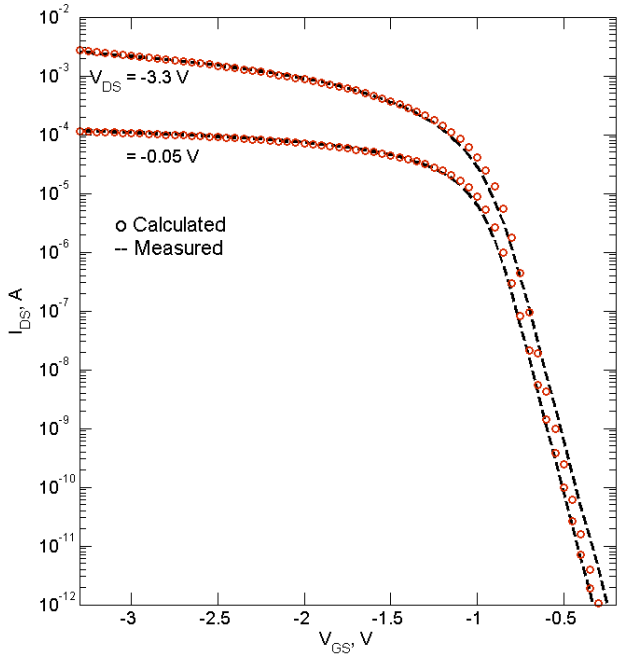

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Figure 1. a) Experimentally measured and numerically calculated room temperature current-voltage curves of a 0.4 µm p-channel SOI-MOSFET. This fitting and b) the subthreshold curves are used for device simulator calibration and doping profile extraction.

investigated using a distributed physics-based model. Thus, we here numerically and experimentally investigate MOSFET operation at 4.2 K, and compare its cryogenic operation with that at room temperature.

Numerical methods are developed to address convergence issues related to two-dimensional finite difference low temperature, 4 K, device simulations. The numerical code solves for carrier transport and electrostatic potential, while resolving more than a hundred orders of magnitude variation in carrier concentration. Numeric simulation of the linear operation of the cryogenic p-channel SOI-MOSFET device agree well with experiment when the low field mobility is adjusted from the room temperature calibrated values. Incomplete donor ionization in the channel and impact ionization (electron-hole generation) significantly affect the simulated short channel device behavior in the subthreshold region of operation at 4.2 K. Accounting for these effects in the 4.2 K simulation produce improved fits to the experimentally obtained results and provides a better model to explain the observed behavior.

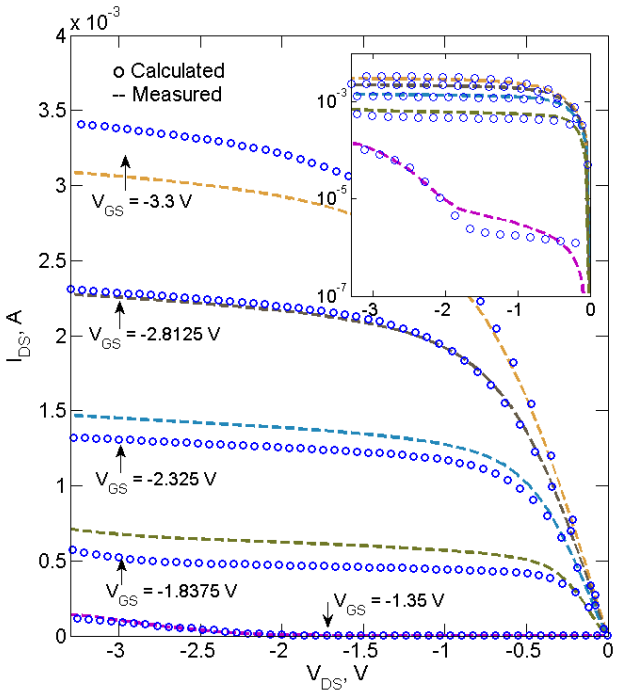
II. Dopant Freeze-Out and Impact Ionization

Our investigations indicate that simulated incomplete and impact ionizations affect device behavior noticeably at 4.2 K. To resolve the dopant freeze-out, we use the following equation for donors and acceptors (phosphorous and boron in silicon, respectively) [1,2]:

$$\frac{N^{+}_{\mathrm{Si:P}}(r,T)}{N^{0}_{\mathrm{Si:P}}(r)} = \frac{b_{\mathrm{Si:P}}(r)}{1+\dfrac{n(r,T)}{g_{\mathrm{Si:P}}N_C(T)e^{-\Delta E_{\mathrm{Si:P}}(r)/kT}}} + (1-b_{\mathrm{Si:P}}(r)) \quad (1)$$

$$\frac{N^{-}_{\mathrm{Si:B}}(r,T)}{N^{0}_{\mathrm{Si:B}}(r)} = \frac{b_{\mathrm{Si:B}}(r)}{1+\dfrac{p(r,T)}{g_{\mathrm{Si:B}}N_V(T)e^{-\Delta E_{\mathrm{Si:B}}(r)/kT}}} + (1-b_{\mathrm{Si:B}}(r)) \quad (2)$$

Here, doping-dependent ΔE is the dopant activation energy, temperature-dependent N is the effective density-of-states at the band edges, doping-dependent b is the fraction of carriers in clusters/localized states, g is the degeneracy factor and k is the Boltzmann constant. We note that even in the absence of a depletion region or at low temperatures, there is a background dopant ionization that is equal to $(1\text{-}b)\times N^0$. In low temperature simulations, we resolve the change in percentage dopant ionization in the channel and the substrate, and also due to impact generated secondary electrons by coupling the aforementioned ionization equations to the Poisson and current continuity equations shown below [1].



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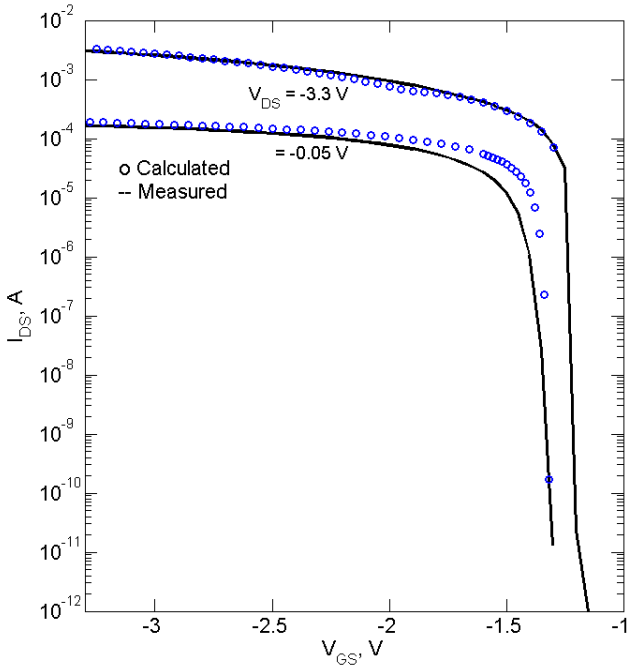

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Figure 2. a) Experimentally measured and numerically calculated 4.2 K current-voltage curves of a 0.4 µm p-channel SOI-MOSFET. b) Measured and simulated subthreshold curves of this MOSFET at 4.2 K show a good match.

$$\nabla^2\phi = -\frac{q}{\varepsilon}\left(p - n + N^{+}_{\text{Si:P}} - N^{-}_{\text{Si:B}}\right) \tag{3}$$

$$F_n = \nabla.\left[\mu_n\left(-n\nabla\phi + V_{\text{th}}\nabla n\right)\right] + \text{GR}_n \tag{4}$$

$$F_p = \nabla.\left[\mu_p\left(p\nabla\phi + V_{\text{th}}\nabla p\right)\right] + \text{GR}_p \tag{5}$$

Above, electrostatic potential, electron concentration and hole concentration are represented by ϕ, n and p, respectively. Moreover, other parameters have their usual meanings.

To account for the impact ionization, we use an experimentally-determined Chynoweth impact ionization expression [3] with a modified exponent γ that we determined empirically. This impact ionization expression is written in Eqn. 6. Below, electron or hole impact coefficient g is calculated using temperature T, local electric field E, and carrier-type dependent parameters A, B, C, and γ.

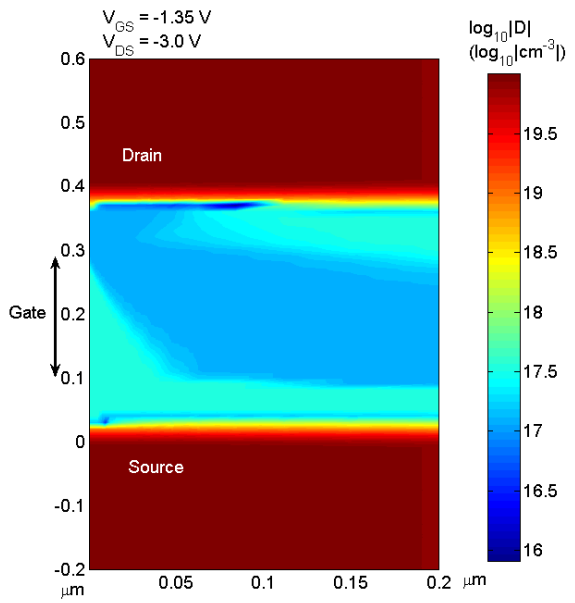
$$g = A\exp\left[-\frac{\left(B + C\times T\right)^{\gamma}}{|E|}\right] \tag{6}$$

Additionally, the intrinsic carrier concentration takes on incredibly small values at cryogenic temperatures. For completeness, we use bandstructure calculated values. We developed numerical and empirical methodologies to circumvent the numerical problems associated with the use of extremely small numbers.

III. Numeric Modeling Results at 4.2 K

The calculated and measured I-V curves at 4.2 K are overlaid in Fig. 2. The combination of simulated donor freeze-out and impact ionization results in a pronounced current kink at 4.2 K as shown in the Fig. 2 inset. The electron temperature is estimated to be approximately 20 K in the channel, deduced by the high V_{SD} subthreshold slope shown in Fig. 2b.

In Fig. 3, we show the channel ionization profile at a high drain bias for the lowest gate voltage. At low drain biases, donors in depletion regions in the channel and around the source/drain terminals are predicted to ionize due to low electron concentrations in these regions. The change in ionization is facilitated by the drain bias dependent impact ionization rate shown also in Fig. 3. As the drain bias rises, the drain-to-channel field also rises, resulting in exponentially increasing ionization rates. The impact generated holes are then swept to the drain terminal due to the high junction field. However, the lateral field from near the drain-junction to source is low, giving rise to accumulation of electrons near the drain. This impact generation gives rise to an increase in



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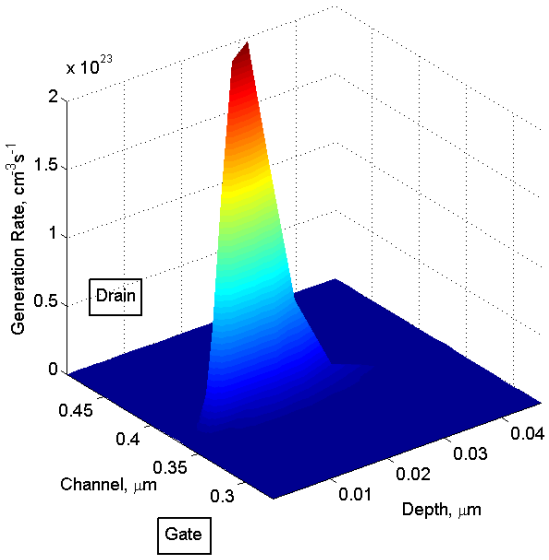

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Figure 3. a) Simulated channel doping profile and b) the associated impact generation rate in the channel at 1.35 V gate and 3.0 V drain biases.

drain current and hence a current kink, even when the dopant ionization level is kept fixed (at a level before the impact ionization becomes important). This type of current kink is similar to those observed in SOI current voltage curves at room temperature, due to source-channel forwarding facilitated by those accumulated minority carriers. However, at 4.2 K, this type of current kink by itself can not explain the amount of increase in drive current for the lowest gate and high drain bias.

The impact generated electrons (channel minority carrier for this p-channel MOSFET) affect channel ionized donor concentration when the denominator of the first term on the right-hand-side of equation 1 starts becoming larger than unity. Some of these impact generated electrons are then trapped at donor sites, resulting in effective lowering of the threshold. The lower threshold along with the shift in body potential due to the residual electrons produces a large current kink at 4.2 K as shown in Fig. 2.

IV. Conclusion

In summary, we developed a two-dimensional self-consistent cryogenic Poisson drift-diffusion simulation tool. The calculated results obtained using this physics-based distributed device simulator reasonably reproduces the 4.2 K measurements when band-to-band impact ionization and freeze-out are both considered. In particular, these models are sufficient to reproduce a current kink that appears at extreme low temperatures while absent at room temperature for the lowest gate bias and high drain voltages.

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