Benchmarking the Accuracy of PCA Generated Statistical Compact Model Parameters Against Physical Device Simulation and Directly Extracted Statistical Parameters

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Abstract—**Statistical variability is a major challenge for CMOS scaling and integration. In order to achieve variability aware design, it's critical important to reliably transfer device characteristics statistical variability information into compact models. A PCA based statistical compact modeling strategy is benchmarked against 'atomistic' device simulation and direct statistical parameter extraction strategy. The results indicate that PCA based approach may introduce considerable error in tail of distribution, which in turn may generate pessimistic or optimistic conclusions in statistical circuit simulation.**

Keywords-statistical variability; statistical compact modeling; principal component analysis; MOSFET

I. INTRODUCTION

Statistical variability (SV) introduced by Random Discrete Dopants (RDD), Line Edge Roughness (LER) and Poly Gate Granularity (PGG) already plays an important role in contemporary CMOS [1]. The investigation of flexible and accurate, yet economical strategies for capturing the above statistical variability in industrial standard compact models is of great importance for variability aware design since compact model acts as the interface between circuit/system designers and semiconductor foundries [2]. The overall accuracy of circuit/system simulation is determined by the accuracy of circuit components modelling. In this paper, using as a reference simulation results obtained by the well-calibrated Glasgow 'atomistic' device, we compare different strategies for statistical compact model parameter generation and their impact on the accurate reproduction of the magnitude of key MOSFET figures of merit, and their correlation.

II. STATISTICAL VARIABILITY IN 35NM PHYSICAL GATE LENGTH DEVICE

The test-bed for our comparison was the physical variability simulation results for a state-of-the art 35 nm physical gate length nMOSFET device with the performance matching Intel 45nm technology generation device results. In order to emphasize the intrinsic parameter fluctuation, the minimum size device with width ratio of 1 is targeted in this study. The simulations were carried out with the Glasgow 3D 'atomistic' drift diffusion (DD) simulator employing density gradient quantum correction simultaneously for electrons and holes. The combined effects of RDD, LER and PGG as SV sources have been taken into account simultaneously. The RDD are generated based on continuous doping profile by placing dopant atoms on silicon lattice sites with the probability determined by the local ratio between dopant and silicon atom concentration [3]; The LER is introduced through 1-D Fourier synthesis with a power spectrum corresponding to a Gaussian auto-correlation function [4]; The PGG is introduced by importing a random section of a large template polycrystalline silicon grain image for the whole gate region. Along the grain boundaries, the Feimi level remains pinned at a certain position in the silicon bandgap [5]. The potential distribution at threshold voltage of a typical device from the statistical ensemble is illustrated in Fig. 1, highlighting the simultaneous impact of the variability sources.

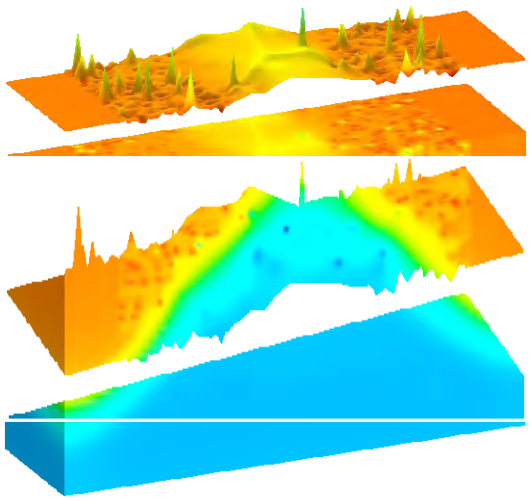

Figure 1. Typical potential profile in a 35nm physical gate length device with RDD, LER and PGG effects on

The distributions of the key figures of merit including the threshold voltage (V_{th}), on current (I_{on}), off current (I_{off}), *DIBL* and subthreshold swing (S) obtained from the physical device

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simulations are shown in Fig. 2. Clearly V_{th}, *DIBL* and $\log(I_{off})$ have largest spread with normalized standard deviations (σ/μ) of 23%, 15% and 7.6%. This indicates that SV has strong impact on the device electrostatic-dominated subthreshold behaviour, introducing noticeable modulation of the short channel effects. It is well known that the DD simulations underestimate the I_{on} variability [6], but still we observe 8.5% normalized standard deviation in I_{on}, equivalent to an σ of 100μA/μm for a minimum size devices. Although multi-width devices are commonly used in digital design, this level of variation will still has a big impact on yield and performance of circuit and system.

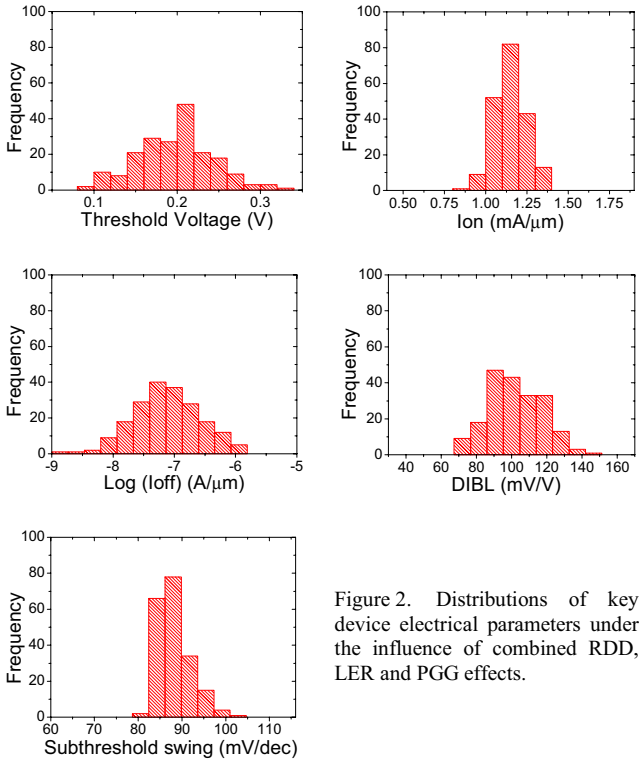

Figure 2. Distributions of key device electrical parameters under the influence of combined RDD, LER and PGG effects.

III. STATISTICAL COMPACT MODELING

A. *Direct extraction approach*

A two-stage statistical compact model parameter extraction strategy [7] has been developed to transfer the SV information obtained by the physical simulations into BSIM4 compact models [8]. In previous studies, only the variability associated with RDD was considered. In this work, in order to precisely reproduce the individual behaviour of each simulated transistor under the influence of combined SV sources, a new set of 7 BSIM4 parameters is identified: *Vth0* is basic long channel threshold voltage parameter, and is selected to account for traditional threshold variation introduced by SV; *U0* is low-field mobility parameter, and is selected to account for current factor variation caused by SV; *Nfactor* and *Voff* are basic subthreshold parameters, and are selected to account for subthreshold slope and off current variation; *Minv* is moderate inversion parameter, and is selected to account for variation at moderate inversion regime; *Rdsw* is basic S/D resistance parameter, and is selected to account for dopant variation at S/D region; *Dsub* is DIBL parameter and is selected to account for DIBL variation introduced by SV.

The final outcome of direct statistical parameter extraction is a statistical set of compact models, each member of the ensemble representing a particular physical simulation. The mean RMS error of the statistical compact model set is 1.2%. The strong correlation between electrical and key statistical BSIM parameters illustrated in Fig. 3 indicates that the physical meaning of the compact model parameters is maintained during statistical extraction. The relatively larger threshold voltage value of this 35nm device comparing to *Vth0* (long channel threshold voltage) clearly demonstrates the strong reverse short channel effects introduced by heavy halo doping in this device.

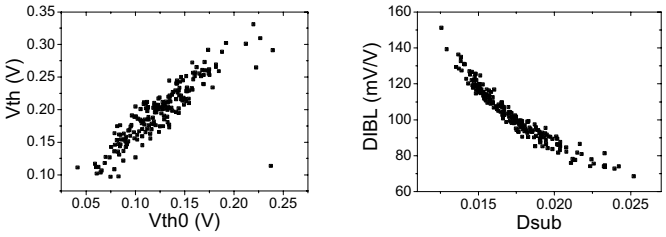

Figure 3. The correlation between electrical and BSIM parameters

Most importantly, by applying this strategy, the correlations between key transistor figures of merit are well preserved, as illustrated in Fig. 4. However there are correlations between the 7 BSIM4 parameters [7], which prevent independent statistical generations of compact model prameters based on analytical approximation of their individual distributions.

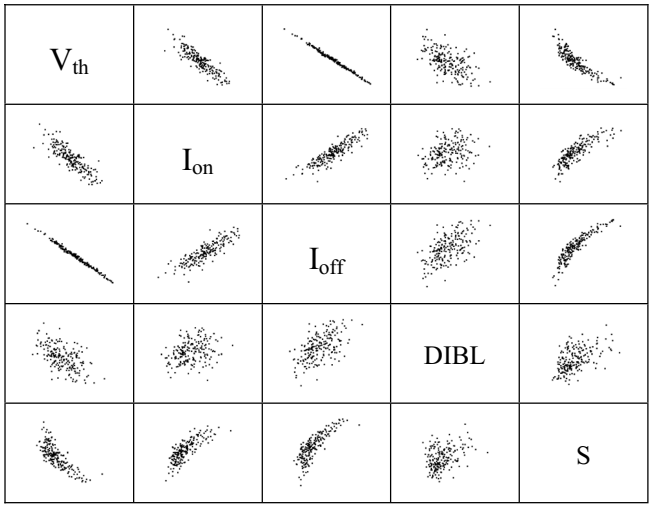

Figure 4. The scatter plots between electrical parameters. Down-left: results from physical 3D device simulation; Up-right: results from direct statistical compact modeling.

B. PCA approach

The general purpose of principal component analysis (PCA) is to transform a large number of correlated variables into a small number of uncorrelated variables called principal components (PC) [9]. The main purpose of the PCA in this study is to allow random generation of 7-parameter set based on the analytic approximation of statistical independent principal components. Before apply PCA on parameter set, all the parameter distributions have been normalized with μ of 0 and σ of 1, and the covariance matrix **S** is generated based on the normalized parameter set distributions. The key step of PCA is to find the eigenvectors and eigenvalues of S, which follows:

$$\mathbf{U'SU = L} \tag{1}$$

Where **U** is eigenvectors, and **L** is eigenvalues. And the transformed variables

$$\mathbf{z = U'x} \tag{2}$$

are the principal components, where **x** are the original variables. For 7-parameter set investigated in this study, the first PC accounts for 45.5% of parameter variations, where the last PC accounts for just under 1% of parameter variations.

PCA itself does not require that the original multi-dimension data follow a particular distribution. However, in order to reconstruct the original data from statistical independent principal components, it is desirable that the original data closely approximate Gaussian distributions and it can be recovered by following operation:

$$\mathbf{x = Uz} \tag{3}$$

where the corresponding principal components follow Gaussian distribution with mean of 0 and variances of eigenvalues **L.**

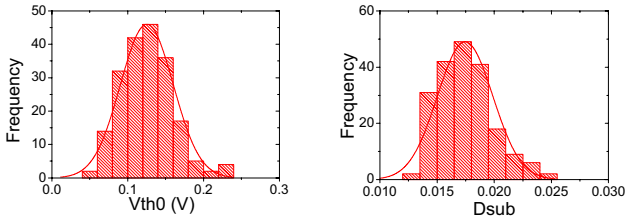

Figure 5. The distribution of two of 7 mapped BSIM parameters

Unfortunately, the typical distributions of the 7 BSIM4 parameters are not always normal, as shown in Fig. 5. This inevitable introduce errors in the values of the statistical compact model parameters after the PCA process. Fig. 6 compares the distribution of 7 BSIM parameters obtained directly from statistical parameter extraction, and generated from the PCA process with all 7 PC involved. The shapes of the BSIM4 parameter distributions are reasonably well preserved by the PCA approach, and the mean value of each BSIM4 parameter is also closely regenerated. Figure 6h also demonstrates that the correlations between statistical parameters are also generally preserved by the PCA approach, although there are some disagreements in the tails of the parameter distributions.

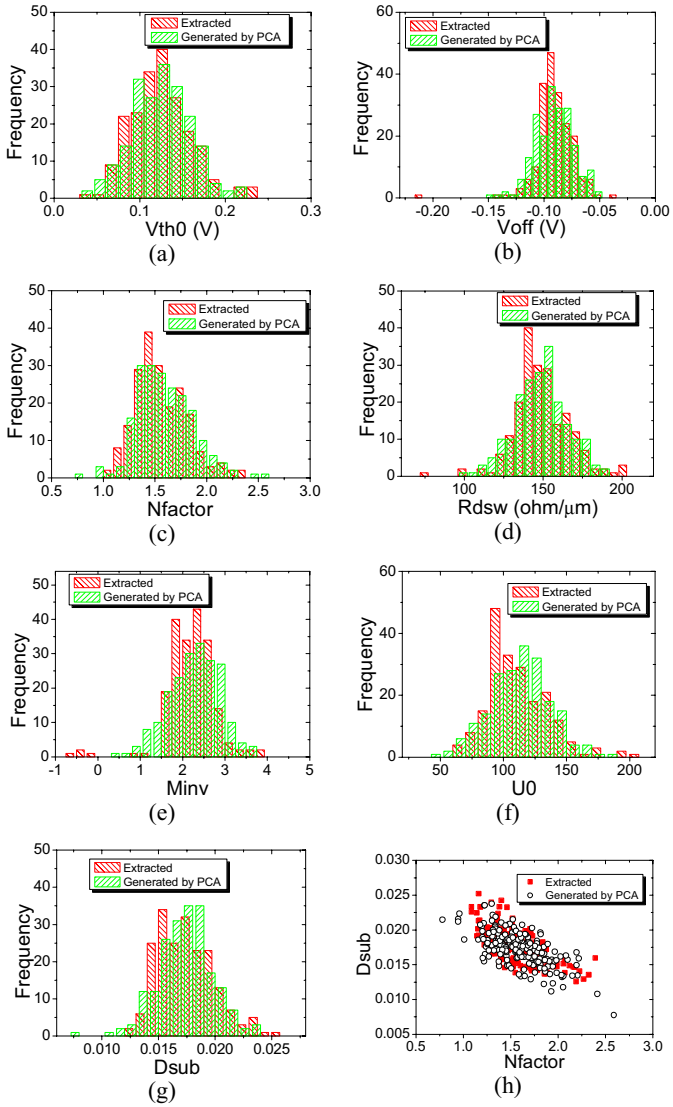

Figure 6. (a)-(g): The distributions of 7 mapped BSIM parameter from direct statistical parameter extraction and PCA process. (h): The correlation between two mapped BSIM parameters

Fig. 7 shows the scatter plot between two key electrical parameters, I_{on} and V_{th} extracted from compact models generated by direct extraction approach and PCA approach respectively. It clearly demonstrates that the correlation between key figures of merits is well preserved by PCA approach; however, PCA approach results in a broader distribution compared to the direct extraction case. Depending on the particular application of the PCA generated statistical compact models, this kind of error may give pessimistic or optimistic results on circuit simulation.

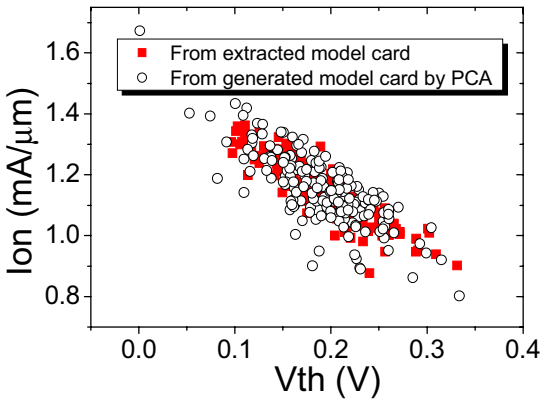

Figure 7. The scatter plot between I_{on} and V_{th}.

C. *Impact of compact modeling approach on circuit simulation*

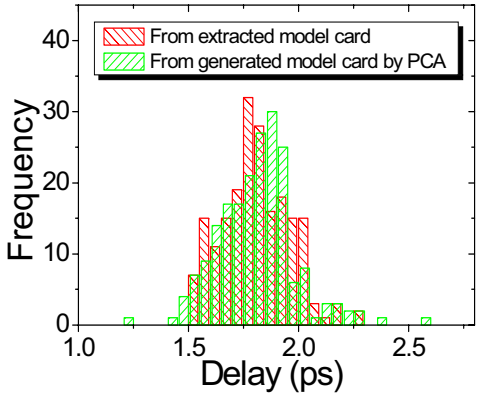

Figure 8. The distribution of inverter delay

In order to investigate the impact of different statistical compact modeling strategies on accuracy of circuit simulation, Monte Carlo circuit simulations were carried out on a CMOS inverter with nMOSFET device randomly generated from these two statistical compact modeling approaches respectively. Since direct extraction approach closely reproduces 'atomistic' physical device simulation results, the circuit simulation results based on this approach is treated as 'gold standard' in this comparison study. The delay of inverter is mainly determined by device's threshold voltage and drive current (assuming load capacitance unchanged). Although the mean values of key figures of merit from these approached are very close, the corresponding distributions were broadened by PCA approach, which in turn may generate considerable errors on standard deviation of delay, as demonstrated by Figure 8. The mean value of inverter delay using directly extracted and PCA generated statistical compact model parameters is in practical the same, but standard deviation of the delay from PCA approach is approximately 15% larger. As a result, for this particular type of circuits, employing PCA approach in statistical circuit simulation will give pessimistic results and introduce unnecessary large margin in circuit design.

IV. CONCLUSIONS

The physical simulation of the combined effect of RDD, LER and PGG in 35 nm physical gate length MOSFETS has been used to benchmark different statistical compact model generation strategies. The directly extracted statistical parameter set preserves the distribution and the correlation between key MOSFET figures of merit. The use of PCA to generate statistical compact model parameters generally preserves the correlation between figures of merit but leads in significant errors in the tails.

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