Compact Modeling of Quasi-Ballistic Transport and Quantum Mechanical Confinement in Nanowire MOSFETs: Circuit Performances Analysis

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Abstract— **In this paper we develop a compact model for ballistic/quasi-ballistic transport in Nanowire. Starting from the well-known approach of Natori/Lundstrom, we enhanced it by including an original modeling of SCE/DIBL (Short Channel Effect and Drain Barrier Lowering), scattering mechanisms and quantum mechanical confinement. Our drain current model has been validated by comparisons with numerical simulations at device and circuit levels. Finally, we used our model to simulate simple circuit elements and to evaluate the impact of Nanowire architecture on the device and circuit performances.**

Nanowire MOSFET, quasi-ballistic transport, compact model, Ring Oscillator, quantum confinement.

I. INTRODUCTION

With the continuous scaling of the MOSFET dimensions in the deca-nanometer range, Nanowire MOSFET have become very attractive mainly due to their excellent SCE immunity compared to conventional structures. Moreover, this aggressive MOSFET scaling introduces new transport properties such as ballistic/quasi-ballistic transport and new scattering mechanisms such as the Remote Coulomb limited Scattering (RCS) mobility due to HfO_2/SiO_2 gate stack. Several pioneering works [1-2] developed analytical formalisms to describe the ballistic and quasi-ballistic regime for ultra-short devices. Nowadays, it is fundamental to include in the same analytical approach the effects of SCE/DIBL, quantum mechanical confinement and scattering mechanisms. However, including this advanced physics does not allow neglecting the impact of parasitic elements on the device characteristics.

In this work, we present a compact model describing the device operation in quasi-ballistic regime using the backscattering coefficient approach. This model is enhanced by the introduction of the "dynamic mean free path" concept (*dfp* including RCS [3]) and the use of a unified backscattering coefficient model valid in low and high electric field [4] with a parabolic potential assumption for the "kT-layer" [5]. In addition, we take into account the SCE/DIBL and quantum effects through the analytical model of the threshold voltage.

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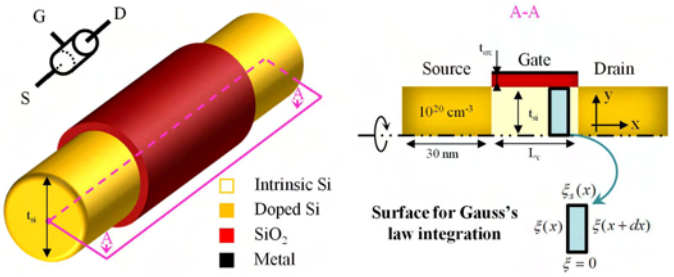


Fig. 1. Nanowire MOSFET and definition of the main geometrical and electrical parameters.

II. ANALYTICAL THRESHOLD VOLTAGE

A. Quasi-ballistic current

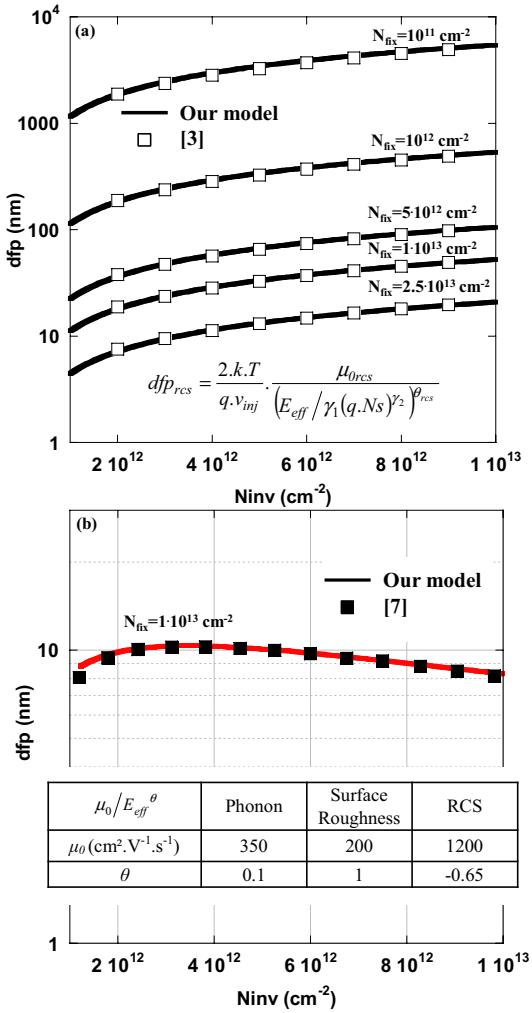
Our quasi-ballistic drain current model is basically inspired from the approach of Natori/Lundstrom [1-2] in the degenerate case, previously used in [6] and extended here for a Nanowire architecture. In this approach, the backscattering coefficient [4] in a parabolic approximation [5] of the "kT-layer" (L_{kT}) is given by:

$$R = \frac{dfp^{-1}}{\frac{1}{2}.L_{kT}^{-1}.\left(1+\coth\left(\frac{L_c}{2.L_{kT}}\right)\right)+dfp^{-1}} \; ; \; L_{kT} = L_c.\left(\frac{k.T}{q.V_{DS}}\right)^{0.5} \qquad (1)$$

where k is the Boltzmann constant, q is the electron charge and T is the lattice temperature. The model accuracy can be improved by including different scattering mechanisms through the "dynamical mean free path" (*dfp*). Due to $TiN/HfO_2/SiO_2$ gate stack, we have built an analytical model to take into account these new scattering effects. We obtain a complete *dfp* model based on an accurate calibration step on numerical [3] and experimental [4] data:

$$dfp_{tot} = \frac{2.k.T/q.v_{inj}}{\left[\left(\frac{\mu_{0rcs}}{\left(E_{eff}/\gamma_1\left(q.N_{fix}\right)^{\gamma_2}\right)^{\theta_{rcs}}}\right)^{-1}+\left(\frac{\mu_{0Ph}}{E_{eff}^{\theta_{Ph}}}\right)^{-1}+\left(\frac{\mu_{0sr}}{E_{eff}^{\theta_{sr}}}\right)^{-1}\right]} \qquad (2)$$

where E_{eff} is the effective electric field, N_{fix} is the fixed charge density at the HfO_2/SiO_2 interface, v_{inj} is the injection velocity and μ_{0rcs}, θ_{rcs}, γ_1, γ_2, μ_{0ph}, μ_{0sr}, θ_{rcs}, θ_{sr} are fitting parameters.



μ_0/E_{eff}^{θ}	Phonon	Surface Roughness	RCS
μ_0 (cm².V⁻¹.s⁻¹)	350	200	1200
θ	0.1	1	-0.65

Fig. 2. Dfp vs. carrier densities (N_{inv}) for various fixed charge densities [3] (N_{fix}) for TiN/HfO_2=3nm/SiO_2=2nm gate stack. Comparisons between our analytical model (solid line) and numerical simulations [3] (dashed): (a) considering only the remote coulomb scattering and (b) comparison with experimental data for t_{si}=15 nm [7]; the model includes RCS, phonon and surface roughness scattering.

Figure 2 illustrates the calibration of this analytical model on numerical simulations [3] (figure 2.a for RCS mechanism) and on experimental data [7] (figure 2.b). As expected for large thickness, the silicon Nanowire mean free path is very close to 10 nm as in planar devices. In fact, recent works [8] showed that the variation of the mean free path extracted on wide range of channel lengths and silicon thicknesses is centred on 10 nm. Note that this observation will be modified by the impact of Nanowire thickness on the band structure. For a large thickness, the scattering rate has the same behaviour as that of a planar structure. However, for small silicon thickness (bellow 5 nm), the scattering rate are strongly impacted by the modification of the band structure and overlaps wavefunctions. Therefore, for a better description of interactions in the Nanowire this point should be taken into account in numerical and analytical models.

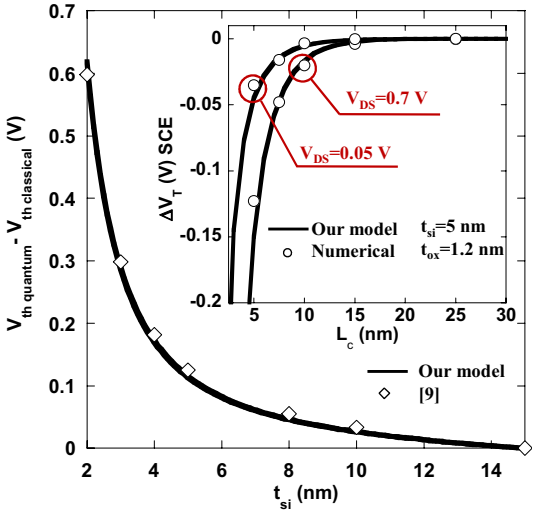


Fig. 3. V_{th} quantum – V_{th} classical (V_{th} classical is the threshold voltage without quantum confinement) vs. tsi. Solid line for analytical model and diamond for numerical simulation [9] [Inset: ΔV_T due to SCE/DIBL versus L_c, comparison between our model (solid line) and TCAD simulations (symbols)]

B. *Short channel effects*

In order to obtain an analytical model for the description of short channel effects, we use the classical approach detailed in [10-11] and already used for symmetrical Double-Gate MOSFET in [6]. In the subthreshold regime, the minority carrier can be neglected and the one-dimensional Poisson's equation is solved by applying the Gauss's law to the particular closed surface (shown on the figure 1):

$$-\xi_{(x)}.\pi.\frac{t_{si}^2}{4}+\xi_{(x+dx)}.\pi.\frac{t_{si}^2}{4}-\xi_{s(x)}.2.\pi.\frac{t_{si}^2}{2}.dx=-\frac{q.N_a}{\varepsilon_{si}}.\pi.\frac{t_{si}^2}{4}.dx \qquad (3)$$

where ξ is the electric field and ξ_S is the surface electric field at the Si/SiO_2 interface. Thus, equation (3) is the same as in [10] with only replacing t_{si} by $t_{si}/2$. After some mathematical manipulations, we obtain an analytical surface potential. However, only the value of the minimum potential at the minimum position (x_{min}) is important for SCE/DIBL:

$$\psi(x_{\min})=2.\sqrt{C_1.C_2}-\frac{C_3}{m_1^2};\ m_1=\sqrt{\frac{2.\eta.C_{ins}}{\varepsilon_{si}.\pi.t_{si}^2}} \qquad (4)$$

where C_{ins} is the cylindrical oxide capacitance, C_1, C_2, C_3 and m_1 are parameters resulting from the Poisson's equation solving in the channel [10]. So, the expression of the threshold voltage shift (ΔV_T) and the S-swing parameter (S) are then obtained from equation (4):

$$\Delta V_T=2.\sqrt{C_1.C_2}\ ;\ S=\frac{k.T}{q}.\ln(10).\left(\frac{d\psi(x_{\min})}{dV_{GS}}\right)^{-1} \qquad (5)$$

We note that, according to [10], parameter η is a fitting parameter that includes the effect of lateral field variation in the depleted film. Therefore, the corresponding value of η is η=0.8 for the expression of S and η=4 for ΔV_T. Finally, in the inset of figure 3, ΔV_T obtained with our analytical model shows a good agreement with numerical simulation results (TCAD Silvaco).

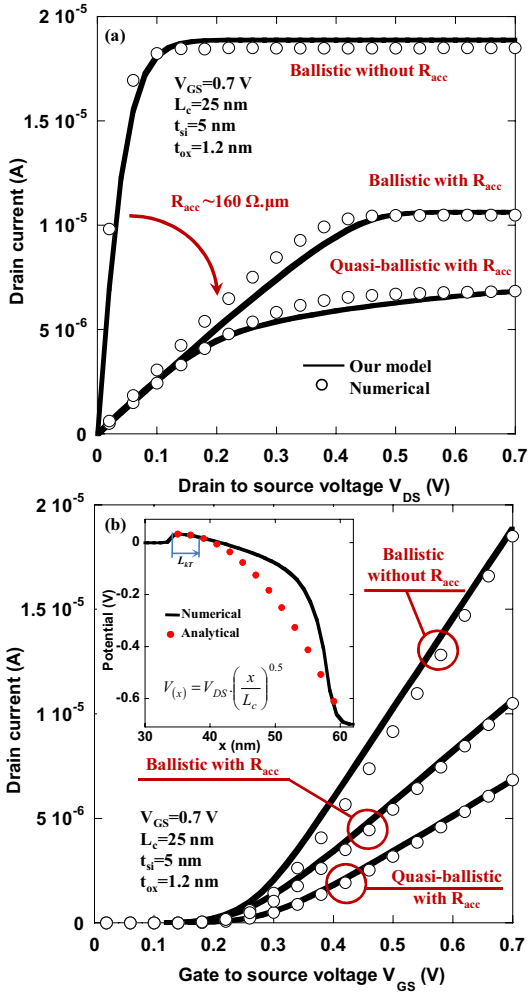


Fig. 4. Drain current versus V_{DS} (a) and V_{GS} (b) for t_{si}=5 nm and L_c=25 nm for ballistic, ballistic with access resistance and quasi-ballistic with access resistance. Solid line for analytical model and circle for numerical simulation [12]. [Inset of figure (b) represents analytical and numerical potentials [12] along the channel for the quasi-ballistic case].

C. *Quantum mechanical confinement*

The threshold voltage is calculated using the boundary condition at the Si/SiO_2 interface [11]:

$$V_{th} = \frac{\varepsilon_{si}}{\varepsilon_{ox}}.t_{ox}.\beta + \phi_F + \psi_s \; ; \; \beta = \frac{k.T.c_{ins}}{2.q.\varepsilon_{si}.t_{si}} \qquad (6)$$

where $c_{ins}=C_{ins}/(\pi.t_{si})$ is the normalized gate oxide capacitance for cylindrical Nanowire and $\Phi_F=(k.T/q).ln(N_a/ni)$. The modeling of quantum confinement is based on the analytical expression of the surface potential ψ_s. The starting point of the development is to simplify the quantum inversion charge Q_i in the subthreshold regime. For a Nanowire, we obtain:

$$Q_i = \sum_n \sum_i \left(\frac{2}{\pi}.\sqrt{\frac{2.m_{1D}}{\hbar^2}} \right).\sqrt{\frac{k.T}{q}}.\int_0^{\infty} \frac{y^{-0.5}}{1+e^{\,y-\frac{q}{k.T}.\left(E_n^i+\frac{E_g}{2}-\psi_s\right)}}.dy \qquad (7)$$

where $\hbar$ is Plank constant, m_{1D} is the one dimensional density of state effective mass (m_{1D}= m_t for n=1,2 and $m_{1D}=m_l$ for n=3), m_t is the transverse mass, m_l is the longitudinal mass and E_g is the silicon gap. However, Q_i in the subthreshold conditions can be simplified as:

$$Q_i \approx Q^*.e^{-\frac{q.\psi_S}{k.T}} \qquad (8.a)$$

$$Q^* = \sum_n \sum_i \left(\frac{2}{\pi}.\sqrt{\frac{2.m_{1D}}{\hbar^2}} \right).\sqrt{\frac{k.T}{q}}.\sqrt{\pi}.e^{-\frac{q}{k.T}.\left(E_n^i+\frac{E_g}{2}\right)} \qquad (8.b)$$

where E_n^i are the energy levels resulting from the quantum confinement of carriers in the Silicon film. As described in [11] this parameter is the sum of two terms: the energy for an infinite rectangular two-dimensional potential and quantum correction of the energy levels using a first-order perturbation method. We finally obtain:

$$\varepsilon_{1,2}^i = \frac{(\hbar.\pi.i)^2}{2.q.t_{si}^2}.\left(\frac{1}{m_t}+\frac{1}{m_l}\right); \; \varepsilon_3^i = \frac{(\hbar.\pi.i)^2}{q.t_{si}^2}.\frac{1}{m_t} \qquad (9.a)$$

$$E_n^i = \varepsilon_n^i + \left(\beta.t_{si}^2/3\right).\left(1+3/\left(\pi^2.i^2\right)\right) \qquad (9.b)$$

We define the threshold voltage, V_{th}, as the gate voltage for which the inversion charge, Q_i, reaches a constant value $Q_{iT}=c_{ins}.k.T/q$ [11]. Then, the surface potential to be used in (6) is:

$$\psi_s = k.T/q.\ln(Q_{iT}/Q^*) \qquad (10)$$

Finally, the threshold voltage used in the drain current equation [6] is $V_T=V_{th}-\Delta V_T$. Figure 3 illustrates the difference between V_{th} with quantum mechanical confinement and classical (i.e. without quantum mechanical confinement) cases. Our model shows also an excellent agreement with results obtained by numerical Schrödinger-Poisson solver calculation [9].

III. SIMULATIONS RESULTS

A. *Model validation at the device level*

Our model is implemented in Verilog-A environment to simulate the Nanowires schematically presented in figure 1. Figure 4.a and 4.b show the drain current versus V_{DS} or V_{GS} in cases of ballistic transport and quasi-ballistic transport with or without access resistances. This analytical model matched well with numerical simulation [12]. Note that the numerical approach in [12] represents an enhanced drift-diffusion-like approach to include ballistic/quasi-ballistic effects in a TCAD simulator. As expected, the current is strongly impacted by scattering mechanisms and access resistances. Moreover, to validate the parabolic potential approach for the "kT-layer", we have compared our analytical potential approach with the corresponding numerical simulation (inset of figure 4.b). The two potentials fit at the beginning of the channel that corresponds to the "kT-layer" localization. Nevertheless, it is important to understand that the exponent of the power law in the "kT-layer" expression (1) depends on the effect of both the mean free path and electrostatic condition. Currently, very few "kT-layer" models [5] have an accurate analytical approximation of this exponent.

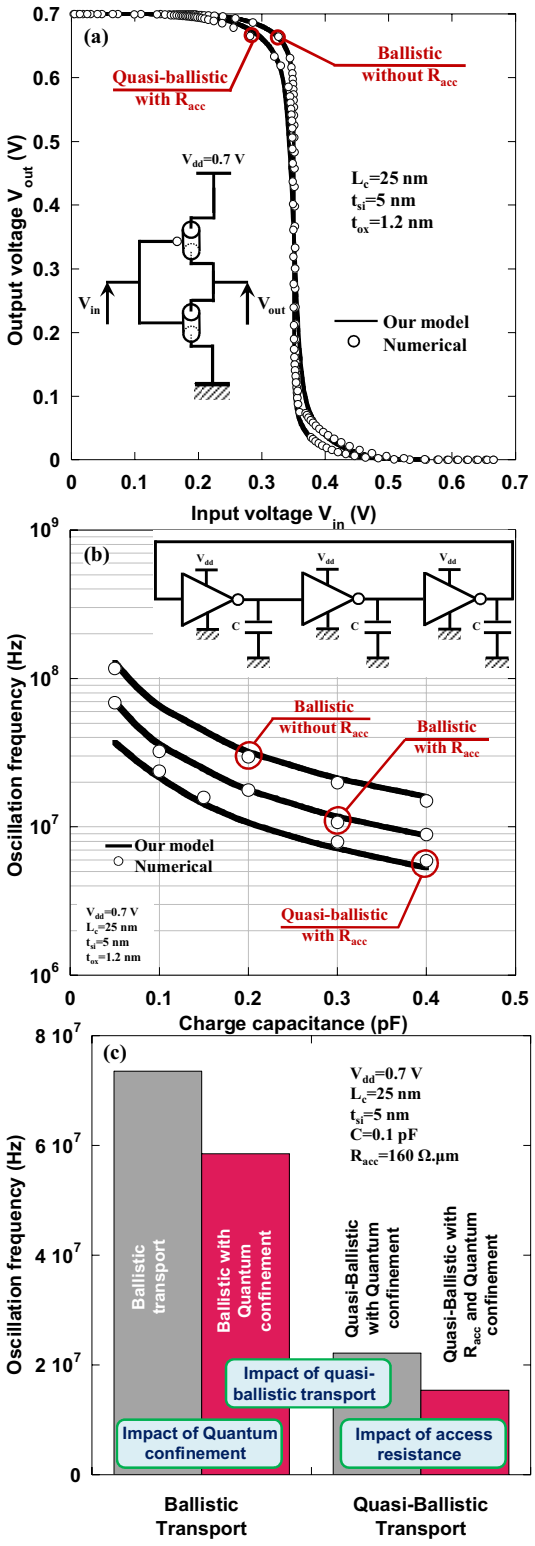


Fig. 5. Comparison between analytical (solid line) and numerical simulation [12] (circle) : (a) V_{out} vs V_{in} of CMOS in ballistic and quasi-ballistic with access resistance and (b) oscillation frequency of ring oscillator in ballistic and quasi-ballistic with or without access resistance. (c) Impact of quantum confinement, quasi-ballistic transport and access resistance for t_{si}=5 nm, L_c=25 nm, C=0.1 pF for TiN/HfO_2=3nm/SiO_2=2nm gate stack.

B. *Circuit operation*

We have performed a detailed analysis of CMOS Nanowire in both static and transient regimes. Figure 5.a and 5.b compare simulation results using the compact model and numerical simulations of CMOS inverters and three stages ring oscillators. To clearly highlight the impact of Nanowire architecture on circuit operation, we compared in Fig. 5.c the oscillation frequency of three stages Ring Oscillator for four cases: ballistic transport with and without quantum confinement, and quasi-ballistic transport (including quantum confinement) with or without access resistances. These results show (whatever the charge capacitance), the strong impact of quantum mechanical confinement, access resistances and quasi-ballistic transport on the oscillation frequency; all these phenomena reduce the oscillation frequency with respect to the ideal case of a ballistic transport in the channel and without access resistances and quantum confinement.

IV. Conclusion

This work proposed a unified compact model for Nanowire MOSFET taking into account SCE/DIBL, quasi-ballistic transport, scattering mechanisms and quantum mechanical confinement. Nevertheless, our model does not address the evolution of the band structure with the silicon thickness, which plays an important role on transport properties.

This model has been validated with some numerical simulation on single device and circuit element: CMOS inverter and three-stage ring oscillator. Therefore, we quantified the significant impact of quasi-ballistic transport, scattering mechanism, electrostatic condition and parasitic element on oscillation frequency. Our results show that if the influence of parasitic elements or quantum confinement is not considered in the analytical model, the Nanowire performances will be strongly overestimated.

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