Statistical Analysis of Metal Gate Workfunction Variability, Process Variation, and Random Dopant Fluctuation in Nano-CMOS Circuits

Chih-Hong Hwang[1], Tien-Yeh Li[1], Ming-Hung Han[1], Kuo-Fu Lee[1], Hui-Wen Cheng[1], and Yiming Li[1,2,3]
[1]Institute of Communication Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu City, Hsinchu 300, Taiwan
[2]Department of Electrical Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu City, Hsinchu 300, Taiwan
[3]National Nano Device Laboratories, No.26, Prosperity Road I, Science-Based Industrial Park, Hsinchu 300, Taiwan

***Abstract*—This work for the first time estimates the influences of the intrinsic parameter fluctuations consisting of metal gate workfunction fluctuation (WKF), process variation effect (PVE) and random dopant fluctuation (RDF) on 16-nm-gate planar metal-oxide-semiconductor field effect transistors (MOSFETs) and circuits. The WKF and RDF dominate the threshold voltage fluctuation; however, the WKF brings less impact on the gate capacitance due to the screening effect of the inversion layer. The fluctuation of timing characteristics depends on the threshold voltage fluctuation, and therefore is proportional to the trend of threshold voltage fluctuation. For an amplifier circuit, the high-frequency characteristics, the circuit gain, the 3dB bandwidth, the unity-gain bandwidth power, and the power-added efficiency, are explored consequently. Similar to the trend of the cutoff frequency, the PVE and RDF dominate both the device and circuits characteristic fluctuations due to the significant gate capacitance fluctuations and the WKF is less important at this simulation scenario. The extensive study assesses the fluctuations on circuit performance and reliability, which can in turn be used to optimize nanoscale MOSFET and circuits.**

Keywords- Emerging device technology, intrinsic parameter fluctuation, nanoscale MOSFET, circuit, coupled device-circuit simulation, modeling and simulation

I. INTRODUCTION

As the dimension of semiconductor device shrunk into nanoscale, variability of performance and yield in nanoscale complementary metal oxide semiconductor (CMOS) devices are great of interest. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, fluctuations in process parameters, and other factors, are known as indispensable components of the robust circuit design procedure. For state-of-art nanoscale CMOS circuits and systems, the intrinsic device parameter fluctuations that result from line edge roughness [1], the granularity of the polysilicon gate [2], random discrete dopants [3-11] and other causes, have substantially affected signal system timing [10,11] and high frequency characteristics [9]. Diverse simulation and suppression approaches have recently been presented to investigate intrinsic parameter fluctuations in semiconductor devices [1-8] and circuits [9-11]. Among these approaches, the metal-gate and high-κ are key technologies for the reduction of intrinsic parameter fluctuations. However, the use of metal as a gate material introduces a new source of random variation due to the dependency of workfunction on the orientation of metal grains [12,13]. Investigation of the impacts of the workfunction fluctuation on both CMOS device and circuit characteristics is lack. Additionally, the circuit performance may depend on different device characteristics. The dominance term of the circuit characteristic fluctuation should be identified.

Therefore, we herein estimate the influences of the intrinsic parameter fluctuations (metal gate workfunction variability (WKF), process variation effect (PVE), and random dopant fluctuation (RDF)) on 16-nm planar CMOS circuits. Instead of using compact models, the characteristic fluctuations of circuit were investigated using 3D device-circuit coupled simulations [9,14] to ensure the best accuracy. The preliminary results show that the WKF and RDF affect device threshold voltage (V_{th}) most and impact the delay time of inverter. The significant V_{th} fluctuation of PMOS induced by WKF demonstrates the increasing importance of WKF in nanoscale device and circuit. The impact of intrinsic parameters on high-frequency characteristics is then examined. Rather different to the results of DC characteristic fluctuation, WKF results in a less impact on high-frequency characteristic owing to the small gate capacitance fluctuation. The study on the intrinsic parameter fluctuations with emphasis on devices and circuits' variability may benefit CMOS design and technology in sub-22-nm era.

The paper is organized as follows. Section II introduces the simulation technique for studying the effect of intrinsic parameter fluctuations in nanoscale devices and circuits. Section III studies the characteristic fluctuations in 16-nm-gate devices and circuits. Finally, conclusions are drawn and the future work is suggested.

II. SIMULATION METHODOLOGY

The devices we investigated are the 16-nm-gate bulk MOSFETs (width: 16 nm) with amorphous-based TiN/HfSiON gate stacks with an EOT of 1.2 nm [12]. The nominal channel doping concentration of the device is 1.48×10^{18} cm^{-3} and the V_{th} are calibrated. The RDF simulation mainly follows our recent work [6-9], in which 758 dopants are randomly

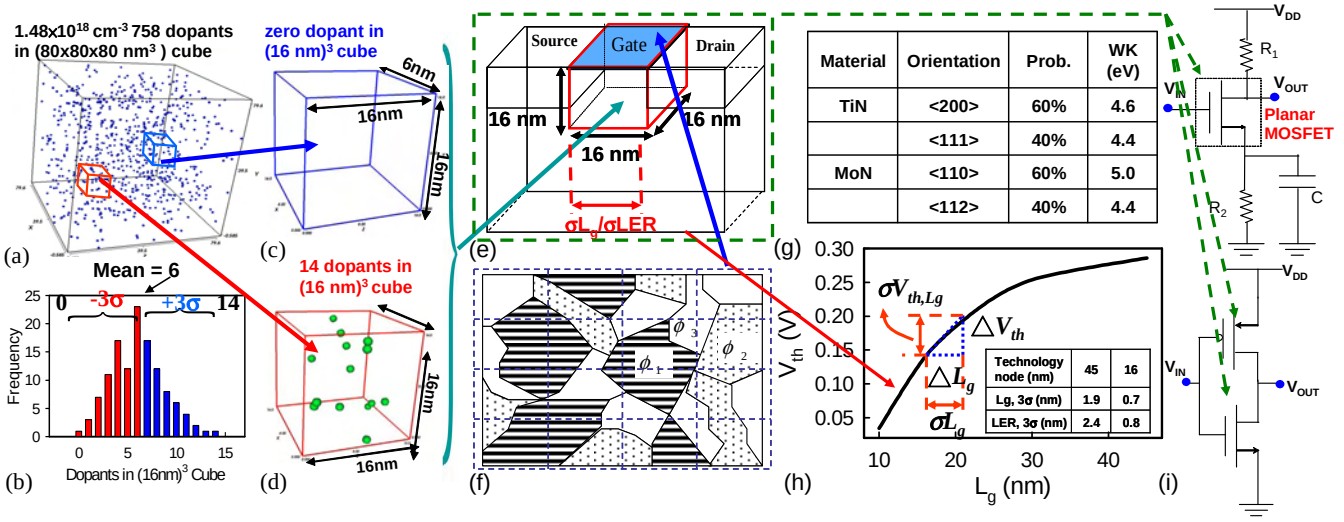

Figure 1. (a) 758 dopants are randomly generated in a large cube of 80x80x80 nm^3, in which the equivalent doping concentration is $1.48x10^{18}$ cm^{-3}. The large cube is then partitioned into 125 sub-cubes of 16x16x16 nm^3. The number of dopants in sub-cube may vary from zero to 14, and the average number is 6 ((b)-(d)). (e) These 125 sub-cubes are equivalently mapped into the device channel of bulk planar MOSFETs for the 3D device simulation with discrete dopants. (f) The gate area of nanoscale devices is composed of a small number of grains and the distribution follows (g). The PVE induced σV_{th} fluctuation is estimated from the V_{th} roll-off characteristics. (i) Presents the tested common-source amplifier and inverter circuits in this study.

generated in a large cube, in which the equivalent doping concentration is $1.48x10^{18}$ cm^{-3}, as shown in Fig. 1(a). The large cube is then partitioned into sub-cubes, in which the number of dopants may vary from zero to 14, and the average number is 6, as shown in Figs. 1(b)-(d). These sub-cubes are mapped into the device channel for the 3D device simulation with discrete dopants, as shown in Fig. 1(e). Note that in "atomistic" device simulation, the resolution of individual charges within classical device simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [4]. The potential becomes too steep with fine mesh; and therefore the majority carriers are un-physically trapped by ionized impurities and the mobile carrier density is reduced [4]. Thus, the density-gradient approximation is used to handle discrete charges by properly introducing the quantum mechanical effects [6-9,15]. The physical model and accuracy of such large-scale simulation approach have been quantitatively calibrated by experimentally measured results [8].

For WKF, considering the sizes of metal grains and the gate area of the devices, the gate area of nanoscale devices is composed of a small number of grains, as shown in Fig. 1(f). Since each grain orientation has a different workfunction, the gate workfunction should be modeled as a probabilistic distribution rather than a deterministic value. Therefore, a statistically-sound Monte-Carlo approach is advanced here for modeling such a probabilistic distribution. The gate area of nanoscale transistor is partitioned into several parts according to the average grain size. Then the grain orientation of each parts and total gate workfunction are estimated based on properties of metal as shown in Fig. 1(g) [13]. Furthermore, we apply the statistical approach to evaluate the effect of PVE, as shown in Fig. 1(h), in which the magnitude of the gate length deviation and the line edge roughness follows the projections of the ITRS 2007. The PVE includes the gate length deviation and the line edge roughness, whose magnitude follow the projections of the ITRS 2007. Figures 1(i) illustrates the inverter and common-source amplifier for test, respectively. To properly capture the circuits' characteristic fluctuations, instead of compact model approach, a 3D device-circuit coupled simulation is employed [9]. A sinusoid input wave (0.5 V offset voltage with frequency from $1x10^{8}$ Hz to $1x10^{13}$ Hz.) is used for studying the high-frequency characteristics of amplifier.

III. Results and Discussion

The V_{th} fluctuations for planar NMOS and PMOS devices are examined in Figs. 2(a) and 2(b). The total V_{th} fluctuation is given by according to the independency of the fluctuation components:

$$\left(\sigma V_{th,total}\right)^2 \approx \left(\sigma V_{th,RDF}\right)^2 + \left(\sigma V_{th,WKF}\right)^2 + \left(\sigma V_{th,PVE}\right)^2 \qquad (1)$$

in which the $\sigma V_{th,RDF}$, $\sigma V_{th,WKF}$, and $\sigma V_{th,PVE}$, are the random-dopant-, workfunction-fluctuation- and process-variation -induced V_{th} fluctuation, respectively. The results show that the RDF dominates the V_{th} fluctuation in NMOSFETs; however, for the V_{th} fluctuation of PMOS, the WKF becomes the dominating factor because of the large deviation of the

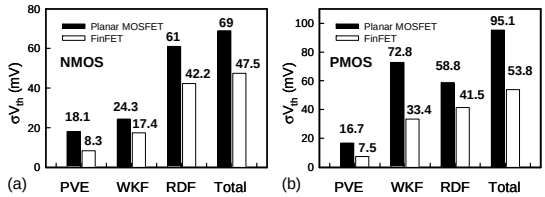

Figure 2. V_{th} fluctuation for (a) NMOS and (b) PMOS devices, where the total σV_{th} is calculated with Eq. (1).

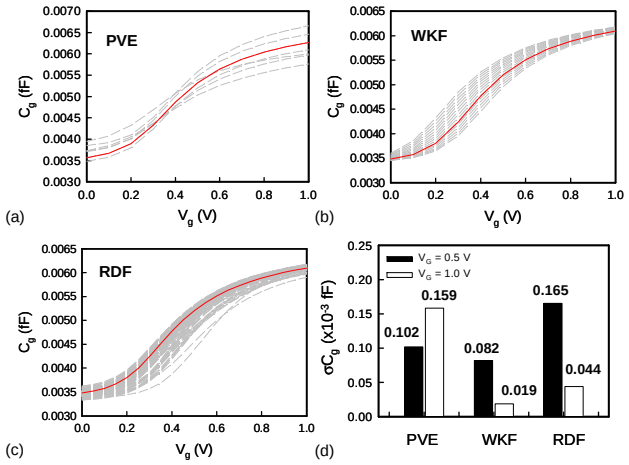

Figure 3. The C_g-V_G characteristics for the explored devices with (a) PVE, (b) WKF, and (c) RDF. (d) The C_g fluctuation for 16-nm-gate MOSFETs with WKF, PVE, and RDF. The filled-in bars are the results of σC_g at V_G = 0.5 V and the open bars are for V_G = 1 V.

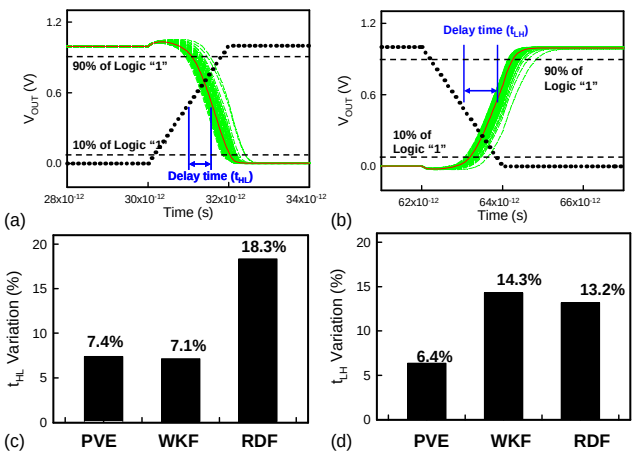

Figure 4. The (a) high-to-low and (b) low-to-high characteristics of the tested inverter, in which the (a) tHL and (b) tLH fluctuations w.r.t. WKF, PVE, and RDF are extracted, respectively.

workfunction for different grain orientation in Fig. 1(g). The WKF, PVE, and RDF fluctuated C_g are presented in Figs. 2(a)-2(c), where the solid line shows the nominal case with 16-nm-gate, 1.48×10^{18} cm^{-3} channel doping and the dashed lines are fluctuated cases. The different intrinsic parameter fluctuation induced rather different C-V characteristics. Figure 2(d) summarizes the gate capacitance fluctuations (σC_g) with 0.5 V and 1.0 V gate bias. Different to the results of V_{th} fluctuation, the WKF brought less impact on gate capacitance fluctuation. Moreover, the RDF and PVE dominate the gate capacitance fluctuations at 0.5 and 1.0 gate bias, respectively. Our preliminary results show that the impacts of the WKF on C_g is reduced significantly at high gate voltage (V_G) due to the screening effect of inversion layer of device, which screens the variation of surface electrostatic potential and decreases the fluctuation of gate capacitance. The screening effect resulting from the inversion layer also decreases the RDF induced gate capacitance fluctuation at high gate bias; however, the screening effect of inversion layer is weakened by discrete dopants positioned near the channel surface. Notably, the PVE brings direct impact on gate length and therefore influences the gate capacitance. The PVE induced gate capacitance fluctuation is independent of screening effect and should be noticed when the transistor operated in high gate bias, as shown in Fig. 2(d).

Figures 4(a) and 4(b) shows the high-to-low and low-to-high transition characteristic of the output signal and the high-to-low delay time (t_{HL}) and low-to-high delay time (t_{LH}) are calculated in Figs. 4(c) and 4(d). Since the t_{HL} and t_{LH} are dependent on the V_{th} fluctuations for NMOS and PMOS devices, respectively, according to the results of Fig. 2, the RDF and WKF are the dominating factors in timing fluctuations and WKF introduces a largest t_{LH} fluctuation due to the large workfunction deviation in scaled gate area as shown in Fig. 1(f). The WKF has shown its increasing importance in nanoscale transistor, especially in PMOS characteristics. Notably, we herein use the transistors' gate

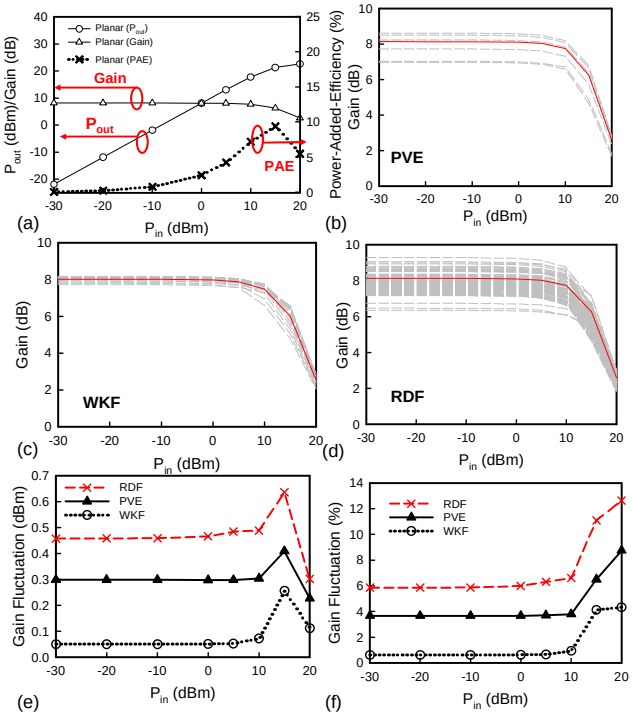

Figure 5. (a) The P_{out}, gain, and PAE of the tested common-source amplifier (the results of nominal case), and gain fluctuations of (b) PVE, (c) WKF, and (d) RDF, respectively. The summarized (e) gain fluctuation and (f) normalized gain fluctuation.

capacitance as the load capacitance (C_{load}) and focused on the device intrinsic parameter fluctuation induced circuit variability. The result of the nominal propagation delay may be changed as we take an additional load capacitance into consideration. Power-added efficiency (PAE), as defined below, is a measure for the power conversion efficiency of power amplifiers, as shown in below:

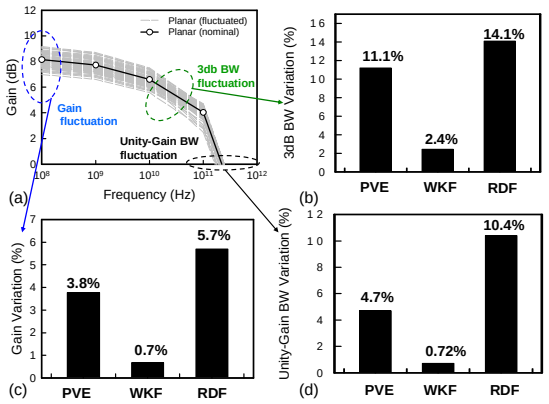

Figure 6. (a) The fluctuation of high frequency response of the common-source amplifiers, in which (b) 3dB bandwidth, (c) gain, and (d) unity-gain bandwidth are extracted.

$$PAE\ (\%) = ((P_{out} - P_{in}) / P_{DC}) \times 100\%, \qquad (5)$$

where P_{out}, P_{in} and P_{DC} are output, input and DC supplied power, respectively. Figure 5(a) shows the nominal output power (P_{out}), gain, and power-added-efficiency (PAE) of the common-source power amplifier as a function input power (P_{in}) in which the channel is continuously doped and the operation frequency is 10^8Hz. Owing to the limitation of output signal swing, the nominal value of Pout is saturated after 10 dBm input power, which in turn decreases the gain of circuit. The gain fluctuations resulted from WKF, PVE, and RDF are explored in Figs. 5(b)-5(d). Since the PVE and RDF dominate gate capacitance fluctuations due to significant affected the channel length and depletion width, the PVE, and RDF play important roles in high frequency characteristic fluctuation, as shown in Figs. 5(e) and 5(f). Effects of WKF in high frequency characteristics may be neglected in this scenario. The enlarged gain fluctuation with increasing input power is resulted from the larger portion of device operation in linear region. While the magnitude of input signal swing increases larger than 0.178 V (input power larger than 15 dBm), some part of device operation enters cutoff region and therefore decreases the gain fluctuation. The high frequency characteristic fluctuation is then investigated in Fig. 6(a), in which the fluctuation of high frequency circuit gain, 3dB bandwidth, and unity-gain bandwidth are extracted, Figs. 6(b)-6(d). Similar to the result of Fig. 3, the RDF and PVE dominates the high frequency characteristic fluctuations and WKF become less important in this analyzing scenario.

IV. Conclusions

In this study, we have estimated the influences of the intrinsic parameter fluctuations in 16-nm planar MOSFETs and circuits. Our preliminary results have shown that the WKF and RDF dominate the σV_{th}; and therefore rule the delay time of the explored digital inverter circuits. The fluctuation of delay time depends on the V_{th} fluctuation which follows the trend of V_{th} fluctuation. The WKF effect in PMOSFETs may bring significant impact on t_{LH} characteristics due to the large difference of workfunction in different grain orientation. For the high-frequency characteristics, the circuit gain, the power, and the power-added efficiency were also explored. Similar to the trend of the device cutoff frequency, the PVE and RDF dominate the device and circuits characteristic fluctuations and the WKF shows less impact on high-frequency characteristic owing to the small gate capacitance fluctuation. The sensitivities of circuit performance with respect to device parameter fluctuation have been reported. It is necessary to include both the WKF and RDF effects in studying digital circuit reliability; however, for the high frequency applications, the PVE and RDF effect are dominating factors.

Acknowledgment

This work was supported in part by Taiwan National Science Council (NSC) under Contract NSC-97-2221-E-009-154-MY2 and Contract NSC-96-2221-E-009-210.

References

[1] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation Study of Individual and Combined Sources of Intrinsic Parameter Fluctuations in Conventional Nano-MOSFETs," *IEEE Trans. Electron Device*, vol. 53, no. 12, pp. 3063-3070, Dec. 2006.

[2] H. P. Tuinhout, A. H.Montree, J. Schmitz, and P. A. Stolk, "Effects of gate depletion and boron penetration on matching of deep submicron CMOS transistor," in *IEDM Tech. Dig.*, 1997, pp. 631–634.

[3] R. W. Keyes, "Effect of Randomness in Distribution of Impurity Atoms on FET Thresholds," *Appl. Phys.*, vol. 8, pp. 251-259, 1975.

[4] K. Noda, T. Tatsumi, T. Uchida, K. Nakajima, H. Miyamoto, and C. Hu, "A 0.1-μm delta doped MOSFET fabricated with post-low-energy implanting selective epitaxy," *IEEE Trans. Electron Device*, vol. 45, no. 4, pp. 809–813, Apr. 1998.

[5] D. Vasileska, W.J. Gross, and D.K. Ferry, "Modeling of deep-submicrometer MOSFETs: random impurity effects, threshold voltage shifts and gate capacitance attenuation" in *Extended Abstracts of International Workshop on Computational Electronics*, pp. 259-262, Oct. 1998.

[6] Y. Li, and C.-H Hwang, "Discrete-dopant-induced characteristic fluctuations in 16 nm multiple-gate silicon-on-insulator devices", *J. Appl. Phy.*, vol. 102, no. 8, 084509, 2007.

[7] Y. Li and S.-M. Yu, "A Coupled-Simulation-and-Optimization Approach to Nanodevice Fabrication With Minimization of Electrical Characteristics Fluctuation," *IEEE Trans. Semi. Manufacturing*, vol. 20, no. 4, pp.432-438, Nov. 2007.

[8] Y. Li, S.-M. Yu, J.-R. Hwang and F.-L. Yang, "Discrete Dopant Fluctuated 20nm/15nm-Gate Planar CMOS", *IEEE Trans. Electron Device*, vol. 55, no. 6, pp. 1449-1455, June 2008.

[9] Y. Li, and C.-H Hwang, "High-Frequency Characteristic Fluctuations of Nano-MOSFET Circuit Induced by Random Dopants," *IEEE Trans. Microwave Theory Tech.*, vol. 56, no. 12, pp. 2726-2733, Dec. 2008.

[10] X. Tang, K. A. Bowman, J. C. Eble, V. K. De, and J. D. Meindl, "Impact of Random Dopant Placement on CMOS Delay and Power Dissipation," in *Proc.29th European Solid-State Device Research Conf.*, pp. 184-187, Sept. 1999.

[11] H. Mahmoodi, S. Mukhopadhyay, and K. Roy," Estimation of delay variations due to random-dopant fluctuations in nanoscale CMOS circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1787-1796, Sept. 2005.

[12] K. Ohmori, et. al, " Impact of additional factors in threshold voltage variability of metal/high-k gate stacks and its reduction by controlling crystalline structure and grain size in the metal gates," in Int. Electron Devices Meeting Tech. Dig., pp. 1-4, Dec. 2008.

[13] H. Dadgour, De Vivek, K. Banerjee, "Statistical modeling of metal-gate Work-Function Variability in emerging device technologies and implications for circuit design," in Proc. of Int. Conf. on Computer-Aided Design, 2008, pp. 270-277.

[14] T. Grasser and S. Selberherr, "Mixed-mode device simulation," *Microelectronics Journal*, vol. 31, no. 11-12, pp.873-881, Dec. 2000.

[15] M. G. Ancona and H. F. Tiersten, "Macroscopic physics of the silicon inversion layer," Phys. Rev. B, vol. 35, no. 15, pp. 7959-7965, May 1987.