Statistical Analysis of Metal Gate Workfunction Variability, Process Variation, and Random Dopant Fluctuation in Nano-CMOS Circuits

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Abstract—This work for the first time estimates the influences of the intrinsic parameter fluctuations consisting of metal gate workfunction fluctuation (WKF), process variation effect (PVE) and random dopant fluctuation (RDF) on 16-nm-gate planar metal-oxide-semiconductor field effect transistors (MOSFETs) and circuits. The WKF and RDF dominate the threshold voltage fluctuation; however, the WKF brings less impact on the gate capacitance due to the screening effect of the inversion layer. The fluctuation of timing characteristics depends on the threshold voltage fluctuation, and therefore is proportional to the trend of threshold voltage fluctuation. For an amplifier circuit, the high-frequency characteristics, the circuit gain, the 3dB bandwidth, the unity-gain bandwidth power, and the power-added efficiency, are explored consequently. Similar to the trend of the cutoff frequency, the PVE and RDF dominate both the device and circuits characteristic fluctuations due to the significant gate capacitance fluctuations and the WKF is less important at this simulation scenario. The extensive study assesses the fluctuations on circuit performance and reliability, which can in turn be used to optimize nanoscale MOSFET and circuits.

Keywords- Emerging device technology, intrinsic parameter fluctuation, nanoscale MOSFET, circuit, coupled device-circuit simulation, modeling and simulation

I. INTRODUCTION

As the dimension of semiconductor device shrunk into nanoscale, variability of performance and yield in nanoscale complementary metal oxide semiconductor (CMOS) devices are great of interest. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, fluctuations in process parameters, and other factors, are known as indispensable components of the robust circuit design procedure. For state-of-art nanoscale CMOS circuits and systems, the intrinsic device parameter fluctuations that result from line edge roughness [1], the granularity of the polysilicon gate [2], random discrete dopants [3-11] and other causes, have substantially affected signal system timing [10,11] and high frequency characteristics [9]. Diverse simulation and suppression approaches have recently been presented to investigate intrinsic parameter fluctuations in semiconductor devices [1-8] and circuits [9-11]. Among these approaches, the metal-gate and high-κ are key technologies for the reduction of intrinsic parameter fluctuations. However, the use of metal as a gate material introduces a new source of random variation due to the dependency of workfunction on the orientation of metal grains [12,13]. Investigation of the impacts of the workfunction fluctuation on both CMOS device and circuit characteristics is lack. Additionally, the circuit performance may depend on different device characteristics. The dominance term of the circuit characteristic fluctuation should be identified.

Therefore, we herein estimate the influences of the intrinsic parameter fluctuations (metal gate workfunction variability (WKF), process variation effect (PVE), and random dopant fluctuation (RDF)) on 16-nm planar CMOS circuits. Instead of using compact models, the characteristic fluctuations of circuit were investigated using 3D device-circuit coupled simulations [9,14] to ensure the best accuracy. The preliminary results show that the WKF and RDF affect device threshold voltage (Vth) most and impact the delay time of inverter. The significant Vth fluctuation of PMOS induced by WKF demonstrates the increasing importance of WKF in nanoscale device and circuit. The impact of intrinsic parameters on high-frequency characteristics is then examined. Rather different to the results of DC characteristic fluctuation, WKF results in a less impact on high-frequency characteristic owing to the small gate capacitance fluctuation. The study on the intrinsic parameter fluctuations with emphasis on devices and circuits’ variability may benefit CMOS design and technology in sub-22-nm era.

The paper is organized as follows. Section II introduces the simulation technique for studying the effect of intrinsic parameter fluctuations in nanoscale devices and circuits. Section III studies the characteristic fluctuations in 16-nm-gate devices and circuits. Finally, conclusions are drawn and the future work is suggested.

II. SIMULATION METHODOLOGY

The devices we investigated are the 16-nm-gate bulk MOSFETs (width: 16 nm) with amorphous-based TiN/HfSiON gate stacks with an EOT of 1.2 nm [12]. The nominal channel doping concentration of the device is 1.48×10¹⁸ cm⁻³ and the Vth are calibrated. The RDF simulation mainly follows our recent work [6-9], in which 758 dopants are randomly...
generated in a large cube, in which the equivalent doping concentration is \(1.48 \times 10^{18} \text{ cm}^{-3}\), as shown in Fig. 1(a). The large cube is then partitioned into sub-cubes, in which the number of dopants may vary from zero to 14, and the average number is 6 (b)-(d). These sub-cubes are equivalently mapped into the device channel for the 3D device simulation with discrete dopants (e). The gate area of nanoscale devices is composed of a small number of grains and the distribution follows (g). The PVE induced \(\sigma_{V_{th}}\) fluctuation is estimated from the \(V_{th}\) roll-off characteristics. (i) Presents the tested common-source amplifier and inverter circuits in this study.

For WKF, considering the sizes of metal grains and the gate area of the devices, the gate area of nanoscale devices is composed of a small number of grains, as shown in Fig. 1(f). Since each grain orientation has a different workfunction, the gate workfunction should be modeled as a probabilistic distribution rather than a deterministic value. Therefore, a statistically-sound Monte-Carlo approach is advanced here for modeling such a probabilistic distribution. The gate area of nanoscale transistor is partitioned into several parts according to the average grain size. Then the grain orientation of each part and total gate workfunction are estimated based on properties of metal as shown in Fig. 1(g) [13]. Furthermore, we apply the statistical approach to evaluate the effect of PVE, as shown in Fig. 1(h), in which the magnitude of the gate length deviation and the line edge roughness follows the projections of the ITRS 2007. The PVE includes the gate length deviation and the line edge roughness, whose magnitude follow the projections of the ITRS 2007. Figures 1(i) illustrates the inverter and common-source amplifier for test, respectively. To properly capture the circuits’ characteristic fluctuations, instead of compact model approach, a 3D device-circuit coupled simulation is employed [9]. A sinusoid input wave (0.5 V offset voltage with frequency from 1x10^6 Hz to 1x10^13 Hz.) is used for studying the high-frequency characteristics of amplifier.

### III. RESULTS AND DISCUSSION

The \(V_{th}\) fluctuations for planar NMOS and PMOS devices are examined in Figs. 2(a) and 2(b). The total \(V_{th}\) fluctuation is given by according to the independency of the fluctuation components:

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\sigma_{V_{th,total}}^2 = \sigma_{V_{th,RDF}}^2 + \sigma_{V_{th,WKF}}^2 + \sigma_{V_{th,PVE}}^2
\]

in which the \(\sigma_{V_{th,RDF}}, \sigma_{V_{th,WKF}}, \text{ and } \sigma_{V_{th,PVE}}\) are the random-dopant-, workfunction-fluctuation- and process-variation-induced \(V_{th}\) fluctuation, respectively. The results show that the RDF dominates the \(V_{th}\) fluctuation in NMOSFETs; however, for the \(V_{th}\) fluctuation of PMOS, the WKF becomes the dominating factor because of the large deviation of the
Delay time (tLH) fluctuations and WKF introduces a largest tLH fluctuation due to the large workfunction for different grain orientation in Fig. 1(g). The WKF, PVE, and RDF fluctuated Cg are presented in Figs. 2(a)-2(c), where the solid line shows the nominal case with 16-nm-gate, 1.48x10^18 cm^-3 channel doping and the dashed lines are fluctuated cases. The different intrinsic parameter fluctuation induced rather different C-V characteristics. Figure 2(d) summarizes the gate capacitance fluctuations ($\sigma C_g$) with 0.5 V and 1.0 V gate bias. Different to the results of $V_{th}$ fluctuation, the WKF brought less impact on gate capacitance fluctuation. Moreover, the RDF and PVE dominate the gate capacitance fluctuations at 0.5 and 1.0 gate bias, respectively. Our preliminary results show that the impacts of the WKF on Cg is reduced significantly at high gate voltage ($V_{th}$) due to the screening effect of inversion layer of device, which screens the variation of surface electrostatic potential and decreases the fluctuation of gate capacitance. The screening effect resulting from the inversion layer also decreases the RDF induced gate capacitance fluctuation at high gate bias; however, the screening effect of inversion layer is weakened by discrete dopants positioned near the channel surface. Notably, the PVE brings direct impact on gate length and therefore influences the gate capacitance. The PVE induced gate capacitance fluctuation is independent of screening effect and should be noticed when the transistor operated in high gate bias, as shown in Fig. 2(d).

Figures 4(a) and 4(b) shows the high-to-low and low-to-high delay characteristic of the output signal and the high-to-low delay time (tHL) and low-to-high delay time (tLH) are calculated in Figs. 4(c) and 4(d). Since the tHL and tLH are dependent on the $V_{th}$ fluctuations for NMOS and PMOS devices, respectively, according to the results of Fig. 2, the RDF and WKF are the dominating factors in timing fluctuations and WKF introduces a largest tLH fluctuation due to the large workfunction deviation in scaled gate area as shown in Fig. 1(f). The WKF has shown its increasing importance in nanoscale transistor, especially in PMOS characteristics. Notably, we herein use the transistors’ gate capacitance as the load capacitance (Cload) and focused on the device intrinsic parameter fluctuation induced circuit variability. The result of the nominal propagation delay may be changed as we take an additional load capacitance into consideration. Power-added efficiency (PAE), as defined below, is a measure for the power conversion efficiency of power amplifiers, as shown in below:
where $P_{\text{out}}$, $P_{\text{in}}$, and $P_{\text{DC}}$ are output, input and DC supplied power, respectively. Figure 5(a) shows the nominal output power ($P_{\text{out, nom}}$), gain, and power-added-efficiency (PAE) of the common-source power amplifier as a function input power ($P_{\text{in}}$) in which the channel is continuously doped and the operation frequency is 10 Hz. Owing to the limitation of output signal swing, the nominal value of $P_{\text{out}}$ is saturated after 10 dBm input power, which in turn decreases the gain of circuit. The gain fluctuations resulted from WKF, PVE, and RDF are explored in Figs. 5(b)-5(d). Since the PVE and RDF dominate gate capacitance fluctuations due to significant affected the channel length and depletion width, the PVE, and RDF play important roles in high frequency characteristic fluctuation, as shown in Figs. 5(e) and 5(f). Effects of WKF in high frequency characteristics may be neglected in this scenario. The enlarged gain fluctuation with increasing input power is resulted from the larger portion of device operation in linear region. While the magnitude of input signal swing increases larger than 0.178 V (input power larger than 15 dBm), some part of device operation enters cutoff region and therefore decreases the gain fluctuation. The high frequency characteristic fluctuation is then investigated in Fig. 6(a), in which the fluctuation of high frequency circuit gain, 3dB bandwidth, and unity-gain bandwidth are extracted, Figs. 6(b)-6(d). Similar to the result of Fig. 3, the RDF and PVE dominates the high frequency characteristic fluctuations and WKF become less important in this analyzing scenario.

IV. CONCLUSIONS

In this study, we have estimated the influences of the intrinsic parameter fluctuations in 16-nm planar MOSFETs and circuits. Our preliminary results have shown that the WKF and RDF dominate the $\sigma V_{\text{th}}$ and therefore rule the delay time of the explored digital inverter circuits. The fluctuation of delay time depends on the $V_{\text{th}}$ fluctuation which follows the trend of $V_{\text{th}}$ fluctuation. The WKF effect in PMOSFETs may bring significant impact on $t_{\text{LH}}$ characteristics due to the large difference of workfunction in different grain orientation. For the high-frequency characteristics, the circuit gain, the power, and the power-added efficiency were also explored. Similar to the trend of the device cutoff frequency, the PVE and RDF dominate the device and circuits characteristic fluctuations and the WKF shows less impact on high-frequency characteristic owing to the small gate capacitance fluctuation. The sensitivities of circuit performance with respect to device parameter fluctuation have been reported. It is necessary to include both the WKF and RDF effects in studying digital circuit reliability; however, for the high frequency applications, the PVE and RDF effect are dominating factors.

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