Random Fluctuations in Scaled MOS Devices

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***Abstract*— Today, variability is recognized as a major obstacle for continuing MOS transistor miniaturization. Among various kinds of variability, this paper mainly focuses on random fluctuation, which is caused by microscopic perturbations, such as discreteness of charges and atomic scale structural irregularity. Some recent research results for quantitatively understanding the causes of random fluctuation are reviewed. Methods of reducing random fluctuation will be discussed.**

Keywords- variability; variation; random dopant fluctuation; MOSFET; large scale integrated circuit

I. INTRODUCTION

In order to properly operate today's extremely large scale CMOS integrated circuits, where hundreds of millions of transistors are gathered to realize complex functions, it is desirable that all the FETs used are manufactured such that their characteristics are identical to, or within small tolerance from the target characteristics. However, due to several reasons, this is becoming more and more difficult today [1][2]. In particular, the increase of random fluctuation is a serious obstacle for continuing further scaling down of transistors. Random fluctuation here refers to a kind of variability that exhibit no correlation between neighboring devices (Fig.1). The absence of correlation suggests that it is caused by some microscopic perturbations, such as random placement of discrete charges, atomic scale irregularity of gate dielectrics, and so on. Since the change of FET characteristics caused by a fixed amount of perturbation increases (i.e. sensitivity increases) as the FET size is reduced, random fluctuation rapidly increases as FETs are shrunk, which may result in failure of further scaling down of integrated circuits. Therefore, it is very important to quantitative understand the origins of random fluctuation, and appropriate measures are taken.

In this paper, after brief overview of variability, some recent experimental activities directed towards quantitative analyses of measured random fluctuation [3] are reviewed. Then, measures to reduce random fluctuation and future prospect will be discussed.

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II. OVERVIEW OF VARIABILITY

There are diverse kinds of variability, which are different in their origins and behavior. Since, not only random fluctuation, but also many of other kinds of variability are becoming more serious due to miniaturization, they will be briefly reviewed first. Variability in integrated circuits is usually classified by its correlation between multiple transistors placed at different positions. One typical way of such classification is schematically shown in Fig.2. In one aspect, such classification is useful for circuit design purposes. Circuits are composed of multiple devices which are functionally interrelated. Therefore, to design circuits by properly accommodating variability, different strategies for managing the design tolerance are required depending on the correlation [4]. In another aspect, spatial correlation is closely related to the physical mechanisms or origins of variability. According to Fig.2, variability is classified into the following five categories.

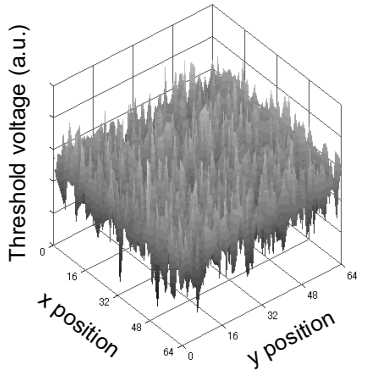

Fig.1 Example of random threshold voltage fluctuation. Closely located identically designed 4k transistors are measured

(a) *Wafer-to-wafer variation* is caused, for example, by some change in machine conditions along time of manufacturing apparatus.

(b) *Wafer level variation* can be caused by any on-wafer non-uniformity in e.g. temperature and gas flow. Time dependence of lithography exposures may be also responsible.

(c) *Die level variation* typically originates from lithography steps, because pattern exposure is performed die-by-die. It may be caused either by imperfection in reticles or non-ideality in lens systems.

(d) *Layout dependent* variation exhibits spatial periodicity, as does die level variation, but is different in that it is strongly correlated with the specific layout of patterns, such as density, distance from the neighboring patterns, etc. Existence of nearby patterns may affect final transistor shapes during lithography (optical proximity effect) and etching (micro loading effect). Pattern dependence of mechanical stress and annealing temperature may be also responsible.

(e) *Random fluctuation* is the kind of variability that exhibits no spatial correlation, as already explained.

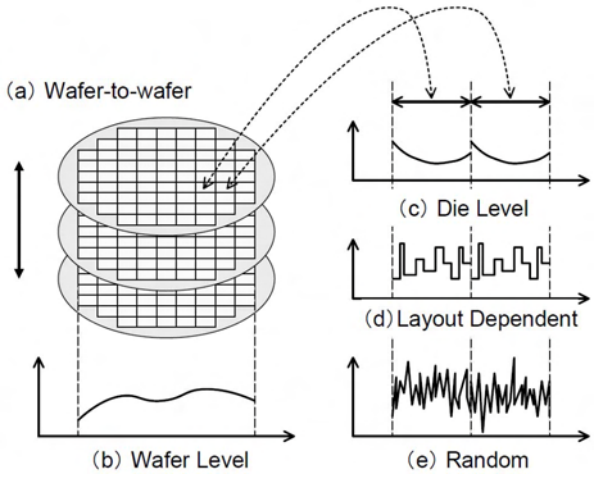

Fig.2 Classification of Variability.

While categories (a) and (b) have always been concerns for integrated circuit manufacturing, (c) to (e) appear to be attracting more attention after CMOS miniaturization entered sub-100nm regime. Major reasons for this situation would be as follows.

(1) *Reduced transistor dimensions*: As the transistors become smaller, the sensitivity of the devices to any perturbation will increase. As a result, various kinds of variability that were once not important emerged.

(2) *Reduced power supply voltage*: Power supply voltage has been reduced to around 1V, to keep the power consumption low and maintain long term reliability. If the same amount of change in device characteristics occurs, its impact will become larger as the power supply voltage is reduced.

(3) *Limitation by lithography wavelength* [5]: Currently, the wavelength widely used for lithography is 193nm, which is much larger than the minimum feature sizes of state-of-the art LSIs. This results in increased die level and layout dependent variability of exposed pattern shapes. Though this can be, in part, offset by resolution enhancement techniques (RET) and mask data handling called optical proximity correction (OPC), layout dependence will remain to some extent.

(4) *Use of mechanical stress*: Mechanical stress is now intentionally used to enhance the drive performance of FETs, as a 'technology booster' [6]. Increased mechanical stress would increase layout dependence.

(5) *Introduction of new fabrication techniques*: One example is the use of rapid thermal processing. To shrink transistors, it is necessary to shorten thermal annealing time to reduce impurity diffusion. The resulting non-equilibrium heating of the wafer may increase variability [2]. Another example frequently discussed in literature is chemical mechanical polishing (CMP) used for STI and interconnect fabrication [7]. Both will degrade layout dependent variability.

Among the variability categories, (a) to (c) can be suppressed by improving the uniformity of manufacturing process. As for (d), in addition to the improvement of manufacturing process, such as introduction of short wavelength EUV lithography, countermeasures from the design side are also effective. These would include use of restricted design rules allowing less irregularity of patterns, more sophisticated OPC, and smart circuit design taking advantage of the predictability of the layout dependence. Therefore, (a) to (d) are extrinsic, in that they are directly controllable by process and design. However, random fluctuation (e) seems to be less controllable due to its microscopic nature, and is rather intrinsic.

III. Impact of Random Fluctuation

Currently, random fluctuation is one of the most serious challenges to overcome in order to continue scaling down of FETs. In the past, it was a problem only for designing analog circuits, and has been traditionally called 'mismatch' [8]. Today, due to the size reduction, random fluctuation is a problem also for digital circuits. Fig.3 shows measured threshold voltage (V_{TH}) distribution of 65nm generation n+ poly silicon gate n-channel FETs (NFETs) [9]. One million transistors were regularly arranged in an addressable device matrix array (DMA), in which all the transistors can be accessed from external terminals to perform dc measurements of individual FETs. Since the FETs are located in a small area, only random fluctuation can be extracted. Empirically, it is reported that random fluctuation of V_{TH} often takes on nearly ideal normal distributions, as shown in Fig.3.

Among various digital components in CMOS LSIs, static random access memory (SRAM) is most vulnerable to random fluctuation. The reasons are as follows. Firstly, smallest transistors must be used in SRAM cells to increase the memory capacity. As a result, the SRAM transistors exhibit larger fluctuation than the others. Secondly, the number of cells is large (a few million or more per chip). The standard deviation (σ) of V_{TH} in Fig.3 is only 43mV. However, if there are 1M transistors, the expected largest deviation of V_{TH} is as large as $\pm 5\sigma$, and even $\pm 6\sigma$ (520mV in range for this example) must be

considered to achieve sufficient yield of products, assuming normal distribution. Such large possible deviation makes functional SRAM design difficult. Thirdly, SRAM cells cannot enjoy averaging effect. In logic circuits, logic gates are serially connected, and the total delay is a summation of delays of many gates. Since the deviation of delay caused by random fluctuation may be both positive and negative due to the lack of correlation, total deviation divided by mean delay (i.e. relative delay deviation) decreases as the number of gates increases, alleviating the impact of random fluctuation on logic circuits. However, such benefit is absent in SRAM cells. Since SRAM takes up significant portion of total die area today, random fluctuation may set a limit on the scaling of integrated circuits.

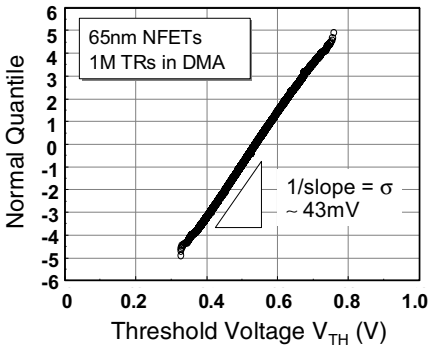

Fig.3 Example of measured random V_{TH} fluctuation.

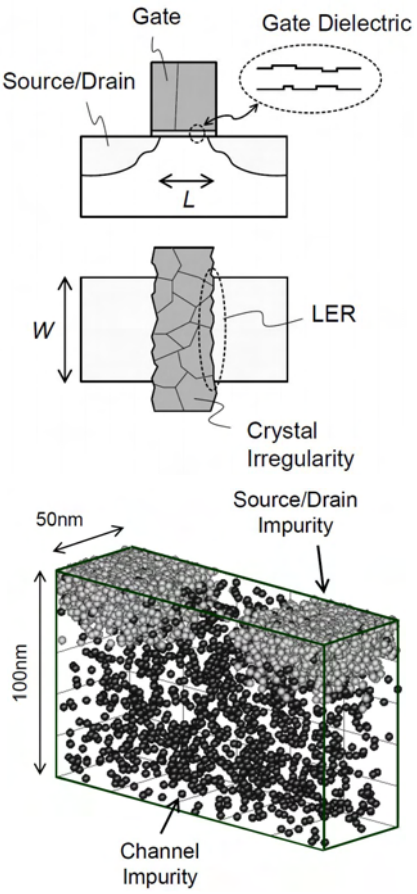

Fig.4 Possible causes of random fluctuation.

IV. Analyses of Random Fluctuation

There are many possible causes of random fluctuation (Fig.4), such as random placement of discrete impurities (random dopant fluctuation = RDF) [10], atomic scale gate dielectric roughness [11], line edge roughness (LER) [12], and crystalline irregularity of gate materials (grain boundary locations [13], crystalline orientation, poly depletion, etc.). To choose proper countermeasures, it is very important to quantitatively understand the extent to which each mechanism contributes to random fluctuation. In this section, a recent attempt of quantitatively analyzing random fluctuation [3] is explained. While, direct measurement or observation of microscopic effects by physical analyses [14] requires considerable effort and skill, collecting electrical data as in Fig.3 is much easier. If such data for various kinds of transistors fabricated by different conditions or in different fabs are collected and properly compared, it would be possible to extract quantitative information about the root causes. Motivated by this consideration, a special normalization method for comparing electrical fluctuation data was developed [15]. Then, it was used to compare devices of various origins to analyze the causes of random fluctuations.

A. Normalization for Comparing Random Fluctuation

Normalization of measured data is sometimes useful for understanding the physics. One example would be 'universal mobility plot'. It is well known empirically that, if effective mobility μ_{EFF} of FETs is plotted versus effective normal field

$$E_{EFF} = (Q_{DEP} + \eta Q_{INV})/\varepsilon_{SI} \quad (1)$$

where Q_{DEP} and Q_{INV} are depletion layer and inversion layer charge per area, ε_{SI} is permittivity of silicon, η is 1/2 (nFET) or 1/3 (pFET), μ_{EFF} vs E_{EFF} plots for different channel doping concentration N_{SUB} and equivalent gate dielectric thickness T_{OX} tend to fall on a single curve [16]. By using this plot, it is possible to do meaningful comparison of mobility between devices, even if the design parameters (T_{OX} and N_{SUB}) are different. It is believed that this has helped enhance understanding of mobility behavior (e.g. dependence on gate dielectric materials) by increasing the amount of available data for mobility analyses.

A well known way of normalizing random fluctuation is to use 'Pelgrom plot'. If random fluctuation is determined by a linear summation of contributions from segments of the channel area,

$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{LW}} \quad (2)$$

where σ_{VT} is standard deviation of V_{TH}, L is channel length, and W is channel width [17]. An example of Pelgrom plot is shown in Fig.4a, where FETs with three different T_{OX} values are shown. If T_{OX} is the same, the data fall on a straight line, in agreement with (2). Therefore, the slopes A_{VT} can be taken as random fluctuation normalized with respect to the FET channel size. It can be used to judge which of FETs produced by different process is superior or inferior with respect to the magnitude of random fluctuation. However, A_{VT} is not suitable for analyzing the physics, since it depends on the FET design

parameters. For example, A_{VT} depends on T_{OX}, as is clear from Fig.4a, though all the FETs are manufactured in the same fab and lot. To overcome this shortcoming, a new normalization plot was proposed. It is based on an equation

$$\sigma_{VT} = B_{VT}\sqrt{\frac{T_{INV}(V_{TH}+V_0)}{LW}} \quad (3)$$

where T_{INV} is electrical gate dielectric thickness (T_{OX} plus inversion layer and gate depletion thickness), and V_0 is potential difference between Fermi-level and band edge at inversion (approximately 0.1V at room temperature for conventional dual poly-Si gate CMOS FETs). By using B_{VT} in (3), σ_{VT} is normalized with respect to the design parameters T_{OX} and V_{TH}, in addition to L and W. Fig.5 shows the new normalization plot for the same data in Fig.4b. All the data points now fall on a single line, regardless of the T_{OX} values.

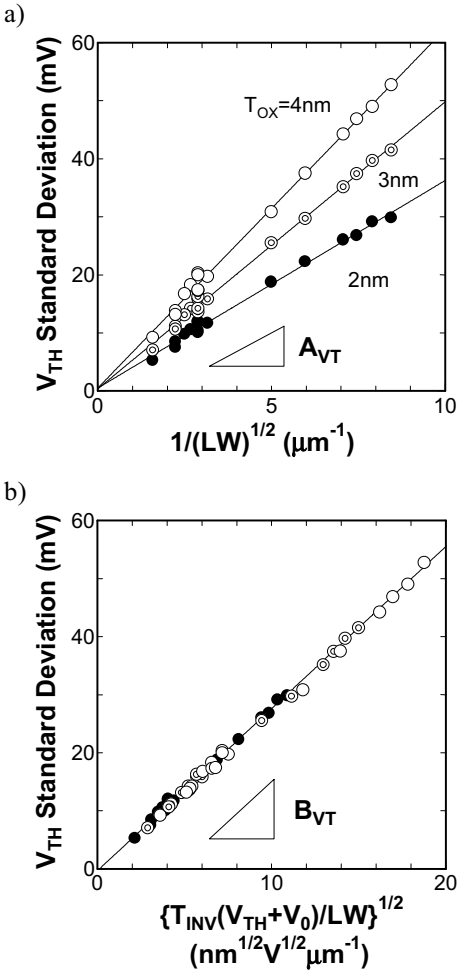

Fig.5 Examples of a) Pelgrom plot and b) new normalization plot.

Equation (3) was derived as follows. Among various causes of random fluctuation, it is considered that RDF should take up significant portion of the entire random fluctuation. Therefore, RDF is chosen as a *gauge* for the normalization. According to a simple analytical model, σ_{VT} due to RDF for uniformly doped channel is given by

$$\sigma_{VT} = \frac{q}{C_{INV}}\sqrt{\frac{N_{SUB}W_{DEP}}{3LW}}, \quad (4)$$

where N_{SUB} is channel impurity concentration, W_{DEP} is channel depletion region width, and $C_{INV}=\varepsilon_{OX}/T_{INV}$ [18]. V_{TH} is given by

$$V_{TH} = V_{FB} + \phi_S + \frac{qN_{SUB}W_{DEP}}{C_{INV}}. \quad (5)$$

Combining (4) and (5), we obtain

$$\begin{aligned}\sigma_{VT} &= \sqrt{\frac{q(V_{TH}-V_{FB}-\phi_S)}{3LWC_{INV}}} \\ &= \sqrt{\frac{q}{3\varepsilon_{OX}}}\sqrt{\frac{T_{INV}(V_{TH}-V_{FB}-\phi_S)}{LW}} \\ &\equiv \sqrt{\frac{q}{3\varepsilon_{OX}}}\sqrt{\frac{T_{INV}(V_{TH}+V_0)}{LW}}.\end{aligned} \quad (6)$$

By comparing (4) and (6), it is clear that B_{VT} is σ_{VT} normalized by ideal RDF. B_{VT} should be constant, if RDF is the only cause of random fluctuation, and the channel doping non-uniformity is small.

To validate the normalization method, B_{VT} was calculated by using Monte Carlo three-dimensional atomistic TCAD simulations, considering only RDF as the source of fluctuations. Multiple devices were generated, randomly placing channel impurity atoms, and the simulated variations of V_{TH} were obtained. Fig.6 shows the simulated B_{VT}. It was confirmed that B_{VT} should be indeed constant, if only RDF exists. It was also found that simulated B_{VT} is slightly larger than the theoretical value $(q/3\varepsilon_{OX})^{1/2}$. It is considered that this discrepancy comes from the oversimplification of the analytical model, where the effects of non-uniformity in the lateral direction are not taken into account.

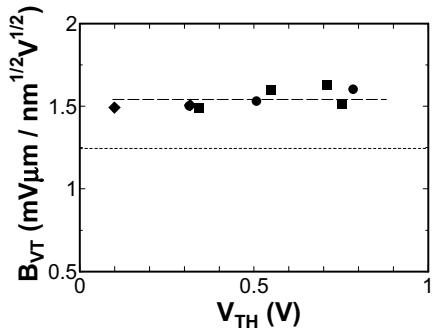

Fig.6 B_{VT} of uniformly doped channel FETs by TCAD simulations.

B. Comparison of Multiple Fabs and Technologies [3]

The proposed method was used to compare measured data of conventional dual poly silicon gate nFETs and pFETs from a wide variety of fabs and technologies; 65nm experimental devices, 0.35um experimental devices (fabricated 10 years ago) and 65 to 90nm technology transistors (tech-A and D: LSTP oriented, tech-B: HP oriented, tech-C: LOP oriented). I/O transistors are included. Care was taken to extract only random fluctuation, eliminating other kinds of variability. This was achieved by measuring only matched pair transistors or device

matrix arrays. To simplify the analyses, drain bias V_{DS} was kept low, and moderately or very long channel transistors were used to avoid the interference of short channel effects and LER.

A_{VT} and B_{VT} for the pFETs are shown in Fig.7. A_{VT} scatters significantly, reflecting the fact that V_{TH} ranges from 0.2V to 2.2V, and T_{INV} from 2 to 15.4nm. However, by using the new normalization, the data converge into almost the same B_{VT} value for all the devices (B_{VT}~1.7). (Hereafter, units of A_{VT} and B_{VT} are (mV·μm) and (mV·μm/nm$^{1/2}$V$^{1/2}$) if not specified.) This B_{VT} value is close to the TCAD results in Fig.6 assuming only RDF. These results strongly suggest that, as for the pFETs, random V_{TH} fluctuation is dominated by RDF, for a wide variety of the device generations, fabs and technologies.

A_{VT} and B_{VT} for the nFETs are shown in Fig.8. Again, though A_{VT} significantly scatters, B_{VT} plots fall into a relatively narrow range of 1.8~3.2. However, clear difference was found between nFETs and pFETs. B_{VT} for nFETs is larger than that for the pFETs, and appreciable difference between different devices remains. This shows that some fluctuation mechanism(s) in addition to simple RDF should significantly contribute to the nFET fluctuations.

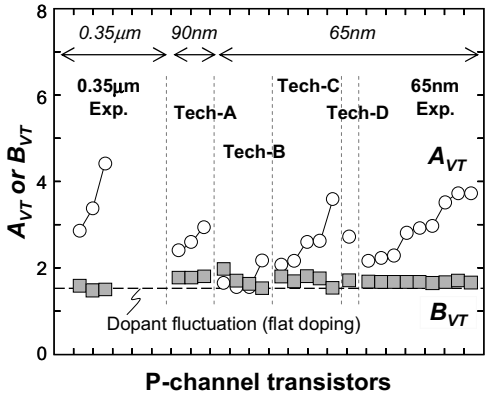

Fig.7 A_{VT} and B_{VT} for various dual poly gate pFETs from multiple fabs and technologies.

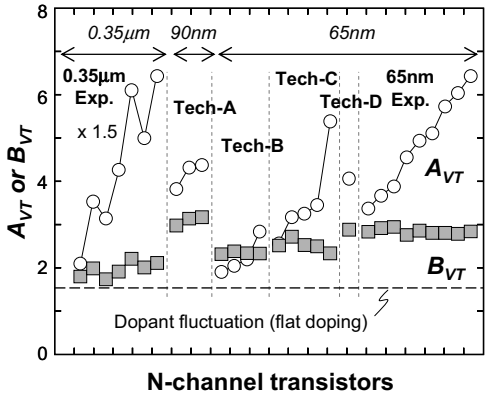

Fig.8 A_{VT} and B_{VT} for various dual poly gate nFETs from multiple fabs and technologies.

C. Analyses based on B_{VT}

The results above demonstrate that, while RDF is indeed a major mechanism that causes random fluctuation, some additional fluctuation mechanism(s) should also exist, at least in nFETs. It is important to clarify this additional mechanism to reduce nFET fluctuation, and achieve further densification of CMOS LSIs. It is considered that candidates for the additional mechanism should be classified into different groups, as shown in Fig.9. V_{FB} variation (gate originated) may be caused by any poly-Si crystal irregularity. T_{INV} variation (dielectric originated) may be caused by non-uniform poly-Si depletion, as well as actual oxide thickness variation. Possible causes of non-ideal charge distribution (substrate originated) would include existence of extra random charges due to boron pile-up at the surface, surface states, charge traps, and also correlated boron distribution [10]. Note that, since relatively long channel devices are used in Figs.7 and 8, only area related mechanisms (i.e. those expected to follow the $1/(LW)^{1/2}$ relationship) are considered.

To distinguish between these possibilities, an effective experimental approach is to examine the response of random fluctuation to the transistor design parameters T_{INV} and N_{SUB}. For example, impact of V_{FB} variation on V_{TH} will not be affected by N_{SUB} change, whereas that of T_{INV} variation will increase as N_{SUB} increases. Fig.10 shows expected response of B_{VT} on some of the fluctuation causes, based on simple considerations as explained above.

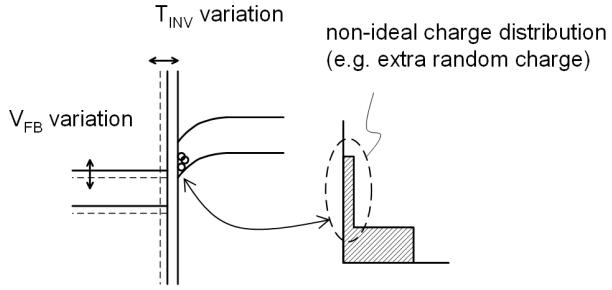

Fig.9 Possible additional mechanisms.

Cause	Device design parameters	
	N_{SUB} increase	T_{INV} increase
V_{FB} variation	↘	↘
T_{INV} variation	↗	↘
Non-ideal charge	depends	depends

Fig.10 Expected response of B_{VT}.

Fig.11 shows measured dependence of B_{VT} on the design parameters, where T_{INV} and N_{SUB} are systematically varied. These data are also plotted in Figs.7 and 8, which are labeled "65nm exp." It is rather controversial that the dependence of B_{VT} on T_{INV} and N_{SUB} is very weak, not only for the pFETs, but also for nFETs. As for the pFETs, since RDF seems to be dominant, it is natural that B_{VT} is constant. However, there is no apparent reason that nFET σ_{VT} becomes constant after being normalized by RDF. As shown in Fig.10, gate and dielectric originated mechanisms do not agree with the almost constant nFET B_{VT}. This suggests that the increased nFET random

fluctuation is caused by some substrate originated mechanisms, at least for the particular FETs examined here. However, though various mechanisms are currently discussed [19][20], further study is necessary to come to the final conclusion. It is also mentioned that the data shown in this section are all for FETs with poly-Si gate stacks. Inclusion of metal gate / high-k FET data remains to be done.

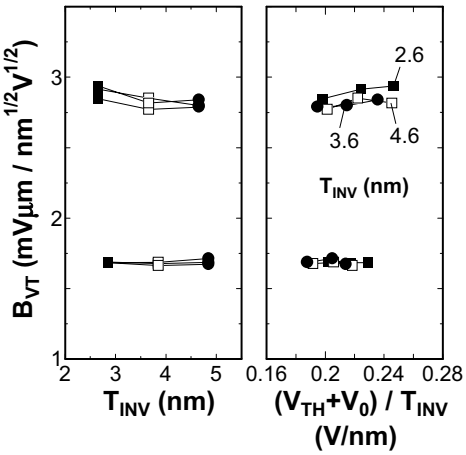

Fig.11 Dependence of B_{VT} on FET design parameters. $(V_{TH}+V_0)/T_{INV}$ equals constant $\times N_{SUB}W_{DEP}$.

V. Reduction of Random Fluctuation

To continue CMOS scaling, further increase of random fluctuation must be avoided. Since it is clear that RDF is either dominant or major factor that determines random fluctuation, methods of reducing RDF are necessary. Since the increased nFET fluctuation also seems to be caused by some charge residing in the substrate, some of these may be also effective for suppressing the additional fluctuation mechanism. These will include the following.

(a) *Controlling vertical doping profile* [18]: σ_{VT} by RDF can be reduced without changing nominal V_{TH} by using steep retrograde channel profiles (i.e. selective low doping at the surface). Actually, very low B_{VT} of around 1.0 is experimentally obtained for long channel pFETs. However, this effect becomes difficult to achieve for sub-100nm devices because the required steepness increases as the channel length decreases.

(b) *Controlling gate work function* [21]: It is reported that by slightly modifying the gate work function (this corresponds to modifying V_0 in (3)), N_{SUB} can be reduced, keeping V_{TH} the same. This will result in the reduction of σ_{VT}, according to (4). However, the effectiveness is limited for bulk FETs, because too much lowering of N_{SUB} will degrade short channel effects, and will increase fluctuation due to LER.

(c) *Reduction of gate dielectric thickness* [2][22]: This seems to be the most effective way for reducing RDF of bulk FETs. According to (3), σ_{VT} will be proportional to $T_{INV}^{1/2}$, if V_{TH} is kept constant by increasing N_{SUB}. If N_{SUB} is kept the same (e.g. by adjusting V_0 to keep V_{TH} the same), σ_{VT} can be even reduced in proportion to T_{INV}. However, it should be noted that reducing T_{INV} may require reduction of power supply voltage. This will partly offset the effect of reduced σ_{VT}, since lowering the voltage will increase the vulnerability of the circuits.

(d) *Adopting new device architecture*: Possible new device architectures include ultra-thin body SOI FETs [23], FinFETs [24] and nano-wire FETs [25]. In these devices, since short channel effect is controlled by their structure, rather than impurity, zero channel doping is possible. Therefore, ideally, RDF can be eliminated. Reduced random fluctuation by using such devices is already reported by several groups [26][27]. Since V_{TH} cannot be adjusted by N_{SUB} in such devices, controlling V_{TH} through gate stack engineering becomes mandatory. Other challenges are the realization of extremely thin/narrow channel (less than a few tenth of L) and low parasitic resistance.

By using new device architectures, it would be possible to substantially reduce random fluctuation. However, it should be noted that, if device miniaturization continues, sensitivity of a device to any perturbation also continues to increase. For example, even a single charge random perturbation may become critical for ultimately scaled FETs [28]. Therefore, random fluctuation will be an important subject as long as miniaturization continues.

VI. Summary

Among various kinds of variability, random fluctuation is a serious problem that needs to be overcome for FET miniaturization. While RDF seems to dominate pFETs, some additional fluctuation mechanism(s) exist in nFETs, which should be identified and controlled. Since miniaturization increases sensitivity of FETs to microscopic perturbation, random fluctuation will continue to be an important issue for scaling FETs.

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