Resonant Injection Enhanced Field Effect Transistor for Low Voltage Switching: Concept and Quantum Transport Simulation

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***Abstract*—A Resonant Injection Enhanced Field Effect Transistor (RIEFET) device concept for low voltage switching has been developed. Two-dimensional electrostatically self-consistent ballistic quantum transport simulations of device operation are provided. To reduce simulation time, the two dimensional ballistic transport code was parallelized. The potential significance of parasitic phonon-assisted transport also is explored in quasi-one-dimensional simulations of transport through the resonant barrier.**

Keywords: Resonant tunneling transistor, Low-voltage switching, Quantum transport, Parallelization

I. INTRODUCTION

CMOS logic is rapidly approaching voltage scaling limits due to the physical process of thermionic emission of carriers over the channel barrier in the OFF state which restricts the subthreshold slope to or above $\ln(10)k_BT/q$, which is approximately 60 mV at room temperature. With multi-order of magnitude ON/OFF ratios and as much or more above threshold voltage required to provide sufficient drive current for rapid switching, this subthreshold leakage leads to minimum required supply voltages approaching half a volt, depending somewhat on application [1].

In this work we consider a novel "Resonant Injection Enhanced Field Effect Transistor" (RIEFET) concept that could potentially provide more sensitive gate control than a MOSFET particularly in the OFF state and, thus, lower supply voltage/power operation. The RIEFET design takes advantages of possibilities offered by use of III-V material systems. Although there are also many technological challenges to such use of III-V systems, these latter challenges are already being explored for the purpose of achieving ultimate CMOS [2,3]. The RIEFET would leverage this latter work on III-V MOSFETs to potentially greater benefit.

In a MOSFET the gate controls the barrier height to the channel. However, the injection efficiency of carriers with enough energy to enter the channel is roughly fixed for short channel devices (and within approximately a factor of two of the ideal of unity for high-performance Si devices). In the proposed RIEFET, as illustrated in Fig. 1, the use of a III-V multi-quantum well injection barrier in the conduction path adds gate control over injection efficiency to the gate control of the channel potential. In the ON state where the gate voltage is equal to the supply voltage, the injection barrier is designed to approach transparency through resonant tunneling, becoming a high-order band-pass filter for electrons, to provide high ON-state drive currents. In the OFF state with zero gate voltage, the inter-well resonances are eliminated and the injection efficiency is attenuated.

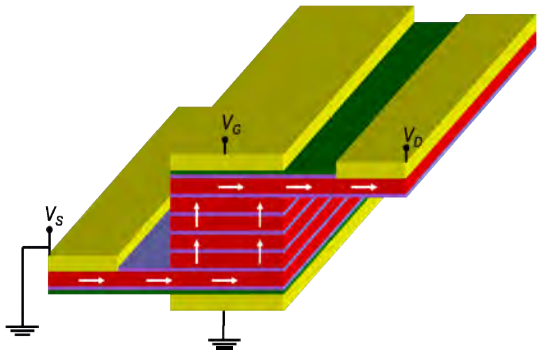

Figure 1. Schematic diagram of one realization of an RIEFET. White arrows show the nominal conduction path for charge carriers. A side-injection geometry is used to optimize tunneling area into the channel beneath the gate. For simulation purposes, for specificity, 7 nm thick GaAs quantum wells are separated by 1 nm AlGaAs tunnel barriers. The channel length under the gate is taken to be 30 nm. An additional 1 nm of material with a dielectric permittivity equal to that of AlAs is used to represent a high-k gate dielectric on top and an additional dielectric barrier on bottom, for a total barrier thickness 2 nm top and bottom. The source and drain contacts are separated from the gate region by 15 nm and 20 nm, respectively. The doping in the quantum well regions is $10^{18}/cm^3$, tailored to achieve a true flat-band under resonance in the ON state, which is set to a gate voltage V_G of 150 mV via suitable adjustment of the gate work-function. A 150 mV drain voltage V_D is also applied in the simulations of this work.

The basic concept of RIEFET can also be realized in alternative geometries, such as the one illustrated in Fig. 2. The difference between this structure and that of Fig. 1 is the use of two resonant tunneling structures here, one at each of the channel/well beneath the gate. Moving the drain contact should reduce its influence on the top gate, and should allow carrier capture in the top well to aid with drain current saturation beyond resonance. However, here we shall consider only the basic operation, leaving design optimization for future works.

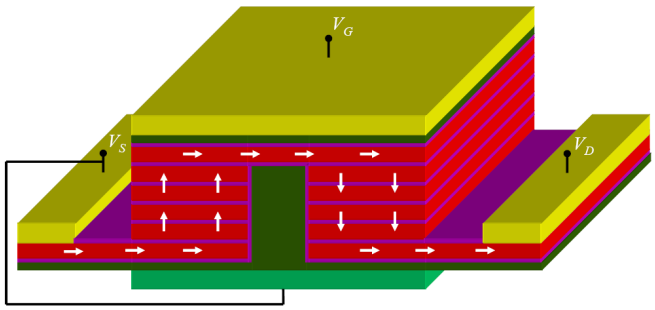

Figure 2. Schematic diagram of a Omega-shaped RIEFET.

Overcoming the technological challenges of III-V systems is still a work in progress, however. Here we consider the potential of the RIEFET through two-dimensional quantum transport simulation. A newly parallelized version of the basic simulation method described in [4] is used. In addition, the possibility of parasitic phonon-assisted transport is explored in quasi-one-dimensional simulations transport through the resonant barrier using the Schrödinger Equation Monte Carlo (SEMC) non-equilibrium Green's function method [5-7].

II. Simulation Results for a Prototype Design:

Fig. 3 shows ballistic quantum transport simulation results of drain current I_D vs. gate voltage V_G for the prototype RIEFET structure of Fig. 1, along with those for a double gate (DG) MOSFET for reference formed in the same material system, illustrating the potential for low-voltage operation. The reference DG-MOSFET had identical channel, barrier and gate dimensions, and identical source and drain doping. However, the conduction channel consisted of only the one quantum well between the gate dielectrics, the channel was left undoped, and both the top and bottom gates were biased at the same voltage. Identical voltages were considered in the simulations, although with a somewhat different gate work-function to obtain a similar threshold voltage. The simulated reference DG-MOSFET has essentially an ideal subthreshold slope of 60 mV/decade for a MOSFET, and an essentially unity injection efficiency so that the peak current is limited only by the source doping. Still, the much improved subthreshold characteristics of the RIEFET are apparent in Fig. 3(top). An ON/OFF ratio of over 10^4 was achieved for the RIEFET with a peak gate voltage equal to a supply voltage of only 150 mV. By comparison, the DG-MOSFET requires somewhat over twice the gate voltage swing to achieve the same ON/OFF ratio. And in terms of required drive currents for fast switching, the reduction in ON-state current seen in Fig. 3(bottom) is largely compensated for by the allowed supply voltage reduction to achieve the same ON/OFF ratio and the associated reduction in the charging current required for a given load capacitance.

The increased subthreshold swing, as designed, can be traced to gate control over the injection efficiency, as illustrated in Fig. 4, in which the transmission probabilities of injected carriers as a function of energy are compared for V_G = 150 mV (ON) and 0V (OFF). As seen, even for the electrons with enough energy to reach the channel directly below the gate, the injection efficiency is greatly reduced in the OFF state. Associated self-consistently obtained band edge profiles and electron densities for the ON and OFF states are shown in Fig. 5. In the ON-state the multiple quantum wells below the gate serve as a nearly transparent high-order band pass filter for electrons under near flat-band conditions. (Of course, one could

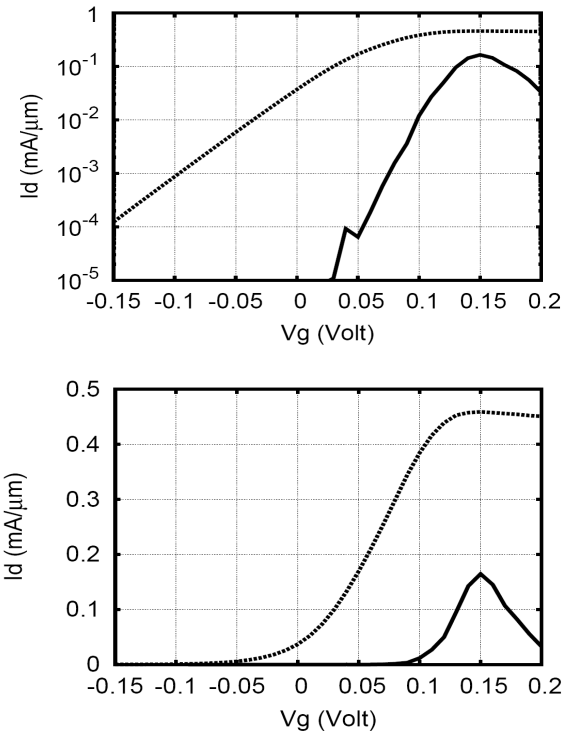

Figure 3. Two-dimensional ballistic quantum transport simulation results of $I_D - V_G$ characteristics for a prototype RIEFET (solid lines), and a reference DG-MOSFET (dashed lines) in the same material system, on log (top) and linear (bottom) current scales. The reference DG-MOSFET has an approximately ideal 60 mV/decade subthreshold swing (top) and near unity injection efficiency.

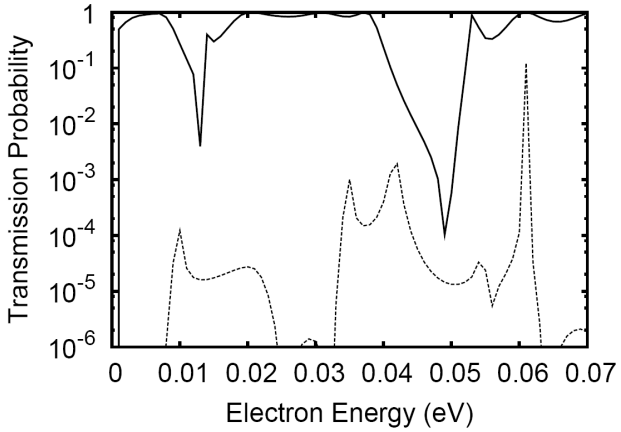

Figure 4. Transmission probabilities of injected carriers as a function of energy for V_G = 150 mV (ON) and 0V (OFF) shown over an approximately $3k_BT$ range. The zero energy reference in each case is the subband minimum energy in the channel directly below the gate to better compare the injection efficiency for carriers with sufficient energy to reach this gate-side (top) channel. In the OFF state there are, of course, also far few carriers that have sufficient energy to reach the gate-side channel.

design for resonance under non-flat-band conditions, but the design would be more complex.) In the OFF-state, the quasi-bound states of the well are misaligned destroying the inter-well resonances and reducing access to the top channel even for electrons with sufficient thermal energy to reach it.

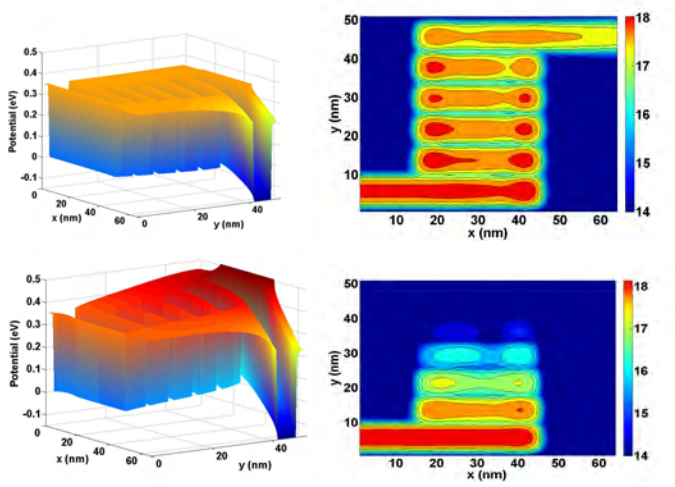

Figure 5. Band edge profiles (left) and the density of propagating charge carriers on a $\log_{10}$ scale (right) in the ON (top) and the OFF (bottom) states, respectively.

We also considered phonon-assisted leakage currents. However, a full two-dimensional quantum transport simulation with a physically accurate treatment of phonon scattering is not possible at this stage. Instead, we used a quasi-1D version [5,6] of our SEMC quantum transport simulator [5-7] to model polar optical phonon scattering in the vertical transmission path through the resonant tunneling structure, as illustrated in Fig. 6. For computational efficiency we considered "downhill" transport, relying on detailed balance to relate this back to "uphill" transport. The net increase in leakage current due to scattering was only approximately a factor of two.

III. Parallelization and Scalability

We parallelized the 2D ballistic simulation code to make it run on High Performance Computing systems, such as The University of Texas at Austin's *Ranger*. Computational time can be greatly shortened by utilizing hundreds of processors. The time needed to get a single data point for the I_D-V_G characteristics of RIEFET was reduced from 3.1 hours to 36 seconds (Fig. 7, top) corresponding to a speed up of approximately 300, when employing 512 processors (Fig. 7, bottom). According to Amdahl's law for parallelization,

$$\text{Speedup} = \frac{1}{(1-P)+P/N},$$

in which, P is the portion of a program that is parallelized and N is the number of CPUs in use. As shown in Fig. 7, 99.7% of the simulation time has been parallelized. Such penalization will be critical to future design optimization.

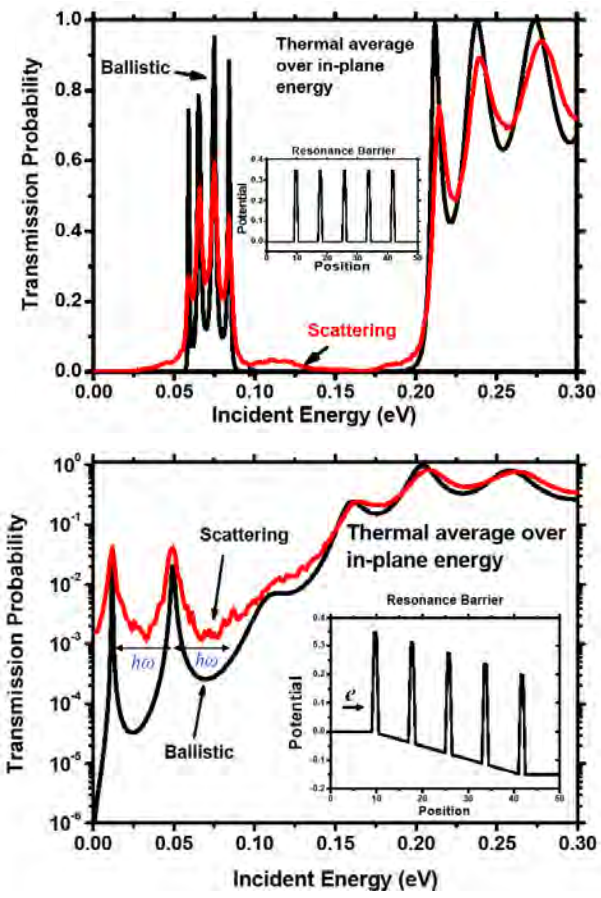

Figure 6. Transmission probability through the resonant tunneling structure potential profile in ON-state (top) and in the OFF-state (bottom) with a 150 meV potential drop, with and without scattering. Calculations were performed using a quai-1D version of the SEMC simulator [5,6].

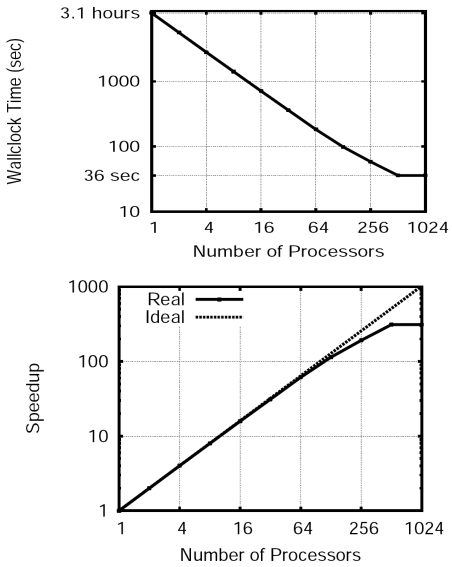

Figure 7. Parallelization scalability (top) and speedup (bottom) of the two-dimensional ballistic simuation code as number of processors is increased.

IV. Conclusion

A Resonant Injection Enhanced Field Effect Transistor (RIEFET) device concept has been developed. The RIEFET might allow for lower voltage operation than "end-of-the-roadmap" MOSFET technologies. In doing so, it could leverage the existing work on III-V MOSFET systems to perhaps greater benefit. Two-dimensional electrostatically self-consistent ballistic quantum transport simulations of device operation were provided, exhibiting the potential for operation of the prototype device design at supply voltages of approximately 150 mV. The potential significance of parasitic phonon-assisted transport was also explored in quasi-one-dimensional simulations of transport through the resonant barrier. To reduce simulation time by over two orders of magnitude and allow future design optimization, the two-dimensional ballistic transport code was parallelized.

Acknowledgment

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