Convex Channel Design for Improved Capacitorless DRAM Retention Time

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***Abstract*— A convex channel surface with $Si_{0.8}Ge_{0.2}$ is proposed to enhance the retention time of a capacitorless DRAM Generation 2 type of capacitorless DRAM cell. This structure provides a physical well together with an electrostatic barrier to more effectively store holes and thereby achieve larger sensing margin as well as retention time. The advantages of this new cell design as compared with the planar cell design are assessed via two-dimensional device simulations. The results indicate that the convex heterojunction channel design is very promising for future capacitorless DRAM.**

Keywords-Capacitorless DRAM; Retention Time; Convex Channel; Silicon Germanium;

I. INTRODUCTION

In order to overcome cell area scalability and process complexity issues of traditional DRAM (1 transistor + 1 capacitor cell design) technology, the concept of capacitorless DRAM was introduced in early 1990s [1]. However, traditional types of capacitorless DRAM cells are difficult to scale into the sub-50nm gate length regime. Thus, there have been many efforts to investigate improved cell designs. Multiple-gate cell designs have been proposed [2,3]. Recently, the capacitorless DRAM Generation 2 (BJT-based) cell design was developed to improve sensing margin [4]. Han *et al.* introduced a band-engineered Unified-RAM (NVM + capacitorless DRAM) [5] in which a buried SiGe layer is used (instead of a buried oxide layer) to avoid the need for a silicon-on-insulator substrate.

In this work, a convex channel structure is proposed for the capacitorless DRAM Generation 2 type cell [4] to improve retention time. In order to retain the holes stored beneath the gate even more effectively in the Hold state, a smaller bandgap material such as silicon-germanium can be used in the convex channel region. The benefits of the convex channel structure are evaluated using two-dimensional device simulation with Sentaurus v.2008.09.

II. CELL OPERATING PRINCIPLE

The previously proposed capacitorless DRAM Generation 2 cell design is illustrated in Figure 1. Note that the body region is lightly doped ($2x10^{15}cm^{-3}$), so that punch-through can occur during a read operation, for enhanced read current in the "1" state (holes stored). The solid lines in Figure 1(b) show the energy-band diagram for the Hold state after a Write "1" operation. Note that the stored holes reduce the potential

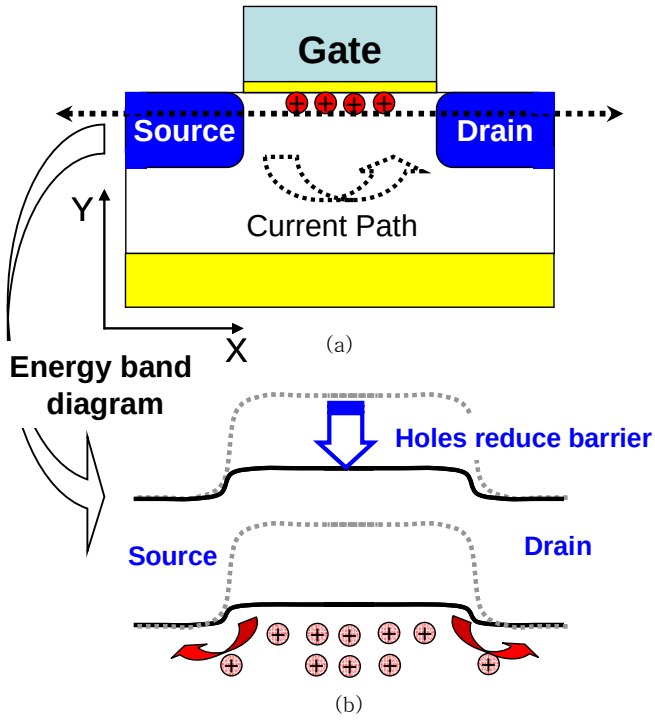

Figure 1. Capacitorless DRAM Generation 2 cell: (a) schematic cross-section. (b) energy band diagram along the channel surface. The dotted lines are for the "0" state in which no holes are stored. The solid lines are for the "1" state in which holes (generated by impact ionization during a Write "1" operation) are stored and hence the potential barrier between the source and body is reduced.

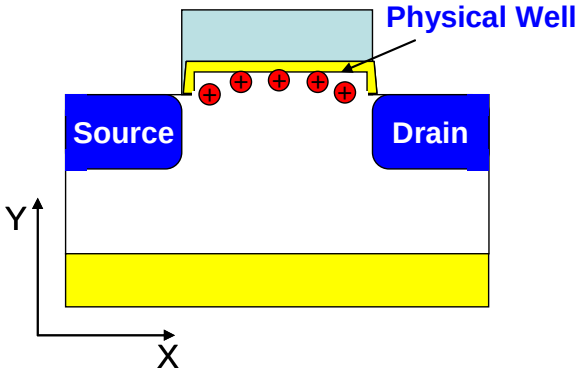

Figure 2. Proposed new convex channel (physical well) design. The increased volume of the charge-storage region enhances retention time.

barrier, so that they can more easily diffuse into the source and drain regions, undesirably reducing the retention time and sensing margin. In order to mitigate this problem, the convex channel design (Figure 2) is proposed to provide a physical well for more effective storage of holes. If a smaller-bandgap material such as $Si_{0.8}Ge_{0.2}$ is used in the convex channel region, then a deeper potential well also is formed for the holes (Figure 3), and retention time should be further increased.

In this work, the performance characteristics of the three capacitorless DRAM Generation 2 cell designs are compared: "Flat Si" (Figure 1), "Convex Si" (Figure 2), and "Convex $Si_{0.8}Ge_{0.2}$" (Figure 3). The gate length L_g = 80nm and gate-oxide thickness T_{ox} = 3nm in each cell design. The convex portion of the channel is 8nm thick and more heavily doped (with a Gaussian profile peaked at $7x10^{16}cm^{-3}$ at the convex channel surface) to store holes more effectively. (The doping level cannot be too high, however; otherwise the "0" state read current is increased.). The body and source/drain doping profiles are the same for all three cell designs.

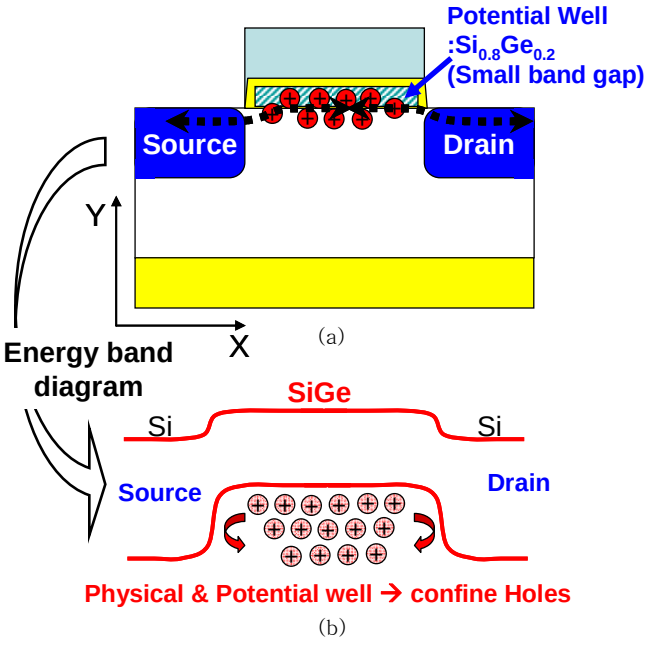

Figure 3. Convex $Si_{1-x}Ge_x$ cell design : (a) schematic cross-section. (b) energy band diagram from source to drain region. A deeper potential well for holes is formed, due to the valence band offset between $Si_{1-x}Ge_x$ and Si.

III. Results and Discussion

A. Simulated cell operation

There are four modes of operation for a capacitorless DRAM cell: Write "1", Write "0", Hold, and Read. The sequence of cell operations simulated in this work is shown in Table I, along with the operating voltages. It should be noted that these voltages have not yet been optimized; in general, lower voltages are desirable. During each of the cell operations, the source and substrate are always grounded at 0V.

In order to avoid erroneous simulation results, a Hold step (20nsec in duration) is applied between Read and Write steps. (Note that the longer the Hold time, the lower the Read current.) Figure 4 shows the hole density profiles for the two states: there are many holes beneath the gate after a Write "1" operation, whereas most of the holes have been swept away after a Write "0" operation.

TABLE I. Sequence of cell operations simulated, and Cell Operation Voltages

Initial → Write 1 → Hold → Read 1 → Hold → Write 0 → Hold → Read 0 → Hold				
	Vg(V)	Vd(V)	Vs,Vsub(V)	Time(nsec)
Write "1"	−0.5	4	0	20
Hold	−3.5	0	0	20
Read	−0.5	1	0	20
Write "0"	−0.5	−2	0	20

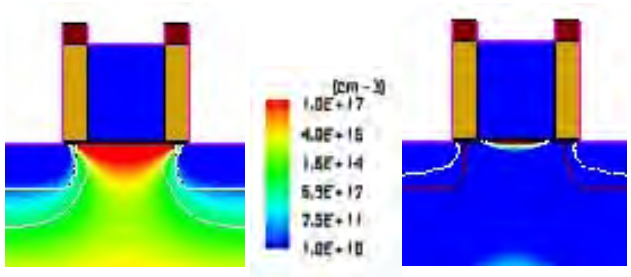

Figure 4. Hole density contour maps for a Flat Si cell. (a) Hold state after Write "1": many holes are stored underneath the gate. (b) Hold state after Write "0": holes have been swept away.

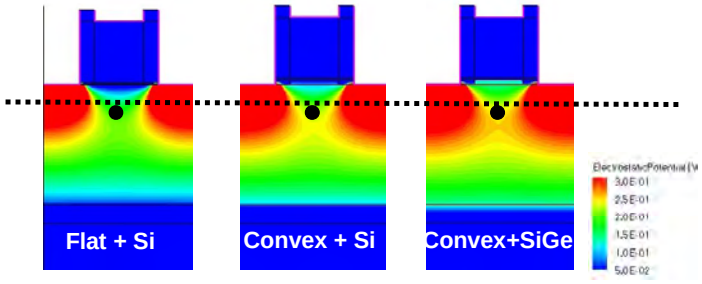

Figure 5. Contour maps of electrostatic potential in the Hold state after a Write "1" operation. The dotted line is shown as a reference for Figure 6, and the large black dots are shown as a reference for Figure 8.

B. Sensing margin

The sensing margin is one of most important performance parameters for capacitorless DRAM. It is defined to be the difference between Read "1" current and Read "0" current. In this study, its value is taken after 3nsec write time.

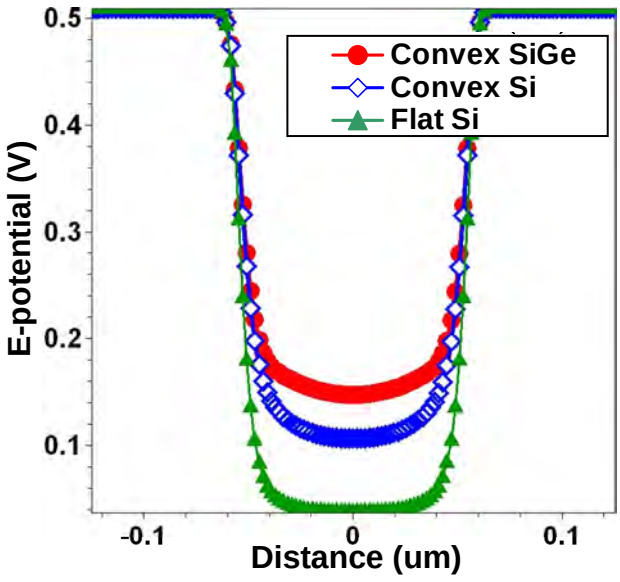

Figure 6. Potential profiles along the x-axis (ref. dotted lines in Figure 5), for cells in the Hold state after a Write "1" operation. The hole potential barrier from the body to the source/drain regions is lowest for the Convex SiGe structure, due to more effective hole storage.

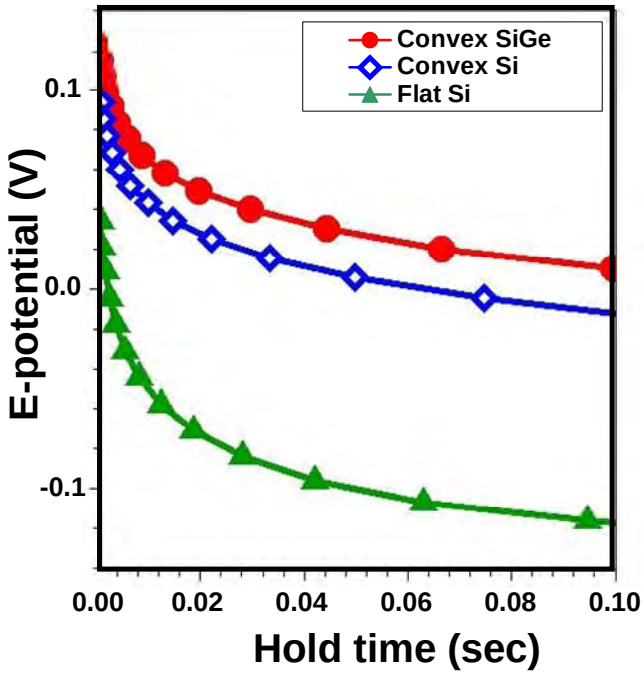

Figure 8. Electrostatic potential at the location in the cell indicated by the black dots in Figure 5 (60 nm below the source/drain surface) *vs*. Hold time, for cells after a Write "1" operation.

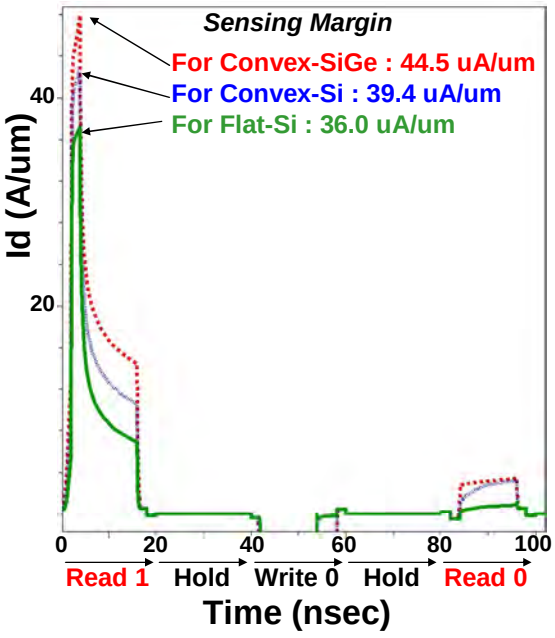

Figure 7. Cell current *vs*. time for the sequence of operations described in Table I. The sensing margin is defined to be the difference between Read "1" current and Read "0" current.

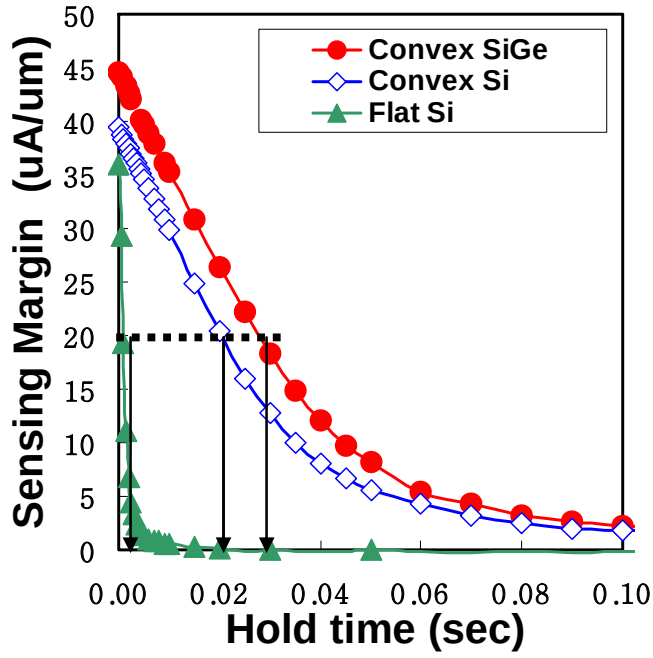

Figure 9. Sensing margin *vs*. Hold time. The Flat Si cell design shows very short (1ms) retention time. Retention time at 20uA/um is improved to >21ms for the convex cell designs.

Figures 5 and 6 show a comparison of the electrostatic potential distributions in the Hold state after a Write "1" operation, for the three cell designs. The potential barrier for the Convex $Si_{0.8}Ge_{0.2}$ design is the smallest, indicating that more holes are stored, so that the Read "1" current is enhanced. Figure 7 compares cell currents for the three designs, during the various cell operations. The difference between the current during a Read "1" operation and the current during a Read "0" operation is defined to be the sensing margin. The sensing margin is enhanced to 39.4uA/um (from 36.0uA/um for the conventional Flat Si design) with the convex channel design, and is further improved to 44.5uA/um with $Si_{0.8}Ge_{0.2}$ as the material in the convex channel region.

C. Retention time

The main benefit of the convex channel design is increased retention time. This can be seen from Figure 8 which shows the electrostatic potential at the center of the body region *vs.* hold time, and even more so from Figure 9 which shows sensing margin *vs.* hold time. The convex channel structures show higher potential values because more holes are stored beneath the gate. As a result, they have dramatically higher Read "1" current hence sensing margin. Recently developed current sense amplifiers are able to detect a current difference down to 2~3uA [3]. In this work, retention time is defined as the time for the sensing margin to drop below 20uA/um [6]. From Figure 9 it can be seen that the retention time is improved dramatically from <1ms to 21ms with the convex channel design. The use of $Si_{0.8}Ge_{0.2}$ as the convex channel material further increases the retention time, to 29ms. It should be noted that the cell designs in this work have not been fully optimized, so that even better retention times should be achievable. However, the relative performance comparison of the various capacitorless DRAM cell structures in this work should still be valid.

IV. CONCLUSION

A convex channel structure is proposed to form a physical well for hole storage to enhance the performance of capacitorless DRAM Generation 2 type capacitorless DRAM cells. Two-dimensional device simulations show that the convex channel design provides for >10× improvement in retention time, as compared against the conventional flat channel design. The use of $Si_{0.8}Ge_{0.2}$ in the convex channel region provides for a deeper potential well and hence further improvement in retention time. Therefore, the convex-channel cell design appears promising for future high-density DRAM application.

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